Application Report
SPMA063–October 2013

Differences Between Stellaris® Tempest- and Firestorm-Class MCUs and Tiva™ C Series TM4C129x MCUs

Sue Cozart

ABSTRACT

This document addresses design considerations when migrating working designs from Tempest- and Firestorm-class Stellaris microcontrollers to Tiva TM4C129x microcontrollers. Topics covered include both software and hardware differences as well as feature changes and enhancements. All software differences are comprehended in the Driver Library APIs that are part of StellarisWare® and TivaWare™ for C Series. As a result, system designers are strongly encouraged to use Driver Library to write software, making it easy to port software between various Stellaris classes and Tiva C Series devices.

Contents

1 Introduction

In this document, information on implementation differences is presented by module with both hardware and software considerations discussed. In general, features that are the same on all devices are not mentioned. Not all modules are included on every part in a class. Modules that are on only one class of part are also not mentioned. In-depth descriptions of functions and features are not included; for further information on overall functionality or details on any item, see the device-specific data sheet. Also, in general, differences due to errata are not comprehended in this document; see the device-specific errata to ensure proper system design.

This document addresses differences between Tempest- and Firestorm-class MCUs and TM4C129x MCUs. For information on differences between Fury- through Firestorm-class devices and TM4C123x devices, see *Differences Between Stellaris® LM3S and Tiva™ C Series TM4C123x MCUs* (SPMA035). For information on differences between the TM4C123x and TM4C129x classes, see *Differences Between Tiva™ C Series TM4C Microcontrollers (AN01296)* (SPMA065).

NOTE: By using the APIs in the Driver Library in StellarisWare and TivaWare for C Series, software can be easily ported among the various MCUs as these APIs comprehend functional differences.

2 Determining the Product Class

Information is presented in terms of product class in this document. To determine what class a particular microcontroller is in, see the CLASS field in the Device Identification 0 (DID0) register at offset 0x400F.E000. The CLASS designations in this register are as follows:

- Sandstorm - 0x0
- Fury - 0x1
- DustDevil - 0x3
- Tempest - 0x4
- Firestorm - 0x6
- TM4C123x - 0x5
- TM4C129x - 0xA

To determine which microcontrollers are in a particular class, check the following TI web pages:

- Sandstorm-class
- Fury-class
- DustDevil-class
- Tempest-class
- Firestorm-class

3 ARM® Cortex™ CPU

Table 1. ARM Cortex-M Features

Feature	Tempest	Firestorm	TM4C129x
Cortex-M version	M3, r2p0	M3, r2p0	M4F, r0p1
Option to run SysTick from PIOSC/4	No	No	Yes
System clock must be greater than 8 MHz to access STRELOAD register	No	No	Yes

4 System Control

4.1 Peripheral Control and Capabilities

Table 2. Peripheral Control and Capabilities Registers

Feature	Tempest	Firestorm	TM4C129x
Legacy registers SRCR0-SRCR2, RCGC0-RCGC2, SCGC0-SCGC2, DCGC0-DCGC2, and DC0-DC9 present	Yes	Yes	No
Peripheral-specific registers SRn, RCGCn, SCGCn, DCGCn, xPP, xPC, and xCC present	No	No	Yes

4.2 Reset Operation

Table 3. Reset Operation

Feature	Tempest	Firestorm	TM4C129x
JTAG reset	All except VECTRESET	All except VECTRESET	Only POR
Filtering on $\overline{\text{RST}}$	No	No	Yes
Hardware System Service reset	No	No	Yes
MOSC fail	Reset only	Reset only	Reset or interrupt
Enhanced BOR function	No	No	Yes
Choice of reset behavior	No	No	Yes
Reset JTAG using TMS pin	No	No	Yes
POR does not complete until proper voltage	No	No	Yes
Hibernation reset reported in the Reset Cause register	No	No	Yes

4.3 Brown-Out Operation

Table 4. Brown-Out Operation

Feature	Tempest	Firestorm	TM4C129x
Default brown-out operation	Interrupt (1)	POR (1)	POR (1)
Enhanced brown-out operation	No	No	Yes
Brown-out control register	PBORCTL	PBORCTL	PTBOCTL
Power-temperature cause register	No	No	PWRTC

(1) If a brown-out condition occurs while the Flash memory is being programmed or erased, a system reset occurs regardless of the setting in the Power-On and Brown-Out Reset Control (PBORCTL) register.

4.4 Core Voltage and LDO

Table 5. Core Voltage and LDO

Feature	Tempest	Firestorm	TM4C129x
VDDC voltage	1.3 V	1.3 V	1.2 V
VDD voltage	3.0 to 3.6 V	3.0 to 3.6 V	2.97 to 3.63 V
VDDA voltage	3.0 to 3.6 V	3.0 to 3.6 V	2.97 to 3.63 V
LDO configurable	No	No	Yes
LDO output	Yes	Yes	No
LDOPCTL register present	No	No	Yes

4.5 Clocking

Table 6. System Clock Options

Feature	Tempest	Firestorm	TM4C129x
Crystal input	3.579545 MHz – 16.384 MHz (1)	3.579545 MHz – 16.384 MHz (1)	5 MHz – 25 MHz (2)
Clock configuration registers	RCC, RCC2, and DSLPCLKCFG	RCC, RCC2, and DSLPCLKCFG	RSCLKCFG, DSCLKCFG, PLLFREQ0 and PLLFREQ1
PLLSTAT register	No	No	Yes
MOSCIM bit in MOSCCTL register (MOSC Failure Action)	No	No	Yes
NOXTAL bit in MOSCCTL register (No Crystal Connected)	No	No	Yes
SESRC bit in MOSCCTL register (Single-Ended Source)	No	No	Yes
OSCRNG bit in MOSCCTL register (Oscillator Range)	No	No	Yes
PWRDN bit in MOSCCTL register (Power Down)	No	No	Yes
MOSCDPD bit in DSCLKCFG register (MOSC Disable Power Down)	No	No	Yes
DIVSCLK output signal	No	No	Yes
PLLCFG register	Yes	Yes	No
PLLFREQn registers	No	No	Yes

(1) If the PLL is not used, the minimum crystal frequency is 1 MHz.
(2) If the PLL is not used, the minimum crystal frequency is 4 MHz.

Table 7. Module Clocking

Feature	Tempest	Firestorm	TM4C129x
Hibernate RTCOSC	32.768-kHz oscillator; 4.194304-MHz crystal	32.768-kHz oscillator; 4.194304-MHz crystal	32.768-kHz oscillator; 32.768-kHz crystal, internal Hibernate LFIOSC
ADC	PLL/25 or 16-MHz system clock	PLL/25 or 16-MHz system clock	Derived from main PLL, 16-MHz MOSC or alternate clock (choose from PIOSC, LFIOSC, and Hibernation module RTCOSC)
USB	Dedicated PLL	Dedicated PLL	Derived from main PLL (1)

(1) The ULPI interface uses either the main PLL or the USB0CLK input.

Table 7. Module Clocking (continued)

Feature	Tempest	Firestorm	TM4C129x
Ethernet PHY	25-MHz crystal or oscillator connected to XTALNPHY and XTALPPHY	25-MHz crystal or oscillator connected to XTALNPHY and XTALPPHY	25-MHz MOSC
GPTM	System clock	System clock	System clock or alternate clock (choose from PIOSC, LFIOSC, and Hibernation module RTCOSC)
SSI baud clock	System clock	System clock	System clock or alternate clock (choose from PIOSC, LFIOSC, and Hibernation module RTCOSC)
UART baud clock	System clock	System clock	System clock or alternate clock (choose from PIOSC, LFIOSC, and Hibernation module RTCOSC)

4.6 NMI

Table 8. NMI Characteristics

Feature	Tempest	Firestorm	TM4C129x
NMI signal location	PB7	PB7	PD7 and PE7
NMI on watchdog timeout	No	No	NMIC
Tamper event can cause NMI	N/A	N/A	NMIC
NMI Cause register	No	No	NMIC

4.7 System Control Interrupt Sources

Table 9. System Control Interrupt Sources

Feature	Tempest	Firestorm	TM4C129x
MOFRIS	No	No	Yes
MOSCPUPRIS	No	No	Yes

4.8 GPIO High-Performance Bus Control

Table 10. GPIO Ports Available on AHB Bus

Feature	Tempest	Firestorm	TM4C129x
GPIO ports available on AHB bus	Port A - Port J	Port A - Port J	All ports available only on the AHB

4.9 Flash and EEPROM Memory Timing

Table 11. Flash and EEPROM Memory Timing Control

Feature	Tempest	Firestorm	TM4C129x
MEMTIM0 and DSMEMTIM0 registers	No	No	Yes

4.10 Peripheral Ready Registers

Table 12. Peripheral Ready Registers

Feature	Tempest	Firestorm	TM4C129x
Peripheral-specific PPx registers	No	No	Yes

4.11 Peripheral Power Control Features

Table 13. Peripheral Power Control Registers

Feature	Tempest	Firestorm	TM4C129x
USB Power Domain Status and Memory Power Control registers, USB Power Control register	No	No	USBPDS, USBMPC, PCUSB
Ethernet MAC Power Domain Status and Memory Power Control registers, Ethernet MAC Power Control and Ethernet PHY Power Control registers	No	No	EMACPDS, EMACMPC, PCEMAC, PCEPHY
LCD Power Domain Status and Memory Power Control registers, LCD Controller Power Control register	No	No	LCDPDS, LCDMPC, PCLCD
CAN Power Domain Status and Memory Power Control registers, CAN Power Control register	No	No	CANnPDS, CANnMPC, PCCAN
CRC and Cryptographic Modules Power Control register	N/A	N/A	PCCCM

4.12 Dynamic Power Management

Table 14. Dynamic Power Management Features

Feature	Tempest	Firestorm	TM4C129x
Ability to lower LDO in Deep-sleep mode	No	No	Yes
Ability to put Flash memory and SRAM in power saving modes in Sleep and Deep-sleep mode	No	No	Yes
Ability to power down the PIOSC in Deep-sleep mode	No	No	Yes

4.13 Driver Library APIs

In this section and sections like it throughout this document, the APIs shown in Table 15 are applicable APIs. The ROM version of the various APIs may or may not be included in the on-chip ROM. To determine which APIs are available in ROM, see the *Tiva C Series ROM User's Guide* (device-specific documents available through the product folders).

Table 15. System Control Driver Library Available Functions and Parameters

Driver Library Function/Parameter	Tempest	Firestorm	TM4C129x
SysCtlADCSpeedSet, SysCtlADCSpeedGet	Yes	Yes	No
SysCtlAltClockConfig	No	No	Yes
SysCtlClockFreqSet	No	No	Yes
SysCtlClockSet, SysCtlClockGet	Yes	Yes	No
SysCtlCodeSRAMSizeGet	Yes (1)	Yes (1)	Yes (1)
SysCtlClockOutConfig	No	No	Yes
SysCtlDeepSleepClockSet	Yes	Yes	No
SysCtlDeepSleepClockConfigSet	No	No	Yes
SysCtlFlashTming, SysCtlFlashDeepSleepTiming, SysCtlEEPROMTiming	No	No	Yes
SysCtlMOSCConfigSet, SYSCTL_MOSC_INTERRUPT, SYSCTL_MOSC_NO_XTAL, SYSCTL_MOSC_PWR_DIS, SYSCTL_MOSC_LOWFREQ, SYSCTL_MOSC_HIGHFREQ, SYSCTL_MOSC_SESRC	No	No	Yes
SysCtlNMIStatus, SysCtlNMIClear	No	No	Yes
SysCtlPeripheralPowerOff, SysCtlPeripheralPowerOn	No	No	Yes
SysCtlPeripheralReady	No	No	Yes
SysCtlPWMClockGet, SysCtlPWMClockSet	Yes	Yes	No
SysCtlResetBehaviorSet, SysCtlResetBehaviorGet	No	No	Yes
SysCtlResetCauseClear, SysCtlResetCauseGet, SYSCTL_CAUSE_HSRVREQ, SYSCTL_CAUSE_HIB	No	No	Yes
SysCtlVoltageEventConfig, SysCtlVoltageEventStatus, SysCtlVoltageEventClear	No	No	Yes

(1) Returns a 0 to indicate no code SRAM on these devices.

5 Hibernation Module

5.1 Features

Table 16. Hibernation Features

Feature	Tempest	Firestorm	TM4C129x
Battery-backed memory	64 words	64 words	16 words
VDD3ON mode	No	No	Yes
Hibernate with arbitrary power removal	No	No	Yes
WRC bit	Yes, some registers	Yes, some registers	Yes, most registers
GNDX pin	No	No	Yes
V_{DD} supplies power even when $V_{BAT} > V_{DD}$	No	No	Yes
Wake from GPIO or $\overline{RST}$	No	No	Yes
Tamper function	No	No	Yes
Low-frequency internal oscillator (LFIOSC)	No	No	Yes
Pins that do not retain state in VDD3ON mode	N/A	N/A	Port C[0:3]
Minimum Sysclk required when reading HIBRTCC	No	No	Yes
External wake interrupt can be used in run, sleep and deep-sleep modes	No	No	Yes
External wake interrupt must be manually cleared	No	No	Yes

5.2 Supporting Circuitry

Table 17. Required Supporting Circuitry

Feature	Tempest	Firestorm	TM4C129x
Supported crystal	4.194304 MHz	4.194304 MHz	32.768 kHz
External load resistor on crystal	Yes	Yes	No
External pull-up on HIB	Yes	Yes	No

5.3 Clocking Options

Table 18. Hibernation Clocking Options

Feature	Tempest	Firestorm	TM4C129x
Internal 32.768-kHz oscillator powered down during Hibernate if RTCEN bit is clear	Yes	Yes	No
Oscillator hysteresis control	No	No	Yes
Oscillator drive capability	No	No	Yes
Oscillator bypass	No	No	Yes
Hibernation Low-Frequency Oscillator (HIBLFIOSC)	No	No	Yes
Hibernate clock (RTCOSC) can be used as the system clock source	No	No	Yes

5.4 Battery Management

Table 19. Battery Management Options

Feature	Tempest	Firestorm	TM4C129x
Configurable low-battery threshold	No	No	Yes
Software check of battery level	No	No	Yes
Hold off HIBREQ if battery low	No	No	Yes
Battery voltage monitored in Hibernate	No	No	Yes
Wake on low battery	No	No	Yes

5.5 Real-Time Clock (RTC)

Table 20. Real-Time Clock Options

Feature	Tempest	Firestorm	TM4C129x
Sub-second counter	No	No	Yes
Hardware calendar and alarm functions	No	No	Yes
RTC clock output	No	No	Yes
Match registers	Two	Two	One
Trim value applied	After 64 seconds	After 64 seconds	When HIBRTCC bits [5:0] go from 0x00 to 0x01, regardless of HIBRTCLD value

5.6 Hibernate Interrupt Sources

Table 21. Hibernate Interrupt Sources

Feature	Tempest	Firestorm	TM4C129x
WC	No	No	Yes
RTCALT1	Yes	Yes	No
PADIOWK	No	No	Yes
RSTWK	No	No	Yes
VDDFAIL	No	No	Yes

5.7 Driver Library APIs

Table 22. Hibernate Driver Library Available Functions and Parameters

Driver Library Function/Parameter	Tempest	Firestorm	TM4C129x
HibernateBatCheckDone, HibernateBatCheckStart	No	No	Yes
HibernateCalendarSet, HibernateCalendarGet, HibernateCalendarMatchSet, HibernateCalendarMatchGet	No	No	Yes
HibernateClockConfig	No	No	Yes
HibernateClockSelect, HIBERNATE_CLOCK_SEL_DIV128	Yes	Yes	No
HibernateClockSelect, HIBERNATE_CLOCK_SEL_LFIOSC	No	No	Yes
HibernateCounterMode	No	No	Yes
HibernateIntClear, HibernateIntDisable, HibernateIntEnable, HibernateIntRegister, HibernateIntStatus, HibernateIntUnregister, HIBERNATE_INT_RTC_MATCH_1	Yes	Yes	No
HibernateIntClear, HibernateIntDisable, HibernateIntClear, HibernateIntDisable, HibernateIntClear, HibernateIntDisable, HIBERNATE_INT_WR_COMPLETE, HIBERNATE_INT_VDDFAIL, HIBERNATE_INT_RESET_WAKE, HIBERNATE_INT_GPIO_WAKE	No	No	Yes
HibernateLowBatGet, HibernateLowBatSet	No	No	Yes
HibernateRTCMatch1Get, HibernateRTCMatch1Set	Yes	Yes	No
HibernateRTCSSGet, HibernateRTCSSMatch0Get, HibernateRTCSSMatch0Set	No	No	Yes
HibernateTamperEnable, HibernateTamperEventsConfig, HibernateTamperEventsGet, HibernateTamperEventsClear, HibernateTamperDisable, HibernateTamperIOEnable, HibernateTamperIODisable, HibernateTamperStatusGet, HibernateTamperExtOscRecover, HibernateTamperExtOscValid	No	No	Yes
HibernateWakeSet, HibernateWakeGet, HIBERNATE_WAKE_LOW_BAT, HIBERNATE_WAKE_GPIO, HIBERNATE_WAKE_RESET, HIBERNATE_WAKE_TAMPER	No	No	Yes

6 Internal Memory

6.1 Features

Table 23. Internal Memory Features

Feature	Tempest	Firestorm	TM4C129x
ROM	Yes	Yes	Yes
Flash Memory	16 KB - 256 KB	384 KB - 512 KB	512 KB - 1024 KB
SRAM	6 KB - 96 KB	48 KB - 96 KB	128 KB - 256 KB
EEPROM	N/A	N/A	6 KB

6.2 ROM Features

Table 24. ROM Features

Feature	Tempest	Firestorm	TM4C129x
Available Boot Loaders	UART0, SSI0, I2C0, Ethernet	UART0, SSI0, I2C0, Ethernet	UART0, SSI0, I2C0, USB
SafeRTOS	LM3S9B96, LM3S9BN6	LM3S9D96, LM3S9DN6, LM3S9U96	N/A

6.3 Flash Memory Features

Table 25. Flash Memory Features

Feature	Tempest	Firestorm	TM4C129x
Organization	1-KB blocks	1-KB blocks	2 (512-KB) or 4 (1024-KB) banks of 8 K x 128 bits, two-way interleaved
Erase size	1 KB	1 KB	16 KB
Speed	50 MHz	50 MHz	16 MHz
Prefetch buffer	2 32-bit words	2 32-bit words	2 or 4 x 256-bit buffer
FCTL register	Yes	Yes	No
Separate two writes to the same word with erase	Yes	Yes	No
Programmable wait states	No	No	Yes
Flash mirroring	No	No	Yes
Program protection	2-KB blocks	2-KB blocks	16-KB blocks
Read protection	2-KB blocks	2-KB blocks	2-KB blocks
µDMA read access	No	No	Yes
Choice of key value for FMC/FMC2 register (KEY bit in BOOTCFG register)	No	No	Yes
Flash Configuration register	No	No	FLASHCONF

6.4 Memory Registers

Table 26. Memory Registers

Feature	Tempest	Firestorm	TM4C129x
Reset Vector Pointer register	No	No	RVP
NW bit in the USER_REGn registers	Yes	Yes	No
ROM Control register	Yes	Yes	No
User Power-up Control register	No	No	USRPWRUP
Can change USER_REGn and BOOTCFG registers after committing	No	No	Yes

6.5 Internal Memory Interrupt Sources

Table 27. Internal Memory Interrupt Sources

Feature	Tempest	Firestorm	TM4C129x
PROGRIS, ERRIS, INVDRIS, VOLTRIS	No	No	Yes
ERIS	N/A	N/A	Yes

6.6 Driver Library APIs

Table 28. Internal Memory Driver Library Available Functions and Parameters

Driver Library Function/Parameter	Tempest	Firestorm	TM4C129x
FlashIntClear, FlashIntDisable, FlashIntEnable, FlashIntStatus, FLASH_INT_EEPROM, FLASH_INT_VOLTAGE_ERR, FLASH_INT_DATA_ERR, FLASH_INT_ERASE_ERR, FLASH_INT_PROGRAM_ERR	No	No	Yes

7 Micro Direct Memory Access (µDMA)

7.1 Features

NOTE: Driver Library APIs automatically adjust for these functional differences.

Table 29. µDMA Features

Feature	Tempest	Firestorm	TM4C129x
Transfer from Flash Memory	No	No	Yes
Possible channel mapping encoding	2	2	9
Option in basic mode to continue transferring as long as peripheral request is asserted	No	No	Yes
DMA Done interrupts in the Interrupt registers in each peripheral	No	No	Yes
Privilege access protection	No	No	Yes
DMA Channel Interrupt Status Register (DMACHIS)	No	Yes	No
DMA Channel Map Select n Registers (DMACHMAPn)	No	No	Yes

7.2 Peripherals

Table 30. Peripheral µDMA Request Types

Feature	Tempest	Firestorm	TM4C129x
ADC	Burst - triggered by sequencer IE bit	Burst - triggered by sequencer IE bit	Single - FIFO not empty Burst - FIFO half full
USB TX	FIFO TXRDY	FIFO TXRDY	USB has integrated DMA and does not use µDMA
USB RX	FIFO RXRDY	FIFO RXRDY	USB has integrated DMA and does not use µDMA
GPIO	N/A	N/A	Burst - trigger event
Ethernet TX	Single - TX FIFO empty	Single - TX FIFO empty	Ethernet has integrated DMA and does not use µDMA
Ethernet RX	Single - RX packet received	Single - RX packet received	Ethernet has integrated DMA and does not use µDMA
I2C TX	N/A	N/A	Single - TX buffer not full Burst - TX FIFO level (configurable)
I2C RX	N/A	N/A	Single - RX buffer not full Burst - RX FIFO level (configurable)

7.3 Driver Library APIs

Table 31. µDMA Driver Library Available Functions and Parameters

Driver Library Function/Parameter	Tempest	Firestorm	TM4C129x
µDMAChannelAssign	No	No	Yes
µDMAChannelSelectDefault, µDMAChannelSelectSecondary	Yes	Yes	Yes (1)
µDMAIntClear, µDMAIntStatus	No	No	Yes

(1) These APIs work for parameters that match those available on Tempest- and Firestorm-class parts. For mappings that are added in the TM4C129x microcontrollers, use the µDMAChannelAssign function.

8 General-Purpose Input/Outputs (GPIOs)

8.1 Features

Table 32. GPIO Features

Feature	Tempest	Firestorm	TM4C129x
Input voltage tolerance	5 V	5 V	3.3 V (1)
Available ports	A - E, 64-pin parts; A - J, 100/108-pin parts	A - E, 64-pin parts; A - J, 100/108-pin parts	A - Q, 128-pin parts A - T, 212-pin parts
6-, 10- and 12-mA drive options	No	No	Yes
Interrupts per pin	No	No	Yes
Trigger µDMA	No	No	Yes
ADC trigger	PB4	PB4	Any GPIO
Pins that can wake from Hibernation	N/A	N/A	Port K [7:4]
Pins with default functions	PA[1:0] - UART0 PA[5:2] - SSI0 PB[3:2] - I2C0 PC[3:0] - JTAG/SWD	PA[1:0] - UART0 PA[5:2] - SSI0 PB[3:2] - I2C0 PC[3:0] - JTAG/SWD	PC[3:0] - JTAG/SWD
µDMA Done interrupt	No	No	Yes

(1) PB1 (USB0VBUS) is 5-V tolerant.

8.2 Driver Library APIs

Table 33. GPIO Driver Library Available Functions and Parameters

Driver Library Function/Parameter	Tempest	Firestorm	TM4C129x
PB4 is selected as the ADC trigger source using the ADCSequenceConfigure function.	No (1)	No (1)	Yes
GPIODMATriggerDisable, GPIODMATriggerEnable	No	No	Yes
GPIOIntEnable, GPIOIntDisable, GPIOIntStatus, GPIOIntClear	No	No	Yes
GPIOIntTypeGet, GPIOIntTypeSet, GPIO_DISCRETE_INT	No	No	Yes
GPIOPadConfigSet, GPIOPadConfigGet, GPIO_STRENGTH_6MA, GPIO_STRENGTH_10MA, GPIO_STRENGTH_12MA, GPIO_PIN_TYPE_WAKE_HIGH, GPIO_PIN_TYPE_WAKE_LOW	No	No	Yes

(1) PB4 is selected as the ADC trigger source using the ADCSequenceConfigure function.

9 External Peripheral Interface (EPI)

9.1 Features

Table 34. EPI Features

Feature	Tempest	Firestorm	TM4C129x
Maximum EPI clock speed	50 MHz	50 MHz	60 MHz
Integer divide option for EPI baud rate	No	No	Yes
Support for 512 Mb PSRAM	No	No	Yes
Read/Write Burst mode to host bus	No	No	Yes
Quad Chip Select with and without ALE modes	No	No	Yes
Automatic routing of data onto proper byte lanes	No	No	Yes (1)
Configurable ALE polarity	No	No	Yes
Option to invert EPI clock in Host Bus mode	No	No	Yes
External iRDY signal in Host Bus mode	No	No	Yes
External iRDY signal in General Purpose mode	Yes	Yes	No
Enhanced wait state precision in Host Bus mode	No	No	Yes
Option for 2-cycle reads in general-purpose mode	Yes	Yes	No (2)
External code addressing	No	No	Yes
Additional µDMA configurability	No	No	Yes
µDMA Done interrupt	No	No	Yes

(1) In Tempest- and Firestorm-class devices, the WORD bit must be set in the EPIHB8CFG2, EPIHB16CFG2, or EPIGPCFG2 register to enable this function.

(2) In Tempest- and Firestorm-class devices, the RD2CYC bit was required to be set. On TM4C129x devices, all reads are two cycles.

9.2 Driver Library APIs

Table 35. EPI Driver Library Available Functions and Parameters

Driver Library Function/Parameter	Tempest	Firestorm	TM4C129x
EPIAddressMapSet, EPI_ADDR_QUAD_MODE, EPI_ADDR_CODE_SIZE_256B, EPI_ADDR_CODE_SIZE_64KB, EPI_ADDR_CODE_SIZE_16MB, EPI_ADDR_CODE_SIZE_256MB, EPI_ADDR_CODE_BASE_NONE, EPI_ADDR_CODE_BASE_1	No	No	Yes
EPIConfigHB8CSSet, EPIConfigHB16CSSet	Yes	Yes	Yes
EPIConfigHB8CSSet, EPIConfigHB16CSSet	Yes	Yes	No (1)
EPIConfigHB16Set, EPI_HB16_WORD_ACCESS	Yes	Yes	No (1)
EPIConfigGPModeSet, EPI_GPMODE_WORD_ACCESS, EPI_GPMODE_READ2CYCLE	Yes	Yes	No
EPIConfigHB8ModeSet, EPI_HB8_ALE_HIGH, EPI_HB8_ALE_LOW, EPI_HB8_CSCFG_ALE_SINGLE_CS, EPI_HB8_CSCFG_QUAD_CS, EPI_HB8_CSCFG_ALE_QUAD_CS, EPI_HB8_CLOCK_GATE, EPI_HB8_CLOCK_GATE_IDLE, EPI_HB8_CLOCK_INVERT, EPI_HB8_IN_READY_EN, EPI_HB8_IN_READY_EN_INVERT	No	No	Yes

(1) The functionality configured using this setting is used automatically.

Table 35. EPI Driver Library Available Functions and Parameters (continued)

Driver Library Function/Parameter	Tempest	Firestorm	TM4C129x
EPIConfigHB16ModeSet, EPI_HB16_ALE_HIGH, EPI_HB16_ALE_LOW, EPI_HB16_CSCFG_ALE_SINGLE_CS, EPI_HB16_CSCFG_QUAD_CS, EPI_HB16_CSCFG_ALE_QUAD_CS, EPI_HB16_CLOCK_GATE, EPI_HB16_CLOCK_GATE_IDLE, EPI_HB16_CLOCK_INVERT, EPI_HB16_IN_READY_EN, EPI_HB16_IN_READY_EN_INVERT, EPI_HB16_BURST_TRAFFIC	No	No	Yes
EPIConfigHB8TimingSet, EPIConfigHB16TimingSet	No	No	Yes
EPIDividerCSSet	No	No	Yes
EPIDMATxCount	No	No	Yes
EPIIntEnable, EPIIntDisable, EPIIntStatus, EPI_INT_DMA_TX_DONE, EPI_INT_DMA_RX_DONE	No	No	Yes
EPIIntEnable, EPIIntDisable, EPIIntStatus, EPI_INT_DMA_TX_DONE, EPI_INT_DMA_RX_DONE	No	No	Yes

10 General-Purpose Timers

10.1 Features

Table 36. GP Timer Features

Feature	Tempest	Firestorm	TM4C129x
Timer synchronization	No	No	Yes
Timers can be clocked from alternate clock	No	No	Yes
Configurable ADC and µDMA trigger events	No	No	Yes
Timer Compare Action mode	No	No	Yes
µDMA Done interrupt	No	No	Yes

Table 37. GP Timer Added Registers

Feature	Tempest	Firestorm	TM4C129x
GPTMTnPV registers	No	No	Yes
GPTMTnPS registers	No	No	Yes
GPTMRTCPD register	No	No	Yes

10.2 Periodic and One-Shot Mode Features

Table 38. Periodic and One-Shot Mode Features

Feature	Tempest	Firestorm	TM4C129x
Delayed load of new load value	No	No	Yes
Delayed load of new match value	No	No	Yes

10.3 Real-Time Clock (RTC) Mode Features

Table 39. RTC Mode Features

Feature	Tempest	Firestorm	TM4C129x
Delayed load of new load value	No	No	Yes
Delayed load of new match value	No	No	Yes

10.4 Input Edge-Count Mode Features

Table 40. Input Edge-Count Mode Features

Feature	Tempest	Firestorm	TM4C129x
Count direction	Down	Down	Down or Up
Delayed load of new load value	No	No	Yes
Delayed load of new load value	No	No	Yes

10.5 Input Edge-Time Mode Features

Table 41. Input Edge-Time Mode Features

Feature	Tempest	Firestorm	TM4C129x
Count direction	Down	Down	Down or Up
Prescaler available	No	No	Yes (1)
Delayed load of new load value	No	No	Yes
Delayed load of new load value	No	No	Yes

(1) In this mode, the prescaler acts as a timer extension and holds the most-significant bits of the count.

10.6 PWM Mode Features

Table 42. PWM Mode Features

Feature	Tempest	Firestorm	TM4C129x
Prescaler available	No	No	Yes
Wait on trigger	No	No	Yes
Delayed load of new load value	No	No	Yes
Option to set CCP to 1 at timeout	No	No	Yes

10.7 Driver Library APIs

Table 43. Timer Driver Library Available Functions and Parameters

Driver Library Function/Parameter	Tempest	Firestorm	TM4C129x
TimerADCEventSet, TimerADCEventGet	No	No	Yes
TimerConfigure, TIMER_CFG_A_ACT_TOINTD, TIMER_CFG_A_ACT_NONE, TIMER_CFG_A_ACT_TOGGLE, TIMER_CFG_A_ACT_CLRTO, TIMER_CFG_A_ACT_SETTO, TIMER_CFG_A_ACT_SETTOGTO, TIMER_CFG_A_ACT_CLRTOGTO, TIMER_CFG_A_ACT_CLRSETTO, TIMER_CFG_B_ACT_TOINTD, TIMER_CFG_B_ACT_NONE, TIMER_CFG_B_ACT_TOGGLE, TIMER_CFG_B_ACT_CLRTO, TIMER_CFG_B_ACT_SETTO, TIMER_CFG_B_ACT_SETTOGTO, TIMER_CFG_B_ACT_CLRTOGTO, TIMER_CFG_B_ACT_CLRSETTO, TIMER_CFG_A_ONE_SHOT_UP, TIMER_CFG_A_PERIODIC_UP, TIMER_CFG_B_ONE_SHOT_UP, TIMER_CFG_B_PERIODIC_UP, TIMER_CFG_ONE_SHOT_UP, TIMER_CFG_PERIODIC_UP	No	No	Yes
TimerClockSourceSet, TimerClockSourceGet	No	No	Yes
TimerDMAEventSet, TimerDMAEventGet	No	No	Yes
TimerIntEnable, TimerIntDisable, TimerIntClear, TimerIntStatus, TIMER_TIMA_DMA, TIMER_TIMB_DMA	No	No	Yes
TimerSynchronize	No	No	Yes

11 Watchdog Timers

11.1 Features

Table 44. Watchdog Timer Features

Feature	Tempest	Firestorm	TM4C129x
NMI option	No	No	Yes

11.2 Driver Library APIs

Table 45. Watchdog Timer Driver Library Available Functions and Parameters

Driver Library Function/Parameter	Tempest	Firestorm	TM4C129x
WatchdogIntTypeSet	No	No	Yes

12 Analog-to-Digital Converters (ADC)

12.1 Features

Table 46. ADC Features

Feature	Tempest	Firestorm	TM4C129x
Resolution	10-bit	12-bit, with 10-bit compatibility mode	12-bit
Analog inputs	Up to 16	Up to 16	Up to 24
2 Msps operation	No	No	Yes
Voltage reference	Internal 3 V, external 3 V	Internal 3 V, internal 1 V, external 3 V	VDDA / GNDA, VREFA+ / VREFA- or VREFA+ only, depending on package type
Enhanced µDMA interface	No	No	Yes
Clock option	PLL/25, MOSC	PLL/25, MOSC	Derived from main PLL, MOSC, or alternate clock
PLL clocking option	Automatic PLL / 25	Automatic PLL / 25	VCO frequency must be configured to provide a clock in the proper range
ADC Busy bit	No	No	Yes
Never trigger option available	No	No	Yes
Dither mode available	No	No	Yes
Configurable sample and hold time	No	No	Yes

12.2 Driver Library APIs

Table 47. ADC Driver Library Available Functions and Parameters

Driver Library Function/Parameter	Tempest	Firestorm	TM4C129x
ADCBusy	No	No	Yes
ADCIntDisableEx, ADCIntEnableEx, ADCIntStatusEX, No ADCIntClearEx	No	No	Yes
ADCReferenceGet, ADCReferenceSet, No ADC_REF_EXT_1V	No	Yes	No
ADCResolutionGet, ADCResolutionSet	No	Yes	No
ADCSequenceConfigure, ADC_TRIGGER_NEVER	No	No	Yes
ADCSequenceDMAEnable, No ADCSequenceDMADisable	No	No	Yes

13 Universal Asynchronous Receivers/Transmitters (UARTs)

13.1 Features

Table 48. UART Features

Feature	Tempest	Firestorm	TM4C129x
9-bit support	No	No	Yes
Clocking options	System clock only	System clock only	System clock or alternate clock
Modem support	Modem flow control and status on UART1 on some devices	Modem flow control and status on UART1 on some devices	Modem flow control and status on UART0 and UART1 Modem flow control on UART2, UART3, and UART4
Enhanced µDMA interface	No	No	Yes

13.2 Driver Library APIs

Table 49. UART Driver Library Available Functions and Parameters

Driver Library Function/Parameter	Tempest	Firestorm	TM4C129x
UART9BitAddrSend, UART9BitAddrSet, UART9BitDisable, UART9BitEnable	No	No	Yes
UARTClockSourceGet, UARTClockSourceSet	No	No	Yes
UARTIntEnable, UARTIntDisable, UARTIntClear, UARTIntStatus, UART_INT_9BIT, UART_INT_DMARX, UART_INT_DMATX	No	Yes	No

14 Synchronous Serial Interface (SSI)

14.1 Features

Table 50. SSI Features

Feature	Tempest	Firestorm	TM4C129x
Module types	Up to two legacy modules	Up to two legacy modules	Four modules support legacy, advance, bi-SSI and quad-SSI
Maximum master clock speed	1/2 system clock speed up to 25 MHz	1/2 system clock speed up to 25 MHz	1/2 system clock speed
SSI0 transmit and receive pin mapping	SSI0Rx - PA4 SSI0Tx - PA5	SSI0Rx - PA4 SSI0Tx - PA5	SSI0XDAT1 (SSI0Rx) - PA5 SSI0XDAT0 (SSI0Tx) - PA4
Enhanced µDMA interface	No	No	Yes
High-speed clock option	No	No	Yes
Clocking options	System clock only	System clock only	System clock or alternate clock
Supported frame formats	TI, Freescale, Microwire	TI, Freescale, Microwire	TI, Freescale
Separate EOT interrupt	No	No	Yes
FSS hold frame option	No	No	Yes

14.2 Driver Library APIs

Table 51. SSI Driver Library Available Functions and Parameters

Driver Library Function/Parameter	Tempest	Firestorm	TM4C129x
SSIAdvDataPutFrameEnd, SSIAdvDataPutFrameEndNonBlocking	No	No	Yes
SSIAdvFrameHoldEnable, SSIAdvFrameHoldDisable	No	No	Yes
SSIAdvModeSet	No	No	Yes
SSIClockSourceGet, SSIClockSourceSet	No	No	Yes
SSIIntEnable, SSIIntDisable, SSIIntClear, SSIIntStatus, SSI_DMARX, SSI_DMATX, SSI_TXEOT	No	No	Yes
SSISlaveDiv6Enable, SSISlaveDiv6Disable	No	No	Yes

15 Inter-Integrated Circuit (I2C) Interface

15.1 Features

Table 52. I2C Features

Feature	Tempest	Firestorm	TM4C129x
SCL signal must be configured as open drain	Yes	Yes	No
High-speed operation	No	No	Yes
Dual-slave address	No	No	Yes
Clock-low timeout	No	No	Yes
ACK override	No	No	Yes
Receive and transmit FIFOs	No	No	Yes
µDMA support	No	No	Yes
Glitch suppression option	No	No	Yes
Burst operation option	No	No	Yes

15.2 I2C Interrupt Sources

Table 53. I2C Interrupt Sources

Feature	Tempest	Firestorm	TM4C129x
CLKRIS (Clock timeout interrupt)	No	No	Yes
DMARXRIS, DMATXRIS (µDMA interrupts)	No	No	Yes
NACKRIS (NACK interrupt)	No	No	Yes
STARTRIS, STOPRIS (start and stop detection)	No	No	Yes
ARBLOSTRIS (arbitration lost)	No	No	Yes
RXRIS, TXRIS (FIFO interrupts)	No	No	Yes
TXFERIS, RXFFRIS (FIFO interrupts)	No	No	Yes
DATARIS (slave data interrupt)	No	No	Yes

15.3 Driver Library APIs

Table 54. I2C Driver Library Available Functions and Parameters

Driver Library Function/Parameter	Tempest	Firestorm	TM4C129x
I2CFIFOStatus, I2CFIFODataPut, I2CFIFODataPutNonBlocking, I2CFIFODataGet, I2CFIFODataGetNonBlocking	No	No	Yes
I2CMasterBurstLengthSet, I2CMasterBurstCountGet	No	No	Yes
I2CMasterControl, I2C_MASTER_CMD_FIFO_SINGLE_SEND, I2C_MASTER_CMD_FIFO_SINGLE_RECEIVE, I2C_MASTER_CMD_FIFO_BURST_SEND_START, I2C_MASTER_CMD_FIFO_BURST_SEND_CONT, I2C_MASTER_CMD_FIFO_BURST_SEND_FINISH, I2C_MASTER_CMD_FIFO_BURST_SEND_ERROR_STOP, I2C_MASTER_CMD_FIFO_BURST_RECEIVE_START, I2C_MASTER_CMD_FIFO_BURST_RECEIVE_CONT, I2C_MASTER_CMD_FIFO_BURST_RECEIVE_FINISH, I2C_MASTER_CMD_FIFO_BURST_RECEIVE_ERROR_STOP	No	No	Yes
I2CMasterGlitchFilterConfigSet	No	No	Yes
I2CMasterIntEnableEx, I2CMasterIntDisableEx, I2CMasterIntStatusEx, I2CMasterIntClearEx, I2C_MASTER_INT_TIMEOUT, I2C_MASTER_INT_RX_FIFO_FULL, I2C_MASTER_INT_TX_FIFO_EMPTY, I2C_MASTER_INT_RX_FIFO_REQ, I2C_MASTER_INT_TX_FIFO_REQ, I2C_MASTER_INT_ARB_LOST, I2C_MASTER_INT_STOP, I2C_MASTER_INT_START, I2C_MASTER_INT_NACK, I2C_MASTER_INT_TX_DMA_DONE, I2C_MASTER_INT_RX_DMA_DONE	No	No	Yes
I2CMasterLineStateGet	No	No	Yes
I2CMasterTimeoutSet	No	No	Yes
I2CMasterMultiMasterEnable, I2CMasterMultiMasterDisable	No	No	Yes
I2CRxFIFOConfigSet, I2CRxFIFOFlush	No	No	Yes
I2CSlaveACKOverride, I2CSlaveACKValueSet	No	No	Yes
I2CSlaveAddressSet, secondary address	No	No	Yes
I2CSlaveFIFOEnable, I2CSlaveFIFODisable	No	No	Yes
I2CSlaveIntEnable, I2CSlaveIntDisableEx, I2CSlaveIntStatusEx, I2CSlaveIntClearEx, I2C_SLAVE_INT_RX_FIFO_FULL, I2C_SLAVE_INT_TX_FIFO_EMPTY, I2C_SLAVE_INT_RX_FIFO_REQ, I2C_SLAVE_INT_TX_FIFO_REQ, I2C_MASTER_INT_ARB_LOST, I2C_SLAVE_INT_TX_DMA_DONE, I2C_SLAVE_INT_RX_DMA_DONE	No	No	Yes
I2CSlaveStatus, I2C_SLAVE_ACT_OWN2SEL, I2C_ACT_QCMD, I2C_SLAVE_ACT_QCMD_DATA	No	No	Yes
I2CTxFIFOConfigSet, I2CTxFIFOFlush	No	No	Yes
GPIOPinTypeI2C for SCL signal	No	No	No
GPIOPinTypeI2CSCL	No	No	Yes

16 Controller Area Network (CAN) Module

There are no differences among the CAN modules between Tempest- and Firestorm-class and TM4C129x devices.

17 Ethernet Controller

17.1 Features

This module is a complete redesign from the module on the LM3S devices.

Table 55. Ethernet Controller Features

Feature	Tempest	Firestorm	TM4C129x
Bias pull-down resistor	ERBIAS, 12.4 KΩ ± 1 %	ERBIAS, 12.4 KΩ ± 1 %	RBIAS, 4.87 KΩ ± 1 %
Flow control and back pressure	No	No	Yes
Enhanced auto-negotiation	No	No	Yes
IEEE 802.1Q VLAN tag detection	No	No	Yes
Enhanced IEEE 1588 support	No	No	Yes
Source and destination address filters	No	No	Yes
Programmable hash filter for multicast address filtering	No	No	Yes
Programmable insertion or deletion of preamble and SOF data	No	No	Yes
Programmable insertion or deletion of CRC and pad data	No	No	Yes
IPv4 and TCP header checksum calculation	No	No	Yes
MII and RMII support	MII support only on devices without integrated PHY	MII support only on devices without integrated PHY	Yes, only on some devices
RMON/MIB counters for network statistics	No	No	Yes
Magic packet and wakeup frame support	No	No	Yes
Integrated DMA controller with bus master capability	No	No	Yes

17.2 MAC Register Differences

The Ethernet MAC register model is completely different on the TM4C129x devices from the Tempest- and Firestorm-class devices.

17.3 PHY Register Differences

The Ethernet PHY register model is completely different on the TM4C129x devices from the Tempest- and Firestorm-class devices, with the exception of the first seven standard registers.

17.4 Driver Library APIs

The Ethernet API is completely changed for the TM4C129x devices from the Tempest- and Firestorm-class devices. For system designers who use lwIP for their Ethernet stack, moving their code is very straightforward as they just have to include lwIP version 4 in their project. For system designers who do not use lwIP, code must be rewritten using the EMACXxxx APIs instead of the EthXxxx APIs in Driver Library. For more information, see the *Ethernet Controller (New Device Classes)* chapter in the *TivaWare™ Peripheral Driver Library User's Guide* (SPMU298).

18 Universal Serial Bus (USB) Controller

18.1 Features

Table 56. USB Controller Features

Feature	Tempest	Firestorm	TM4C129x
Endpoints	32	32	16
Integrated USB DMA with bus master capability	No	No	Yes
ULPI interface with optional high-speed operation	No	No	Yes
Link Power Management (LPM) mode	No	No	Yes
USB0RBIAS pin	Yes	Yes	No
Enhanced control of USB0VBUS and USB0ID signals	No	No	Yes
Valid ID detect	Yes	Yes	No
Test packet support	No	No	Yes
USB information registers (USBEPINFO and USBRAMINFO)	No	No	Yes
Ping disable	No	No	Yes
Incomplete RX transmission status	No	No	Yes

18.2 Driver Library APIs

Table 57. USB Driver Library Available Functions and Parameters

Driver Library Function/Parameter	Tempest	Firestorm	TM4C129x
USBClockEnable, USBClockDisable	No	No	Yes
USBControllerVersion	No	No	Yes
USBDevEndpointConfigSet, USB_EP_DIS_NYET, USB_EP_SPEED_HIGH, USB_EP_DMA_INT_EN, USB_EP_DMA_DISABLE	No	No	Yes
USBDevLPMConfig, USBDevLPMRemoteWake, USBDevLPMEnable, USBDevLPMDisable	No	No	Yes
USBDMAChannelAddressSet, USBDMAChannelAddressGet, USBDMAChannelCountSet, USBDMAChannelCountGet, USBDMANumChannels, USBDMAChannelAssign	No	No	Yes
USBDMAChannelEnable, USBDMAChannelDisable, USBDMAChannelConfigSet, USBDMAChannelStatus, USBDMAChannelStatusClear	No	No	Yes
USBDMAChannelIntEnable, USBDMAChannelIntDisable, USBDMAChannelIntStatus	No	No	Yes
USBDMAError, USBDMAErrorClear	No	No	Yes
USBDMAModeSet, USBDMAModeGet	No	No	Yes
USBHighSpeed, USBDevSpeedGet	No	No	Yes
USBHostEndpointSpeed, USBHostEndpointPing	No	No	Yes
USBHostLPMConfig, USBHostLPMSend, USBHostLPMResume	No	No	Yes
USBHostSpeedGet, USB_HIGH_SPEED	No	No	Yes
USBLPMLinkStateGet, USBLPMIntEnable, USBLPMIntDisable, USBLPMIntStatus	No	No	Yes
USBRequestPacketCountSet	No	No	Yes
USBULPIConfig, USBULPIEnable, USBULPIDisable, USBULPIRegRead, USBULPIRegWrite	No	No	No

19 Analog Comparators

There are no differences among the Analog Comparators between Tempest- and Firestorm-class and TM4C129x devices.

20 Pulse Width Modulator (PWM)

20.1 Features

Table 58. PWM Controller Features

Feature	Tempest	Firestorm	TM4C129x
PWM Clock Configuration register	Run-mode Clock Configuration (RCC) register in System Control	Run-mode Clock Configuration (RCC) register in System Control	PWMCC

20.2 Driver Library APIs

Table 59. PWM Driver Library Available Functions and Parameters

Driver Library Function/Parameter	Tempest	Firestorm	TM4C129x
PWMClockSet, PWMClockGet	No	No	Yes

21 Quadrature Encoder Interface (QEI)

There are no differences among the QEI modules between Tempest- and Firestorm-class and TM4C129x devices.

22 Packaging and Pinout

22.1 Packages

Table 60. Device Packages

Feature	Tempest	Firestorm	TM4C129x
64-pin LQFP, 10 x 10 mm body size, 0.50 mm pitch	Yes	Yes	No
100-pin LQFP, 14 x 14 mm body size, 0.50 mm pitch	Yes	Yes	No
108-ball BGA, 10 x 10 mm body size, 0.8 mm pitch, 12 x 12 array	Yes	Yes	No
128-pin TQFP, 14 x 14 mm body size, 0.40 mm pitch	No	No	Yes
212-ball BGA, 10 x 10 mm body size, 0.5 mm pitch, No 19 x 19 array	No	No	Yes

22.2 Pinout Comparison

Table 61. Device Pinout

Feature	Tempest	Firestorm	TM4C129x
ADC	Top left corner	Top left corner	Corner Bottom right
Hibernate	Bottom right corner	Bottom right corner	Corner Right side of
JTAG	Right side of top	Right side of top	Right side of top
LDO/VDDC	LQFP - Center top and bottom sides; LDO on top of left side BGA - Left side of center opening	LQFP - Center top and bottom sides; LDO on top of left side BGA - Left side of center opening	LQFP - Center top side, center bottom side BGA - Center at the top and right of the center cluster
UART0	Left of bottom side	Left of bottom side	Left of bottom side
SSI0	Left of bottom side	Left of bottom side	Left of bottom side
I2C0	Top of right side	Top of right side	Top of right side
USB0	Top of right side	Top of right side	Top of right side
Ethernet	LQFP - Center and right side of bottom, center of right side; XTAL pins center left side BGA - Bottom right corner; XTAL pins center left side	LQFP - Center and right side of bottom, center of right side; XTAL pins center left side BGA - Bottom right corner; XTAL pins center left side	Right side of bottom; Separate XTAL no longer needed
Reset	Center of right side	Center of right side	Lower right side
Oscillator pins	Right side of bottom	Right side of bottom	Upper right side

23 Conclusion

Between Tempest- and Firestorm-class Stellaris microcontrollers and Tiva C Series TM4C129x microcontrollers, there are minor hardware and software differences. This application report has provided an overview of these differences. By using Driver Library APIs, software can be easily ported between the various classes.

24 References

The following related documents and software are available on the TI web site. Documents can also be found through the Tiva Technical Documents search tab.

- Tiva C Series Data Sheet (individual device documents available through the product folders)
- *Tiva™ C Series TM4C129x Microcontrollers Silicon Revisions 1 and 2 Silicon Errata* (SPMZ850)
- TivaWare Peripheral Driver Library for C Series
- *TivaWare™ Peripheral Driver Library User's Guide* (SPMU298)
- *Tiva™ C Series TMS4C129x ROM User's Guide* (SPMU363)
- *Differences Among Stellaris® LM3S and Tiva™ C Series TM4C123x MCUs* (SPMA035)
- *Transitioning Designs from Stellaris® LM3S Microcontrollers to Tiva™ C Series Microcontrollers* (SPMA049)
- *Differences Between Tiva™ C Series TM4C Microcontrollers* (SPMA065)
- *Migrating Software Projects from StellarisWare® to TivaWare™* (SPMA050)
- *System Design Guidelines for the TM4C129x Family of Tiva™ C Series Microcontrollers* (SPMA056)
- *System Design Guidelines for the TM4C123x Family of Tiva™ C Series Microcontrollers* (SPMA059)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265