Application Report
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TMS320x2833x/2823x to TMS320x2834x Delfino Migration Overview

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ABSTRACT

This application report describes differences between the Texas Instruments TMS320x2833x/2823x and the TMS320x2834x Delfino™ devices to assist in application migration. While the main focus of this document is migration from TMS320x2833x/2823x to TMS320x2834x, you will also find this document useful if you are considering migrating in the reverse direction. Functions that are identical in both devices are not necessarily included. All efforts have been made to provide a comprehensive list of the differences between the two device groups in the 28x generation; however, the descriptions are explained only to the extent of highlighting areas that require attention when moving an application from one device to another.

Note: For a detailed description of features specific to each device, see the most recent device-specific data manuals, errata, user guides, and software packages.

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1 Introduction

The TMS320x2833x/2823x and TMS320x2834x devices are members of the C2000™ device generation for use within embedded control applications. The TMS320x2834x devices operate up to 300 MHz and do not include any Flash or one time programmable (OTP) memory.

For purposes of migration, these devices can be thought of in two groups:

1. TMS320x2833x and TMS320x2823x
2. TMS320x2834x

As the focus of this document is to describe the differences between the two device groups, the descriptions are explained only to the extent of highlighting areas that require attention when moving an application from one device to the other. For a detailed description of features specific to each device, see the device-specific data manuals and user guides available on the TI website at http://www.ti.com. This application report does not cover the silicon exceptions or advisories that may be present on each device. Consult the following silicon errata for specific advisories and workarounds:

- *TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232 DSC Silicon Errata* (SPRZ193)
- *TMS320C2834x Delfino MCU Silicon Errata* (SPRZ267)

Note: Always refer to the TMS data manual for information regarding any electrical specifications.

1.1 Abbreviations

The following abbreviations are used in this document:

- 2833x: Refers to the TMS320x2833x devices. For example, TMS320F28335, TMS320F28334 and TMS320F28332.
- 2823x: Refers to the TMS320x2823x devices. For example, TMS328F28235, TMS320F28234 and TMS320F28232.
- 2834x: Refers to the TMS320x2834x devices. For example, TMS320C28346, TMS320C28345, TMS320C28344, TMS320C28343, TMS320C28342 and TMS320C28341.
- C28x+FPU refers to the C28x plus floating point unit.
- CCS refers to Code Composer Studio™ software.

For a full list of devices currently available within the 2833x/2823x and 2834x families, see the TI website.

2 Developments Tools

A new set of header files and peripheral examples are available for the C2834x with the same structure as the 2833x/2823x header files. For more information, see the *C2834x C/C++ Header Files and Peripheral Examples* (SPRC876).

3 Package and Pinout

Both F2833x/F2823x and C2834x devices have a 179-pin u*BGA (ZHH) package that are not pin compatible. All other packages are neither package nor pin compatible. Any application being moved from 2833x or 2823x to the 2834x requires a new board layout to accommodate the changes in the pinout and the package.

4 Operating Frequency and Power Supply

The 2833x/2823x devices require only two voltage rails: one for the core voltage and another for the I/O voltage. The 2834x devices require three voltage rails: one for the core voltage, one for the I/O voltage and one for the oscillator/phase-locked loop (PLL) voltage.

- F2833x/F2823x - two voltage rails:
  - Core voltage
    - 1.9 V for 150 Mhz devices
    - 1.8 V for 100 MHz devices
  - 3.3-V I/O voltage
- C2834x - three voltage rails:
  - Core voltage
    - 1.2 V for 300 MHz devices
    - 1.1 V for 200 MHz devices
  - 3.3-V I/O voltage
  - 1.8-V oscillator/PLL voltage

5 Power Sequencing

There is one additional voltage rail to consider on the 2834x devices. For the 2833x/2823x devices, V_{DD} pins can be powered prior to or simultaneously with the V_{DDIO} pins. For the 2834x, this behavior still holds. Additionally, the 1.8-V V_{DDK} rail can be powered along with the V_{DD} and V_{DDIO} pins.

See the appropriate data manual for each device for details related to power sequencing:

- *TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232 Digital Signal Controllers (DSCs) Data Manual* (SPRS439)
- *TMS320C28346, TMS320C28345, TMS320C28344, TMS320C28343, TMS320C28342, TMS320C28341 Delfino Microcontrollers Data Manual* (SPRS516)

6 Static Random Access Memory (SARAM)

This section highlights the major differences in the SARAM memory subsystem.

Increased amount of SARAM

On the 2833x/2823x, up to 34K x 16 words of SARAM are available. On the 2834x, up to 258K x 16 words are available.

Maximum SARAM block size 32K x 16

L0-L7 SARAM blocks have increased to 8K x 16 words each on the 2834x compared to the 4Kx16 SARAM block size on the 2833x/2823x. Additionally, six additional 32K x 16 word blocks have been added to the 2834x to replace the flash blocks on the 2833x/2823x.

SARAM blocks no longer dual-memory mapped

Memory blocks L0, L1, L2, and L3 are dual-mapped into both high and low memory on the 2833x/2823x devices. This is no longer the case with the 2834x devices - L0-L7 SARAM blocks exist in the low 64K memory space only. H0-H5 SARAM blocks now exist in the high 64K memory space.

Wait states and DMA accessibility

On the 2833x/2823x, L0-L3 are not DMA-accessible, and are 0-wait state for CPU data and program read/write accesses. L4-L7 are DMA-accessible and are 0-wait state for CPU data read/write accesses and 1-wait state for CPU program read/write accesses. DMA data read/write accesses are all 0-wait state. On the 2834x, L0-L7 are all DMA-accessible. CPU data and program read/write accesses are 0-wait state for L0-L5. L6 and L7 CPU data and program read/write accesses are 1-wait state. DMA read/write accesses are 1-wait state for L0-L7. CPU data and program read/write accesses are 1-wait state for H0-H5. Program accesses to the H0-H5 memories have an op-code pre-fetch to improve throughput. For more information on wait-states, see the device-specific data manual.

7 Flash and OTP

Unlike the 2833x/2823x, the 2834x has no Flash or OTP memories.

Table 1. SARAM/Flash/OTP Memory Addresses

Memory Address	2833x/2823x Memory Block	2834x Memory Block
0x008000 - 0x008FFF	L0 SARAM	L0 SARAM
0x009000 - 0x009FFF	L1 SARAM	
0x00A000 - 0x00AFFF	L2 SARAM	L1 SARAM
0x00B000 - 0x00BFFF	L3 SARAM	
0x00C000 - 0x00CFFF	L4 SARAM	L2 SARAM
0x00D000 - 0x00DFFF	L5 SARAM	
0x00E000 - 0x00EFFF	L6 SARAM	L3 SARAM
0x00F000 - 0x00FFFF	L7 SARAM	
0x010000 - 0x011FFF	unused	L4 SARAM
0x012000 - 0x013FFF	unused	L5 SARAM
0x014000 - 0x015FFF	unused	L6 SARAM
0x016000 - 0x017FFF	unused	L7 SARAM
0x300000 - 0x307FFF	Flash	H0 SARAM
0x308000 - 0x30FFFF	Flash	H1 SARAM
0x310000 - 0x317FFF	Flash	H2 SARAM
0x318000 - 0x31FFFF	Flash	H3 SARAM
0x320000 - 0x327FFF	Flash	H4 SARAM
0x328000 - 0x32FFFF	Flash	H5 SARAM
0x330000 - 0x33FFF7	Flash	Reserved
0x33FFF8 - 0x33FFFF	128-Bit Password	128-Bit Password
0x380000 - 0x3807FF	TI & User OTP	Unused
0x3F8000 - 0x3F8FFF	L0 (dual-mapped)	Unused
0x3F9000 - 0x3F9FFF	L1 (dual-mapped)	Unused
0x3FA000 - 0x3FAFFF	L2 (dual-mapped)	Unused
0x3FB000 - 0x3FBFFF	L3 (dual-mapped)	Unused

8 Boot ROM

The Boot ROM on the 2834x devices is very similar to the 2833x/2823x Boot ROM. The following changes have been made:

- Due to the lack of Flash memory on the 2834x, the *Jump to Flash Boot Mode* has been removed and replaced by a TI Test mode.
- The inter-integrated circuit (I2C) bootloader has two timing modes because the 2834x devices can run at two different maximum frequencies: 300 MHz and 200 MHz.
  - I2C Timing 1: This mode is the same as 2833x/2823x. The expectations are:
    - SYSCLK = CLKIN/2
    - 28 MHz < CLKIN < 48 MHz
    - I2C_Init:
      `I2caRegs.I2CPSC.all = 0x1;`
  - I2C Timing 2: This mode is the same as 280x /2801x /2804x. It replaces the *Boot to Flash, skip ADC Calibration* mode on the 2833x/2823x devices. The expectations are:
    - SYSCLK = CLKIN/2
    - 14 MHz < CLKIN < 24 MHz
    - I2C_Init:
      `I2caRegs.I2CPSC.all = 0x0;`
- The eCAN bootloader has two timing modes because C2834x devices can run at two different maximum frequencies: 300 MHz and 200 MHz.
  - eCAN-A Timing 1: For users who want to use a 30 Mhz input. In this case, DIVSEL is configured such that SYSCLKOUT is equal to the input clock. It replaces the *eCAN-A* boot mode on 2833x and 2823x devices.
  - eCAN-A Timing 2: For users who wish to use a 20 Mhz input. In this case, DIVSEL is configured such that SYSCLKOUT is 1/2 of the input clock. It replaces the *Jump to OTP* mode on 2833x and 2823x devices.

These timing sets provide the bit rates as shown in Table 2:

Table 2. eCAN-A Boot Timing Sets

Bit Time	XCLKIN	SYSCLK	CAN Clock	Bit Rate	PLL Divider
15	30 MHz	30 MHz	7.5 MHz	500 kbps	/1
10	20 MHz	10 MHz	2.5 MHz	250 kbps	/2

Boot-Mode Selection

The boot-mode pin configuration is very similar for both device families. Some boot modes no longer exist due to the non-existent Flash and OPT.

The boot-mode selection table for 2834x is shown in Table 3.

Table 3. 2834x Boot-Mode Selection Table

Mode	GPIO87 XA15	GPIO86 XA14	GPIO85 XA13	GPIO84 XA12	Mode (1)
F	1	1	1	1	TI Test Only
E	1	1	1	0	SCI-A Boot
D	1	1	0	1	SPI-A Boot
C	1	1	0	0	I2C-A Boot Timing 1
B	1	0	1	1	eCAN-A Boot Timing 1
A	1	0	1	0	McBSP-A Boot
9	1	0	0	1	Jump to XINTF x16
8	1	0	0	0	Reserved
7	0	1	1	1	eCAN-A Boot Timing 2
6	0	1	1	0	Parallel GPIO I/O Boot
5	0	1	0	1	Parallel XINTF Boot
4	0	1	0	0	Jump to SARAM
3	0	0	1	1	Branch to Check Boot Mode
2	0	0	1	0	I2C-A Boot Timing 2
1	0	0	0	1	Reserved
0	0	0	0	0	TI Test Only

(1) All four GPIO pins have an internal pullup.

For more information on the Boot ROM, see the *TMS320x2833x, 2823x System Control and Interrupts Reference Guide* (SPRUFB0) and the *TMS320x2834x Boot ROM Reference Guide* (SPRUFN5).

9 Clocks and System Control

This section describes changes that affect device clocking and system control. This includes new and renamed registers, pin functionality, new logic, and other enhancements. For more information on system control, see the following reference guides:

- *TMS320x2833x, 2823x System Control and Interrupts Reference Guide* (SPRUFB0)
- *TMS320x2834x System Control and Interrupts Reference Guide* (SPRUFN1)

9.1 Register Changes

Table 4 shows a summary of registers that were added, renamed, or modified from the 2833x/2823x devices. The sections that follow describe the changes that were made.

Table 4. New and Updated System Control Registers

Register	Change	Description
PCLKCR2	Updated	Updated to support EPWM9 and EQEP3 clock enables
PCLKCR0	Updated	Updated to support SPI-D and remove ADC clock enables
PCLKCR1	Updated	Updated to support EPWM7 and EPWM8 clock enables
HISPCP	Updated	HSPCLK bit field=00000 disables HSPCLK on C2834x/C2823x. Bitfield is now 5 bits wide.
PLLCR	Updated	PLLCR bit field is now 5 bits and SYSCLKOUT = CLKIN * (PLLCR+1)/DIVSEL
PLLSTS	Updated	DIVSEL bit field = 0 is /8 instead of /4, and limp mode bits have been removed.
EXTSOCCFG	New	Added to support external ADC interface

9.2 Input Oscillator

External Clock Connections

A separate ground pin on the 2834x, V_{SSK}, has been added to complement the V_{DD18} oscillator voltage rail. Therefore, there are several external clock connection differences on these devices compared to the 2833x/2823x devices. Table 5 and Table 6 show the differences in oscillator connections between the two device families due to the additional V_{SSK} ground pin.

Table 5. 2834x Oscillator Connections

External Clock Connection Options	XCLKIN	X1	X2
Using 3.3 V External Oscillator	External 3.3 V clock signal	V_{SSK} (oscillator ground)	No Connect
Using 1.8 V External Oscillator	V_{SS} (V_{DD}/V_{DDIO} ground)	External 1.8 V clock signal	No Connect
Using Internal Oscillator	V_{SS} (V_{DD}/V_{DDIO} ground)	Crystal connected across X1 and X2 that are connected to capacitors C1 and C2, respectively, which then connect to V_{SSK} (oscillator ground)	

Table 6. 2833x Oscillator Connections

External Clock Connection Options	XCLKIN	X1	X2
Using 3.3 V External Oscillator	External 3.3 V clock signal	V_{SS} (ground)	No Connect
Using 1.8 V External Oscillator	V_{SS} (ground)	External 1.8 V clock signal	No Connect
Using Internal Oscillator	V_{SS} (ground)	Crystal connected across X1 and X2 that are connected to capacitors CL1 and CL2, respectively, which then connect to V_{SS} (ground)	

Input Clock Range

On the 2833x/2823x, the allowable frequency range for resonators and crystals is 20-35 MHz. On the 2834x, this is limited to 20-30 MHz.

Oscillator Missing Detect Logic

Unlike the 2833x/2823x, the 2834x does not support a limp mode clock and missing clock detection logic. Therefore, the OSCOFF, MCLKSTS, MCLKCLR, and MCLKOFF bits no longer exist in the PLL Status Register (PLLSTS) on these devices.

9.3 Phase Locked Loop (PLL)

PLL Control Register

On the 2833x/2823x, the PLL Control Register (PLLCR) DIV bit field is 4-bits wide where VCOCLK = CLKIN * DIV, and 0 <= DIV <= 10. On the 2834x, the DIV bit field is 5-bits wide where VCOCLK = CLKIN * (DIV + 1), and 0 <= DIV <= 31.

PLL Divider Selection Bit

On the 2833x/2823x, the maximum PLLSTS[DIVSEL] divider is /4 (default). The DIVSEL bit field allows for /4, /2, and /1 modes. /1 mode can be used, but the duty cycle may not be clean while the PLL is enabled. On the 2834x, the maximum PLLSTS[DIVSEL] divider is /8 (default). This allows for /8, /4, /2, and /1 modes. /1 mode is not recommended while the PLL is enabled because the duty cycle will not be clean.

PLL Output Frequency

On the 2833x/2823x devices, the input clock and PLLCR[DIV] bits should be chosen in such a way that the output frequency of the PLL (VCOCLK) does not exceed 300 MHz. On the 2834x devices, the input clock and PLLCR[DIV] bits should be chosen in such a way that the output frequency of the PLL (VCOCLK) falls between 400 MHz and 600 MHz.

9.4 Peripheral Clock Enable Registers

Due to the addition of new peripheral instances and the removal of the ADC module on the 2834x, the registers to enable and disable the clocks to individual peripherals have been updated. On the 2833x/2823x devices, the PCLKCR2 register is reserved and not used. This register now includes the EPWM9 and EQEP3 clock enables on the 2834x.

9.5 External ADC Interface Settings

While the 2833x/2823x devices have an on-chip ADC module, the module has been removed from the 2834x devices. Instead, these devices have an external ADC interface. The EXTSOCCFG register is new to the 2834x to support the external ADC interface on these devices. The High-Speed Peripheral Clock Pre-Scaler Register (HISPCP [HSPCLK]) bit field configures the external ADC clock (EXTADCCLK) rate with reference to SYSCLKOUT and the clock output of this prescaler is used to generate SOC's. The HSPCLK bit field has been expanded to 5-bits to offer a wider range of prescaler options. On the 2833x/2823x, the setting HISPCP[HSPCLK] = 0000b sets the HSPCLK frequency equal to SYSCLKOUT/1. Now setting HISPCP[HSPCLK] = 00000b disables the HSPCLK, and therefore, disables the EXTADCCLK.

9.6 General Purpose Input/Output (GPIO) and External Signals

On the 2833x/2823x devices, GPBMUX2 (GPIO48-63) peripheral selection 2 and 3 both result in the selection of XINTF XD[31:16] pins. On the 2834x, peripheral selection 2 remains the same while peripheral selection 3 results in the selection of other new peripherals added on the 2834x devices (SPI-D, EQEP3, and EPWM7-9). Additionally, the external TCK pin on the 2834x devices requires an external pull-up resistor (2.2 kΩ resistor should be sufficient). On the 2833x/2823x devices, the TCK pin has an internal pull-up resistor.

9.7 Security

The 2833x/2823x devices allow you to program a 128-bit password into the password locations at 0x33FFF8- 0x33FFFF in order to lock secure memories on a device. By default, the 2834x devices do not allow 128-bit passwords to be programmed into the password locations. These locations will always read back 0xFFFF. To preserve compatibility with other C28x™ DSP designs, the password locations must be read after a device reset. Otherwise the *secure* memories will appear locked. Custom secure versions of these devices are available where the 128-bit password locations are set to a customer-chosen value, and a TI-generated AES decryption routine is embedded into an on-chip secure ROM, providing a method to secure application code that is stored externally. Call TI for more details about this option.

10 Peripherals

Most of the peripherals on the 2834x devices are identical to those on the 2833x/2823x devices. Several peripherals have been either slightly modified or removed. This section briefly describes the changes. For an overview of all peripherals available, see the *TMS320x28xx, 28xxx DSP Peripheral Reference Guide* (SPRU566).

10.1 Enhanced Control Peripherals

The enhanced capture (eCAP), enhanced pulse width modulator (ePWM), high resolution PWM (HRPWM), and enhanced quadrature encoder pulse (eQEP) modules remain functionally the same. The register sets are identical on the two device groups: the memory addresses of the registers for each instance of peripheral are also identical. For example, Ehanced Pulse With Modulator Registers (ePWM1) on the 2833x/2823x are at the same location as ePWM1 registers on the 2834x. In addition, the interrupt vector location in the PIE vector table is identical. New interrupt vectors have been added to the PIE vector table for the additional peripheral instances (i.e., ePWM7-9 and eQEP3). The HRPWM on the 2834x devices operates at a typical resolution of 60 ps, while the 2833x/2823x HRPWM operates at a typical resolution of 150 ps. There are two other notable differences to the control modules:

- ePWM and eCAP Synchronization

  Due to the addition of ePWM7-9 on the 2834x, the synchronization scheme varies slightly between 2833x/2823x and 2834x. For more information, see the device-specific *Enhanced Pulse Width Modulator (ePWM) Module Reference Guides* and the device-specific *Enhanced Capture (eCAP) Module Reference Guides*. Otherwise, code that has been written for these modules on the 2833x/2823x can be directly targeted for the 2834x.
- ePWM Connection to DMA

  On the 2833x/2823x, the ePWM/HRPWM module registers can be re-mapped to peripheral frame 3 where they can be accessed by the DMA module. The MAPCNF[MAPEPWM] bit defines whether the ePWM/HRPWM registers are mapped to peripheral frame 1 or if they are mapped to peripheral frame 3. On the 2834x, the ePWM/HRPWM module registers are only mapped to peripheral frame 1 and cannot be re-mapped. There is no MAPCNF register on the 2834x.

Table 7. Available Control Peripherals

Device	ePWM With High Resolution (HRPWM)	ePWM	eCAP	eQEP
28335, 28235	ePWM1 - ePWM6	ePWM1 - ePWM6	eCAP1 - eCAP6	eQEP1, eQEP2
28334, 28234	ePWM1 - ePWM6	ePWM1 - ePWM6	eCAP1 - eCAP4	eQEP1, eQEP2
28332, 28232	ePWM1 - ePWM4	ePWM1 - ePWM6	eCAP1 - eCAP4	eQEP1, eQEP2
28346, 28345, 28344, 28343	ePWM1 - ePWM9	ePWM1 - ePWM9	eCAP1 - eCAP6	eQEP1 - eQEP3
28342, 28341	ePWM1 - ePWM6	ePWM1 - ePWM6	eCAP1 - eCAP4	eQEP1, eQEP2

10.2 Communication Peripherals

The serial communications interface (SCI), serial peripheral interface (SPI), multichannel buffered serial port (McBSP), and inter-integrated circuit (I2C) modules remain functionally the same. The register sets are identical on the two device groups. The memory addresses of the registers for each instance of peripheral are also identical. For example, the SPI-A registers on 2833x/2823x are at the same location as SPI-A registers on 2834x. In addition, the interrupt vector location in the PIE vector table is identical. New interrupt vectors have been added to the PIE vector table for the additional peripheral instances (i.e., SPI-D). Code that has been written for the I2C, SCI, SPI or McBSP on the 2833x/2823x can be directly targeted for the 2834x.

The 2834x eCAN is now clocked at one-fourth the SYSCLKOUT frequency, unlike 2833x/2823x which clocks the eCAN module at one-half the SYSCLKOUT frequency. Code written for the eCAN needs to take this timing change into account. Otherwise, the eCAN module is functionally the same and the register sets are identical on the two device groups.

Table 8. Available Communication Peripherals

Device	I2C	SCI	SPI	eCAN	McBSP
28335/28235	I2C-A	SCI-A, SCI-B, SCI-C	SPI-A	eCAN-A, eCAN-B	McBSP-A, McBSP-B
28334/28234	I2C-A	SCI-A, SCI-B, SCI-C	SPI-A	eCAN-A, eCAN-B	McBSP-A, McBSP-B
28332/28232	I2C-A	SCI-A, SCI-B	SPI-A	eCAN-A, eCAN-B	McBSP-A
28346/28345/ 28344/28343	I2C-A	SCI-A, SCI-B, SCI-C	SPI-A, SPI-D	eCAN-A, eCAN-B	McBSP-A, McBSP-B
28342/28341	I2C-A	SCI-A, SCI-B, SCI-C	SPI-A, SPI-D	eCAN-A, eCAN-B	McBSP-A

10.3 External Interface (XINTF)

The functionality of the XINTF module remains mostly the same on the 2833x/2823x and 2834x devices. On the 2834x, an additional divide-by-2 bit (XINTCNF2[BY4CLKMODE]) has been added. On the 2833x/2823x devices, XCLKOUT = SYSCLKOUT/1, SYSCLKOUT/2, or SYSCLKOUT/4. The new BY4CLKMODE bit allows an additional XCLKOUT = SYSCLKOUT/8 option on the 2834x devices.

Additionally, the XA0 and $\overline{\text{XWE1}}$ XINTF signals are multiplexed on the 2833x/2823x devices. These signals are independent signals on the 2834x devices.

11 Interrupts

The functionality of the PIE module and of the PIE configuration registers remains the same. The PIE vector table has been updated to accommodate the interrupts issued by the new peripheral blocks such as SPI-D, ePWM 7-9, ePWM7-9 TZ, and eQEP3. ADC interrupts have also been removed because there is no on-chip ADC module on the C2834x devices.

12 Errata Fixes

For more information on the various advisories, see the TI website for the most recent device-specific silicon errata. This includes:

- *TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232 DSC Silicon Errata* (SPRZ272)
- *TMS320C2834x Delfino MCU Silicon Errata* (SPRZ267)

13 References

- http://www.ti.com
- *TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232 DSC Silicon Errata* (SPRZ193)
- *TMS320C2834x Delfino MCU Silicon Errata* (SPRZ267)
- *C2833x/C2823x C/C++ Header Files and Peripheral Examples* (SPRC530)
- *TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232 Digital Signal Controllers (DSCs) Data Manual* (SPRS439)
- *TMS320x2833x Analog-to-Digital Converter (ADC) Module Reference Guide* (SPRU812)
- *TMS320x2833x, 2823x System Control and Interrupts Reference Guide* (SPRUFB0)
- *TMS320x28xx, 28xxx DSP Peripheral Reference Guide* (SPRU566)
- *TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232 DSC Silicon Errata* (SPRZ272)
- *C28x FPU Fast RTS Library* (SPRC664)
- *TMS320x2833x, 2823x Boot ROM Reference Guide* (SPRU963)
- *C2834x C/C++ Header Files and Peripheral Examples* (SPRC876)
- *TMS320C28346, TMS320C28345, TMS320C28344, TMS320C28343, TMS320C28342, TMS320C28341 Delfino Microcontrollers (MCUs) Data Manual* (SPRS516)

- *TMS320x2834x Boot ROM Reference Guide* (SPRUFN5)
- *TMS320x2834x System Control and Interrupts Reference Guide* (SPRUFN1)
- *TMS320C2834x Enhanced Pulse Width Modulator (ePWM) Module Reference Guide* (SPRUFZ6)
- *TMS320x2834x High Resolution Pulse Width Modulator (HRPWM) Reference Guide* (SPRUG77)
- *TMS320x2834x Direct Memory Access (DMA) Reference Guide* (SPRUG78)
- *TMS320C2834x External Interface (XINTF) Reference Guide* (SPRUFN4)

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