Application Report
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Usage Guidelines for C55x On-Chip Low Dropout Regulators (LDOs)

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ABSTRACT

The C5515/C5535/C5545/C5517 devices include three low dropout regulators ANA_LDO, DSP_LDO and USB_LDO. This application report provides the guidelines for using these on-chip low dropout regulators. This document also covers the USB power-up sequence that must be followed when using the device USB.

Contents

List of Figures

1 Introduction

The C5515/C5535/C5545/C5517 devices include three Low-Dropout Regulators (LDOs) that can be used to regulate the power supplies of the analog PLL and SAR ADC/Power Management (ANA_LDO), Digital Core (DSP_LDO), and USB Core (USB_LDO). These LDOs are controlled by a combination of pin configuration and register settings.

The LDOI pins provide power to the internal Analog LDO, DSP LDO, USB LDO, the bandgap reference generator, and some I/O input pins. The bandgap provides accurate voltage and current references to the POR, LDOs, PLL, and SAR; therefore, for proper device operation, power must always be applied to the LDOI pins even if the LDO outputs are not used.

CVDDRTC must also be supplied at RESET for proper power up. CVDDRTC must not be supplied by any on-chip LDO, even though it requires 1.3 V. You can use an external LDO or a resistor divider appropriately sized to maintain valid voltage and current into the CVDDRTC pin. For more information, see the device-specific data sheet.

The ANA_LDOO pin is the output of the internal ANA_LDO and can provide regulated 1.3 V power of up to the specified current rating in the data sheet. The ANA_LDOO pin is intended to be connected, on the board, to the VDDA_ANA and VDDA_PLL pins to provide a regulated 1.3 V to the 10-bit SAR ADC, Power Management Circuits, and System PLL. VDDA_ANA and VDDA_PLL may be powered by this LDO output, which is recommended, to take advantage of the device's power management techniques, or by an external power supply. The ANA_LDO cannot be disabled individually.

The ANA_LDO charges at the same rate as the bandgap circuit, which takes about 100 msec to charge the external 0.1 µF capacitor via the internal 326-kΩ resistor. It is recommended to use external supplies if the shortest boot time is required.

The DSP_LDOO pin is the output of the internal DSP_LDO and provides software-selectable regulated 1.3 V or regulated 1.05 V power of up to the specified current rating in datasheet. The DSP_LDOO pin is intended to be connected, on the board, to the CVDD pins. In this configuration, the DSP_LDO_EN pin must be tied to the board VSS, thus enabling the DSP_LDO. Optionally, the CVDD pins may be powered by an external power supply; in this configuration the DSP_LDO_EN pin must be tied (high) to LDOI, disabling DSP_LDO.

Also note that the DSP_LDO_EN is not intended to be changed dynamically.

The USB_LDOO pin is the output of the internal USB_LDO and provides regulated 1.3 V, software switchable (on/off) power of up to the specified current rating in the device-specific data sheet. The USB_LDOO pin is intended to be connected, on the board, to the USB_VDD1P3 and USB_VDDA1P3 pins to provide power to portions of the USB. Optionally, the USB_VDD1P3 and USB_VDDA1P3 can be powered by an external power supply and the USB_LDO can be left disabled.

When the USB_LDO is disabled, its output pin is in a high-impedance state.

2 Status of LDO's During Reset and Before TRIM Update

When internal LDOs are enabled, the LDO will not be trimmed (that is, adjusted to generate specified voltage levels) until after reset when the bootloader configures the TRIM register. The details of the analog TRIM update and un-trim LDO voltage are further explained below.

2.1 TRIM Update

The bandgap references may be relatively robust and accurate, but not immune to process variations and mismatch offsets whose adverse effects on accuracy varies across devices, wafers, lots, and technology nodes, making each device unique. As a result, trimming (that is, tweaking) the output voltage is necessary to produce predictable reference values, this is known as TRIM update.

2.2 Untrimmed LDO Voltages

- Untrimmed LDO voltage is the LDO voltage before the Analog TRIM register gets updated. As shown in Figure 1, the un-trimmed voltage level after the initial ramp can be between 0.95 V and 1.43 V.
- If you intend to use the untrimmed LDOs in your design for power sequencing (such as, for power good monitoring before releasing reset), then the respective power up sequence design must consider LDO operating from 0.95 V and greater.

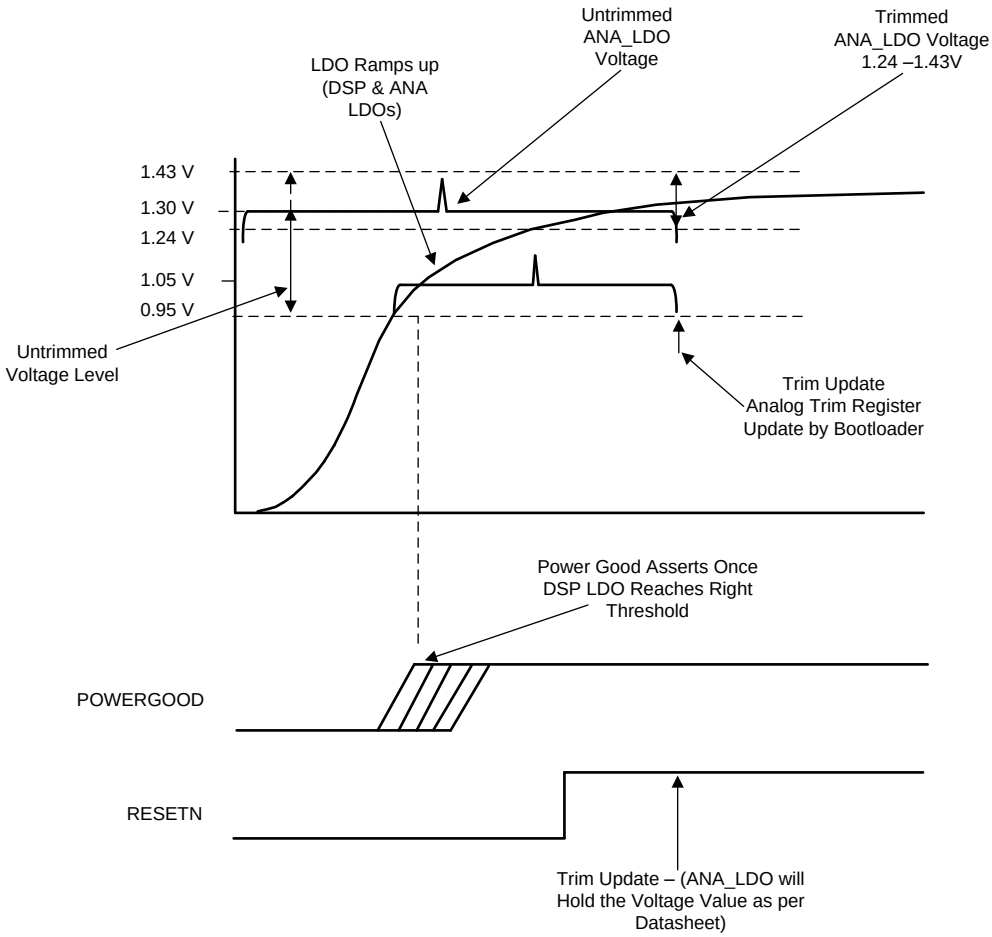


Figure 1. Untrimmed LDO Voltages

2.3 Analog TRIM Register Update

Until the Analog TRIM register is configured, the LDO voltage may not match the voltage specified in the datasheet. The Analog TRIM register is updated by the bootloader (during boot process) and this happens only after the reset is released.

The TRIM register is updated during boot sequence. Following is the boot procedure during which the Analog TRIM register gets updated:

1. Immediately after reset, the CPU fetches the reset vector from 0xFFFF00. MP or MC is 0 by default, so 0xFFFF00 is mapped to internal ROM. The PLL is in bypass mode.
2. Set CLKOUT slew rate control to slow slew rate.
3. Idle all peripherals, MPORT and HWA.
4. If CLK_SEL = 0, the bootloader powers up the PLL and sets its output frequency to 12.288 MHz (with a 375x multiplier using VP = 749, VS = 0, input divider disabled, output divide-by-8 enabled, and output divider enabled with VO = 0). If CLK_SEL = 1, CLKIN pin (approximately 12 MHz) is CLK source and the bootloader keeps the PLL bypassed. Enable Timer0 to count the settling time of BG_CAP. This CLK_SEL is for the C5515 device. For CLK_SEL information on other C55xx devices, see the device-specific data sheet.
5. Apply manufacturing trim to the bandgap references (update analog TRIM registers)
6. Bootloader then polls boot peripherals, copies program code into internal memory from first peripheral with valid boot signature

2.4 DSP LDO When Disabled

The DSP_LDO_EN also affects how reset is generated to the chip. When the DSP_LDO is disabled, the internal power on reset voltage monitor is disabled and the only source of RESET is from the RESET pin.

2.5 Enabling USB LDO

At reset, the USB_LDO is turned off. The USB_LDO can be enabled via the USBLDOEN bit (bit 0) in the LDOCNTL.

Additionally, the USB_LDO is enabled by the USBLDOEN bit of the bootloader if it reaches the USB boot step in the boot sequence.

3 USB Power Up Sequence

If the USB subsystem is used, the subsystem must be powered up in the following sequence.

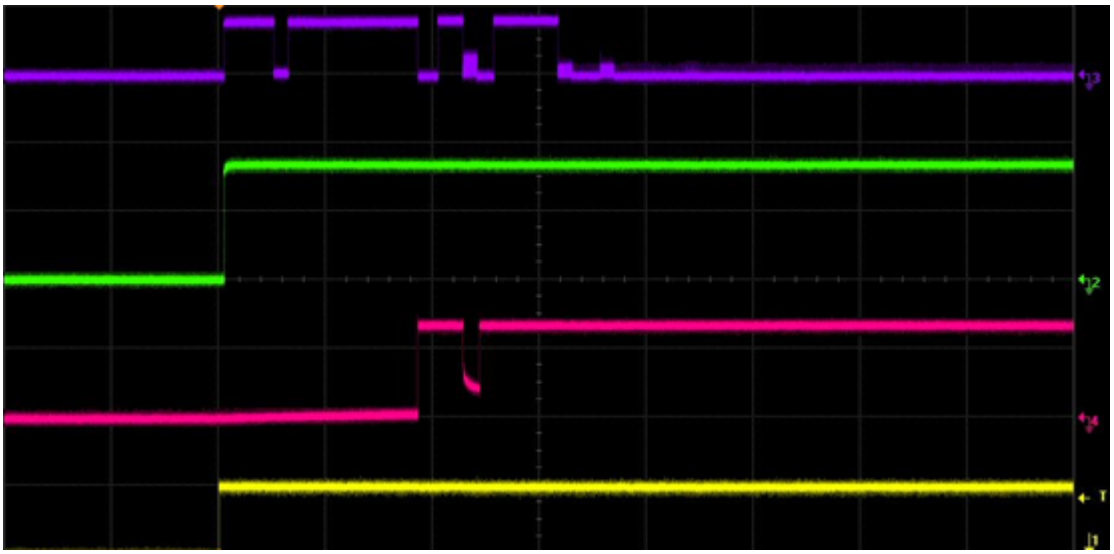
1. USB_VDDA1P3 and USB_VDD1P3
2. USB_VDDA3P3
3. USB_VBUS

To enforce this power up sequence, load switches can be used.

- TPS22913 – is small, low rON load switches with controlled turn on.

3.1 Irregular Short-Term Signal Transition on USB DP/DM Lines

If the proper USB power sequencing procedure is not followed, the DP/DM USB signals might produce an irregular short term signal transition, which in turn may result in failure of enumeration process.



(1) Legend:
- Channel 1 (Yellow): VBUS
- Channel 2 (Green): USB_VDDA3P3
- Channel 3 (Purple): DP/DM
- Channel 4 (Pink): USB_LDO

Figure 2. Irregular Short Term Signal Transition on DP/DM line

As observed in the above figure, VBUS ramps up and then USB_VDDA3P3 ramps up following VBUS. This results in irregular short term signal transition on DP/DM and stops only when USB_LDO ramps up.

The irregular short term signal transition on DP/DM is caused by having a residual voltage on VDDA3P3V without VDD1P3V. Following the correct USB power up sequence, that is powering up VDD1P3V before VDDA3P3V will overcome the above irregular signal transition issue.

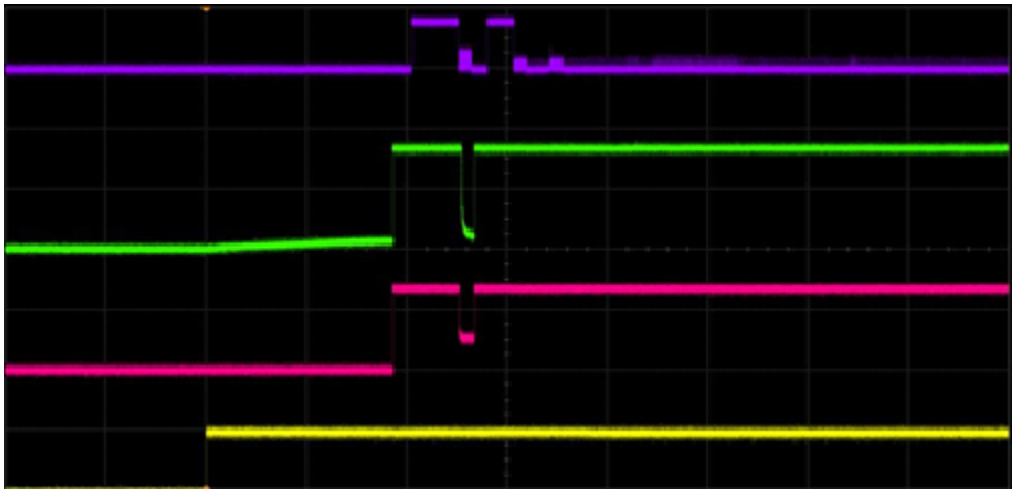
Also, from VBUS to VDDA3P3V there is a weak path through weak resistors. Therefore, if VDDA3P3V is down and VBUS is up, there is a residual voltage on VDDA3P3V supply. Anytime there is a residual voltage on VDDA3P3V without VDD1P3V, results in irregular short term signal transition issue.

If the power sequencing is ignored, and the irregular short term signal transition occurs before the C55x device has completed boot-loading, the USB host will likely time out before software correctly configures the USB module, resulting in a failed USB enumeration.

Additionally, for USB power sequencing - ensure USB VBUS pin does not inadvertently get supplied through any ESD devices. TPD2E001 should be avoided in this case since there is a 3.3 V path from USB_DP to VBUS through the ESD diodes. Instead, use TPD2EUSB30 for DP/DM and TPD1E10B06 for VBUS to break the path from DP to VBUS.

The board designer must not allow USB oscillator or CLK generator to start until after VDDA3P3V is supplied. For example, 12 MHz clock oscillator supplied by VDDA3P3V instead of VDDA3P3V, alternately use 12 MHz crystal between USB_MXO and USB_MXI or use clock oscillator supplied by VDDA3P3V, gated until after VDD1P3V is up.

Figure 3 shows the proper USB power up sequence; here USB_VDDA3P3 is gated by USB_LDO, and ramps up when USB_LDO ramps up, with no irregular short term signal transition observed on DP/DM lines.



(1) Legend:
- Channel 1 (Yellow): VBUS
- Channel 2 (Green): USB_VDDA3P3
- Channel 3 (Purple): DP/DM
- Channel 4 (Pink): USB_LDO

Figure 3. No Irregular Short Term Signal Transition on DP/DM

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