Migrating From TMS320C6416/15/14/11 Rev 1.1 to Rev 2.0

Kimberly Daniel   *Digital Signal Processing Solutions*

ABSTRACT

This application report describes issues of interest related to migration from the TMS320C6416/15/14/11 Rev 1.1 to the TMS320C6416/15/14/11 Rev 2.0 device. The objective of this document is to indicate differences between the two device families. Functions that are identical between the two devices are not included. For detailed information on the specific functions of either device, refer to the *TMS320C6414, TMS320C6415, TMS320C6416 Fixed-Point Digital Signal Processors Data Sheet* (SPRS146), *TMS320C6411 Fixed-Point Digital Signal Processor Data Sheet* (SPRS196), and the *TMS320C6000 Peripherals Overview Reference Guide* (SPRU190).

C6416/15/14/11:

Unless otherwise noted, the information contained in the C6416/15/14/11 data sheet (see section 7, References) should be considered Production Data.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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1   Introduction

The TMS320C6416/15/14/11 rev 2.0 only slightly differs from C6416/15/14/11 rev 1.1. The differences apply solely to device identification and a single External Memory Interface (EMIF) asynchronous timing parameter (ARDY input hold).

To appropriately consider the impact of the change to the asynchronous EMIF ARDY hold timing spec, it is necessary to understand the current interface timings for a given system. A timing analysis of the affected signal should be done to calculate the amount of available margin in the affected interfaces.

Previous workarounds implemented on TMS320C6416/15/14/11 rev 1.1 need not be undone when migrating to TMS320C6416/15/14/11 rev 2.0.

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2 Device Identification

The TMS320C6416/15/14/11 Rev 2.0 devices are new products. The JTAG (BSDL) ID and Silicon Revision ID are different than other TMS320C64x DSP devices.

Table 1 identifies the difference in JTAG (BSDL) ID between the C6416/15/14/11 Rev 1.1 and C6416T/15T/14/11 Rev 2.0. The single difference lies in the value of the variant field.

Table 1. JTAG (BSDL) ID for C6416/15/14/11

Device	JTAG (BSDL) ID			
	Variant	Part Number	Manufacturer	LSB
C6416/15/14/11 Rev 1.1	0010	0000000001110000	00000010111	1
C6416/15/14/11 Rev 2.0	0011	0000000001110000	00000010111	1

Table 2 identifies the Silicon Revision ID differences between the C6416/15/14/11 Rev 1.1 and C6416/15/14/11 Rev 2.0.

Table 2. Silicon Revision ID for C6416/15/14/11

Device	Silicon Revision ID (0x01B00200)
	Revision ID
C6416/15/14/11 Rev 1.1	0010 or 0000
C6416/15/14/11 Rev 2.0	0011

3 IO Timing: EMIF Asynchronous Memory

Table 3 lists the asynchronous timing parameter that changed from C6416/15/14/11 rev 1.1 to 2.0. The input ARDY hold time changed from 1ns to 1.3 ns.

Table 3. Asynchronous Memory Timing Change

No.	Parameter	Rev 1.1 Min	Rev 2.0 Min	Unit
7	th(EKO1H-ARDY) Hold time, ARDY valid after ECLKOUTx high	1	1.3	ns

4 Reference

1. *TMS320C6414, TMS320C6415, TMS320C6416 Fixed-Point Digital Signal Processor Data Sheet* (SPRS146).
2. *TMS320C6411 Fixed-Point Digital Signal Processor Data Sheet* (SPRS196).
3. *TMS320C6000 Peripherals Overview Reference Guide* (SPRU190).

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