Migrating From TMS320C6416/15/14 to TMS320C6416T/15T/14T

Kimberly Daniel

ABSTRACT

This application report describes issues of interest related to migration from the TMS320C6416/15/14 to the TMS320C6416T/15T/14T device. The objective of this document is to indicate differences between the two device families. Functions that are identical between the two devices are not included. For detailed information on the specific functions of either device, see the *TMS320C6414, TMS320C6415, TMS320C6416 Fixed-Point Digital Signal Processors Data Sheet* (SPRS146), the *TMS320C6414T, TMS320C6415T, TMS320C6416T Fixed-Point Digital Signal Processor Data Sheet* (SPRS226), and the *TMS320C6000 DSP Peripherals Overview Reference Guide* (SPRU190).

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1 Introduction

Migration issues from the C6416/15/14 to C6416T/15T/14T are indicated with the following symbols. These symbols are included at the beginning of each section in this document.

- **S** Means software modification is required.
- **H** Means hardware modification is required.
- **D** Means the C6416/15/14 and C6416T/15T/14T devices are different (usually due to added features or enhancements on the C6416T/15T/14T device) but no modification is necessary for migration (i.e., different but compatible).
- **F** Requires further end-use application evaluation

C6416/15/14:

Unless otherwise noted, the information contained in the *TMS320C6414, TMS320C6415, TMS320C6416 Fixed-Point Digital Signal Processors Data Sheet* (SPRS146) should be considered Production Data.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

C6416T/15T/14T:

Unless otherwise noted, the information contained in the *TMS320C6414T, TMS320C6415T, TMS320C6416T Fixed-Point Digital Signal Processor Data Sheet* (SPRS226) should be considered Product Preview.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

2 Core Power [H]

The core voltage of the C6416T/15T/14T is 1.1 V with 5% tolerance (1.2 V with 3% tolerance for high-performance operation); reduced from 1.2 V and 1.4 V, respectively, on the C6416/15/14. In systems where the C6416T/15T/14T replaces the C6416/15/14, the power supply circuit on the board must be modified to support this change. Table 1 shows the relationship between operating voltages, frequencies, and CV_{DD} tolerances supported on the C6416T/15T/14T devices. The DV_{DD} (I/O voltage) is unchanged (3.3 V 5%).

Table 1. Voltages, Frequencies, and CV_{DD} Tolerances on the C6416T/15T/14T Device

CV_{DD}	Tolerance	Maximum Frequency
1.2 V	3%	1 Ghz
1.2 V	3%	720 Mhz
1.1 V	5%	600 Mhz

2.1 Peak Power [F]

Steady-state use cases and conditions relative to power requirements are similar. These differences should be considered during migration power analysis between the two devices and may occur during initial in rush or peak conditions (including, but not limited to power up) depending on the end-use application design.

Key considerations include: power supply selection; transient and bulk capacitance; and end-use application sequencing (DSPs, etc.).

3 Device Identification (ID)

The TMS320C6416T/15T/14T devices are new products. The JTAG (BSDL) ID and Silicon Revision ID are different than other TMS320C64x™ DSP devices.

Table 2 identifies the JTAG (BSDL) ID differences between the C6416/15/14 and C6416T/15T/14T.

Table 2. JTAG (BSDL) ID for C6416T/15T/14T

		JGAG (BSDL) ID		
Device	**Variant**	**Part Number**	**Manufacturer**	**LSB**
C6416T/15T/14T	0000	0000000010000001	00000010111	1
C6416/15/14 (Rev. 1.1)	0010	0000000001110000	00000010111	1

Table 3Table 3 identifies the Silicon Revision ID differences between the C6416/15/14 and C6416T/15T/14T.

Table 3. Silicon Revision ID for C6416T/15T/14T

	Silicon Revision ID (0x01B00200)	
Device	**Turbo ID [20]**	**Revision ID [19:16]**
C6416T/15T/14T	1	0000
C6416/15/14 (Silicon Rev. 1.1)	0	0010

4 Package and Pins [H D]

The physical dimensions and pin out of the package used for C6416T/15T/14T are the same as those on the C6416/15/14. Some modifications can be made to the package that are transparent to you. These changes (e.g., different substrate) may affect the thermal characteristics of the package; see the *TMS320C6414T, TMS320C6415T, TMS320C6416T Fixed-Point Digital Signal Processor Data Sheet* (SPRS226).

4.1 External Terminators [H D]

The C6416T/15T/14T input/output (I/O) buffers have been modified for the new 0.09-µm manufacturing process and have different output impedance than those of the C6416/15/14. For boards designed with the C6416/15/14, termination resistor values need to be recalculated and changed if necessary.

5 PLL/CPU Clock [H]

PLL configuration options on C6416T/15T/14T are the same as were available on C6416/15/14, with the addition of the x20 mode. The PLL can be configured for x20 mode by setting CLKMODE[1:0] to 11b.

For a board using C6416/15/14 with CLKMODE [1:0] set to 10b, using a 50-MHz CLKIN would result in a 600-MHz CPU clock. For the C6416T/15T/14T to maintain a CPU frequency of 600 MHz, no changes to the board are necessary, since the CLKMODE [1:0] pins remain at 10b. With the 50-MHz CLKIN, the x12 PLL mode still results in 600 MHz. To achieve the frequency of 720 MHz, increase CLKIN to 60 MHz. For C6416T/15T/14T to maintain a CPU frequency of 1 GHz, the CLKMODE [1:0] pins must be changed to 11b and a CLKIN of 50 MHz must be provided.

Table 4 shows the changes in PLL modes when transferring from C6416/15/14 to C6416T/15T/14T.

Table 4. Changes in PLL Modes When Transferring From C6416/15/14 to C6416T/15T/14T

PLL MODE	CLKIN (Min.)	CLKIN (Max.)	CPU CLK (Min.)	CPU_CLK (Max.)
		C6416/15/14		
6	30	75	180	450
12	30	60	360	720
		C6416T/15T/14T		
6	42	75	252	450
12	42	75	504	900
20	25	50	500	1000

6 System Reset [D]

There is a minor modification in the reset logic of the C6416T/15T/14T that will cause system reset to extend by approximately 16070 CPU cycles. This delay occurs after the device is powered on, and device reset, $\overline{\text{RESET}}$, goes inactive. The device will not be fully out of reset and initialized until after the 16070P (P=1/CPU) delay, and the *host boot* should not proceed until the 16070P delay has elapsed.

In addition to the previous difference, when the device has been powered up and the PLL is in a stable state, when device reset, $\overline{\text{RESET}}$, goes active it will cause the PLL to reset. This requires that the device reset, $\overline{\text{RESET}}$, be held for 250 µs to give the PLL time to stabilize. This is different than the 6416 where the $\overline{\text{RESET}}$ pulse needed to be only 10P (P=1/CPU) since the PLL was already stable and not reset by the device reset going active.

These two items result in the compatibility of the C6416T/15T/14T relative to 6416/15/14 during and a relatively short time after reset is not 100%.

Note: Cycle compatibility after the 16070 cycles is 100%.

7 I/O Timing [D S]

The C6416T/15T/14T has the same AC characteristics for I/O timings as the timings of the C6416/15/14 (600 MHz and below). When the CPU/X option is used for peripheral clocking, the relative timing to the reference remains the same, but the absolute timing of the I/O could be impacted. This requires reconfiguring the peripheral registers for controlling the timing parameters, depending upon the system requirement. Therefore, overall timing can be recalculated to adjust the cycle-time difference by using the C6416/15/14 and C6416T/15T/14T data sheets (see Section 10, References). The CPU/X option is used for peripheral clocking on the following peripherals: timers, multichannel buffered serial ports (McBSPs), and external memory interface (EMIF).

Note: For keeping 600 MHz, there is no change required.

7.1 EMIF

You should verify the EMIF timings per -6E3, as specified in the C6416/15/14 and C6416T/15T/14T data sheets (see Section 10, References).

Assuming that the C6416T/15T/14T is running at 720 MHz and EMIF at CPU/6 = 120 MHz, be aware that input/output setup times will change based on EMIF going from a 100-MHz to 120-MHz interface. Input/output hold times will remain the same. As -6E3 timings are ensured up to 133 MHz, you should not have a problem meeting timing at 120 MHz.

If the C6416T/15T/14T is running at 1 GHz, an external clock must be provided to the EMIF on ECLKIN. This is because when operating at 1 GHz and the EMIF at CPU/6 = 166.6 MHz, the maximum frequency of the EMIF, which is 133 MHz, will be violated.

8 Sequencing [F]

Given the variety of end-use application designs, unknown end-use design configurations, or unknown end-use conditions, the core should be sequenced before the I/O supply rail. Sequence timing between the core (V_{good}) and I/O (V_{good}) should be ≤ 200 ms. If the I/O (V_{good}) is sequenced before the core (V_{good}) it must occur ≤ 50 ms.

9 Notes

The end use of each DSP application is different to some degree; therefore, Texas Instruments cannot control the quality or implementation of each application design beyond the DSP processor referenced in this document. Because of the variation in application designs, proper engineering and due diligence is always recommended when substituting devices or designing new applications. Good design principals that take into account multi-DSP requirements, power sequencing, source and sync power requirements, and dynamic noise should always be evaluated regardless of change.

10 References

- *TMS320C6414, TMS320C6415, TMS320C6416 Fixed-Point Digital Signal Processors Data Sheet* (SPRS146)
- *TMS320C6414T, TMS320C6415T, TMS320C6416T Fixed-Point Digital Signal Processor Data Sheet* (SPRS226)
- *TMS320C6000 DSP Peripherals Overview Reference Guide* (SPRU190)
- *TMS320C6000 Peripherals Reference Guide – Manual Update Sheet for SPRU190D* (SPRZ122)

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