TEXAS INSTRUMENTS

Application Report
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TMS320C6472/TMS320TCI6486 DDR2 Implementation Guidelines

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ABSTRACT

This application report contains implementation instructions for the DDR2 interface contained on the TMS320C6472/TMS320TCI6486 DSP devices. The approach to specifying interface timing for the DDR2 interface is quite different than on previous devices.

The previous approach specified device timing in terms of data sheet specifications and simulation models. The customer was required to obtain compatible memory devices, as well as their data sheets and simulation models. The customer would then take this information and design their printed circuit board (PCB) using high speed simulation to close system timing.

For the C6472/TCI6486 DDR2 interface, the approach is to specify compatible DDR2 devices and provide the PCB routing rule solution directly to the customer. TI has performed the simulation and system design work to ensure DDR2 interface timings are met. The DDR2 system solution is referred to as the C6472/TCI6486 DDR2 collateral. This document describes the content of this collateral.

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1 Prerequisites

1.1 High Speed Design

While the goal of the C6472/TCI6486 collateral is to make system implementation easier for the customer by providing the system solution, it is still expected that the PCB design work is to be supervised by a knowledgeable high-speed PCB designer as an assumption is made that the PCB designer is using established high-speed design rules. Ground plane cuts should be avoided, if at all possible, as they are tricky to do correctly. Due to PCB design, crosstalk and EMI impacts should be evaluated as the PCB design progresses because it can be difficult to go back and fix issues later. Thorough planning aids in the design cycle.

1.2 Familiarity With the JEDEC DDR2 Specification

The DDR2 interface on the C6472/TCI6486 device is designed to be compatible with the JEDEC JESD79-2B DDR2 specification. It is assumed that the reader is familiar with this specification and the basic electrical operation of the interface. In addition, several memory manufacturers provide detailed application reports on DDR2 operation.

2 Compatible JEDEC DDR2 Devices

Table 1 shows the parameters of the JEDEC DDR2 devices that are compatible with this interface. Generally, the DDR2 interface is compatible with all x16 DDR2-533 speed grade DDR2 devices and most x8 DDR2-533 speed grade DDR2 devices. When implementing four x8 devices to achieve a 32-bit memory solution, the maximum clock frequency is reduced to 250 MHz for DDR2-500 operation.

Table 1. Compatible JEDEC DDR2 Device Parameters

No.	Parameter	Min	Max	Unit	Notes
1	JEDEC DDR2 Device Speed Grade	DDR2-533			See Note [1]
2	JEDEC DDR2 Device Bit Width	x8	x16	Bits	
3	JEDEC DDR2 Device Count	1	4	Devices	See Note [2]
4	JEDEC DDR2 Device Ball Count	60	92	Balls	See Note [3]
5	JEDEC DDR2 Device Size	256M	2G	Bits	See Note [4]

(1) Higher DDR2 speed grades are supported due to inherent JEDEC DDR2 backwards compatibility.
(2) One x16 DDR2 device is used for a 16-bit DDR2 memory system and two x16 DDR2 devices are used for a 32-bit DDR2 memory system. Similarly, two x8 DDR2 devices are used for a 16-bit DDR2 memory system and four x8 DDR2 devices are used for a 32-bit DDR2 memory system. In all cases, the DQ connections are point-to-point.
(3) 92-ball devices retained for legacy support. New designs will migrate to 84-ball x16 DDR2 devices and 60-ball x8 DDR2 devices. Electrically, the older and newer DDR2 devices are the same.
(4) 2Gb devices can be used in x16 width. 1Gb is the largest device used in x8 width.

TI is working with specific DDR2 manufacturers/devices. The following JEDEC DDR2 compatible devices are recommended:

- MT47H128M16HG-37E - Micron 2Gb DDR2-533 84 ball package
- MT47H64M16BT-37E - Micron 1Gb DDR2-533 92 ball package
- MT47H32M16BT-37E - Micron 512Mb DDR2-533 92 ball package
- MT47H32M16CC-37E - Micron 512Mb DDR2-533 84 ball package
- MT47H16M16BG-37E - Micron 256Mb DDR2-533 84 ball package
- EDE5116ABSE-5C-E - Elpida 512Mb DDR2-533 84 ball package
- EDE5116AFSE-5C-E - Elpida 512Mb DDR2-533 84 ball package
- EDE2516ABSE-5C-E - Elpida 256Mb DDR2-533 84 ball package

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2.1 JEDEC DDR2 84-Ball Versus 92-Ball Packages

The 84- and 92-ball DDR2 BGA packages are electrically compatible. The additional 8 balls on the 92-ball package are support balls only. The provided DDR2 layout allows room for these support balls.

2.2 DDR2 Package Size Warning

Use caution when determining the DDR2 component keep out, as the JEDEC specification generally calls out only maximums for package sizing. Some manufacturers' JEDEC-compliant DDR2 parts are narrower than these maximums. This can cause assembly interference issues if the part is later changed to another manufacturer with a wider package width. It is best to follow MO-207J and the manufacturer's documentation to determine overall package sizing. Pay close attention to the limits allowed by MO-207J, as these will likely be more restrictive than a specific manufacturer's part specification. This allows physical placement compatibility with all JEDEC DDR2 parts supported by this device.

3 Related Documentation

The *Flip Chip Ball Grid Array Package Reference Guide* (SPRU811) provides guidance with respect to PCB design and Texas Instruments BGA packages. It contains PCB design rules, PCB assembly parameters, rework process, thermal management, troubleshooting tips, plus other critical information.

JEDEC specification JEDSD-79A contains the JEDEC DDR2 specification. JEDEC specification MO-207J contains package drawings for JEDEC DDR2 devices.

Specific examples of the implementation of this specification including schematics and a PCB layout can be obtained from the C6472/TCI6486 EVM documentation. In addition, the interested reader may refer to the *High-Speed DSP Systems Design Reference Guide* (SPRU889).

For configuration of the DDR interface, see the *TMS320C6472/TMS320TCI648x DSP DDR2 Memory Controller User's Guide* (SPRU894).

4 Schematics and Electrical Connections

Figure 1 shows a high-level schematic of the DDR2 interface when using x16 devices. Specific pin numbers can be obtained from the *TMS320TCI6486 Communications Infrastructure Digital Signal Processor* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612) and the JEDEC DDR2 data sheet. The 32-bit DDR2 interface of the C6472/TCI6486 device is connected to two 16-bit DDR2 devices, thus the clock, address, and control connections are three-point nets and the data lines are point-to-point nets.

Figure 2 shows a high-level schematic of the DDR2 interface when using x8 devices. The 32-bit DDR2 interface of the C6472/TCI6486 device is connected to four 16-bit DDR2 devices, thus the clock, address, and control connections are five-point nets and the data lines are point-to-point nets.

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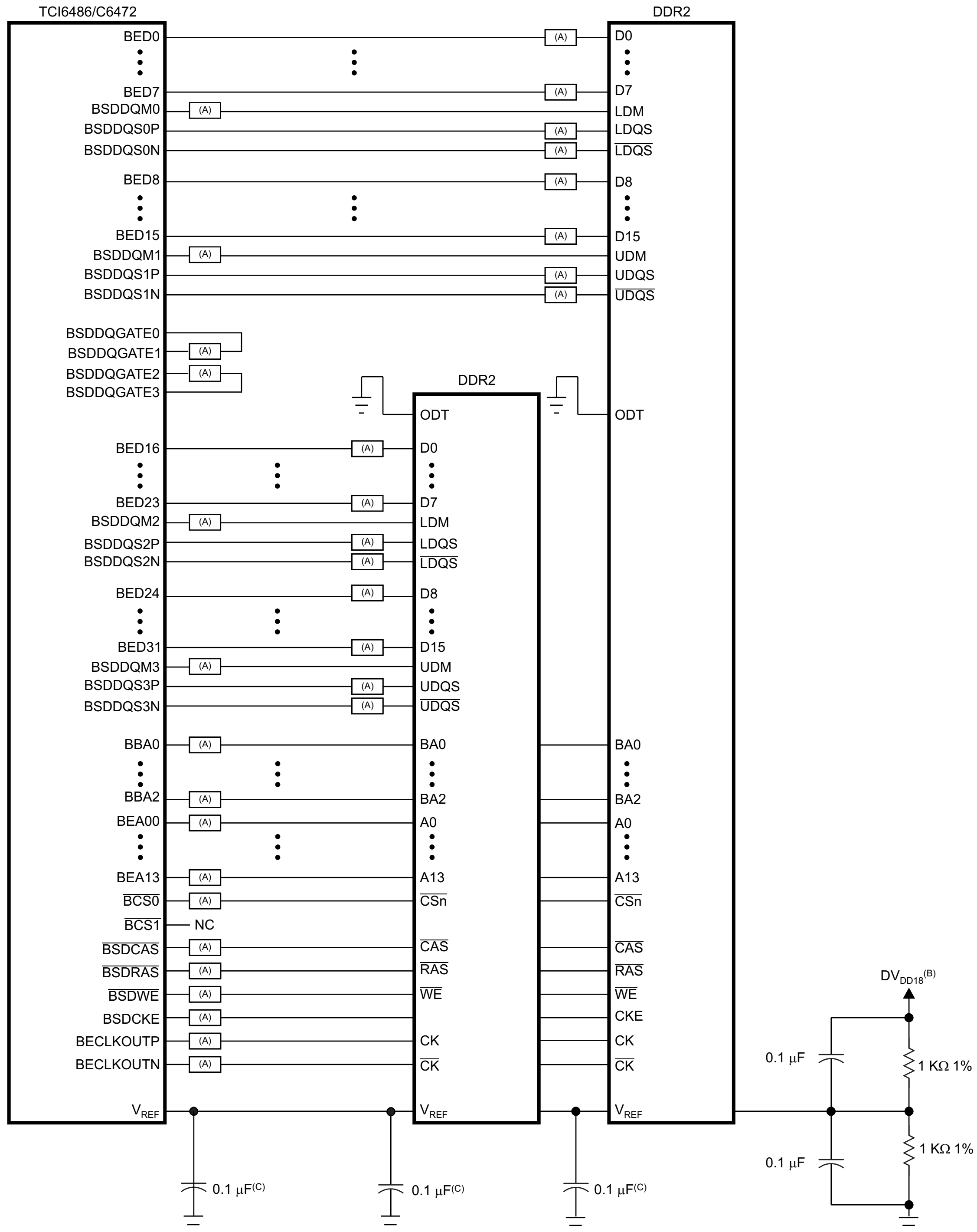
Figure 1. C6472/TCI6486 DDR2 High-Level Schematic - x16 Devices



A Terminator, if desired. See terminator comments.

B DV_{DD18} is the V_{REF} power supply for the DDR2 memories and DSP DDR2 interface.

C One of these capacitors can be eliminated if the divider and its capacitors are placed near a device pin.

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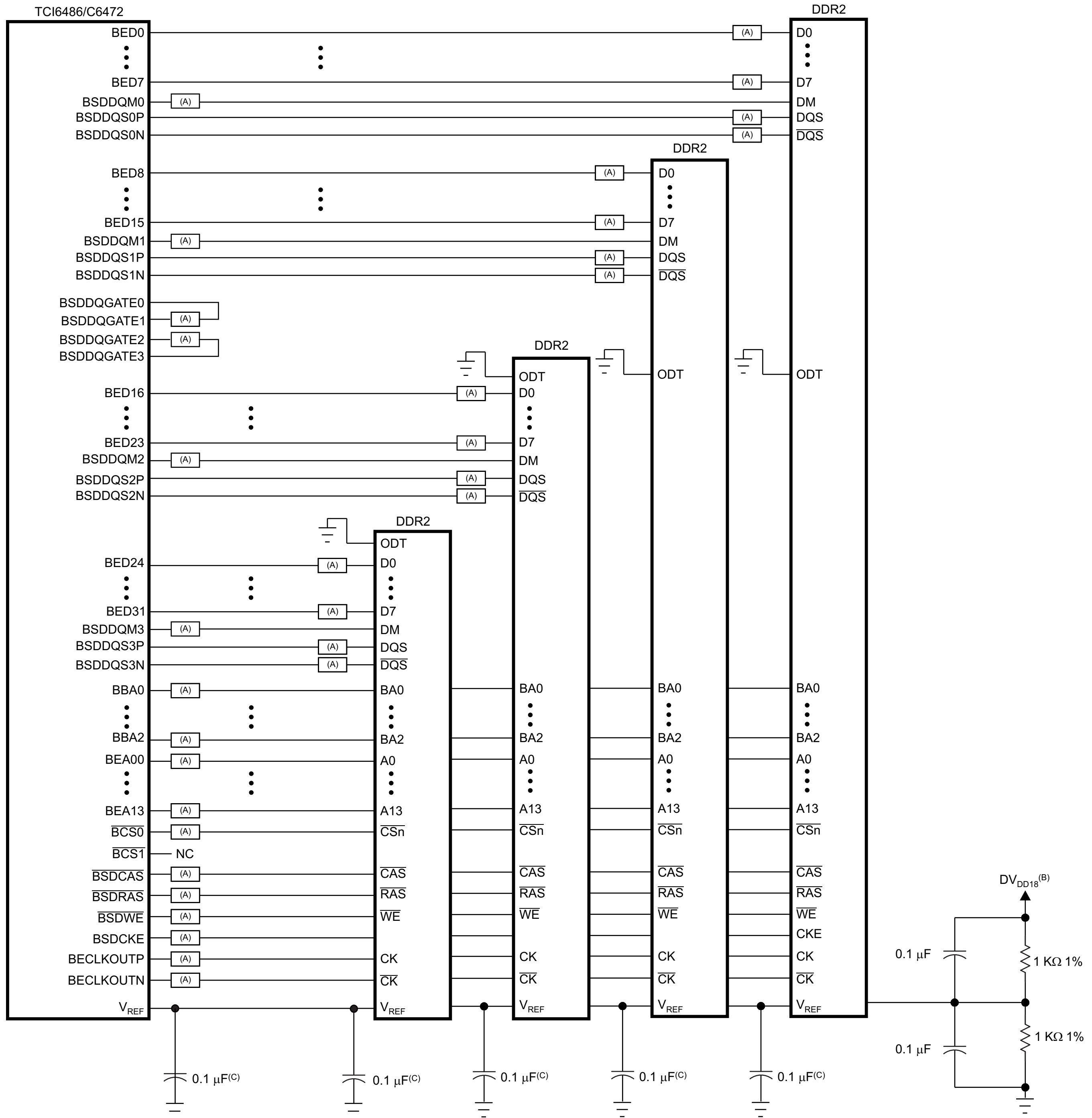
Figure 2. C6472/TCI6486 DDR2 High-Level Schematic - x8 Devices



A Terminator, if desired. See terminator comments.

B DV_{DD18} is the V_{REF} power supply for the DDR2 memories and DSP DDR2 interface.

C One of these capacitors can be eliminated if the divider and its capacitors are placed near a device pin.

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4.1 Differences Between the C6472/TCI6486 DDR2 Interface and the Typical PC Application

There are some subtle differences between the embedded DDR2 application used on the C6472/TCI6486 device and the typical PC motherboard/DDR2 DIMM application. The C6472/TCI6486 DDR2 interface does not use stub-series termination (the SST in SSTL). Stub-series terminators are parallel terminators and they are not used in this case due to their high power consumption. Consequently, the termination voltage, V_{tt}, is also not used nor is it required for the C6472/TCI6486 DDR2 interface. The terminators shown in Figure 1 and Figure 2 are series-resistor terminators.

4.2 DDR2 Power Supplies

The power supply for the DDR2 interface is 1.8 V ±5%. This power supply is used for the C6472/TCI6486 DDR2 power pins (DV_{DD18}) as well as the JEDEC DDR2 devices. V_{REF} is derived from the DDR2 power supply via a resistive divider.

4.3 Signal Terminations

It is strongly recommended that all DDR2 memory implementations with the C6472/TCI6486 contain series termination resistors. Series terminations on the PCB allow the DDR2 signals to be tuned to meet EMI certification requirements, control overshoot, and limit crosstalk. A PCB that fails EMI certification without series terminations likely has to be re-spun in order to address the EMI shortcomings. It can take multiple PCB spins to correct EMI issues. Note that re-spinning a dense, non-terminated PCB layout to include terminators can be a very difficult effort because physical room must be made for the terminations. This means an entire PCB design may have to be redone. It is much easier to remove terminations rather than adding them after the PCB has been found to fail EMI.

Customers who are sensitive to the cost/schedule issues with respect to EMI may wish to include terminations on their boards even though they plan not to have terminations on the final product. This way, the terminations can easily be replaced with zero-Ω resistors and checked for EMI compliance. If the PCB fails EMI, it is then possible to install the necessary terminations without re-spinning the PCB. Once the termination scheme has been verified to pass EMI, the remaining zero-Ω terminations can be carefully removed from the PCB layout in a single PCB design spin.

Operation has been validated with series termination resistors through both simulation and board implementations. This has been done with the DDR2 memory configured for 100% drive strength. Operation without series termination resistors requires that the DDR2 memory be configured for 60% drive strength to meet the overshoot specification in many implementations.

Parallel termination is not supported by the DDR2 interface on the C6472/TCI6486 due to the increased power consumption.

4.4 PTV Compensated Output Impedance

In order to meet the signal integrity and AC timing needs of a DDR2 interface, the C6472/TCI6486 DDR2 I/O buffers dynamically compensate for process, temperature, and voltage (PTV) to hold a constant output impedance. The output impedance is set by the PTV18 resistors that are connected from the PTV18P pin to GND and the PTV18N pin to DV_{DD18}. These resistors should be 200-Ω 1% resistors.

5 Stackup

A stackup for a 16-layer board is shown in Table 2. This stackup was used on a development board for the C6472/TCI6486 device. It contains several signal routing layers, since all of the peripheral interfaces were implemented. Similarly, this required all I/O power inputs to be supplied as well. The number of layers could be reduced by spreading the DDR2 memories further from the C6472/TCI6486 DSP, thus reducing routing congestion. However, for a relatively dense packing of DSPs with their memories in a DSP farm arrangement, a stackup similar to the one below is expected to be needed.

A PCB with a single-ended controlled impedance with a nominal value between 50 Ω and 60 Ω is acceptable for the DDR2 interface. DDR2 trace impedance should be controlled to within 10 Ω. Board designs utilizing the SRIO interface must also have the target PCB impedance optimized for the differential impedance required by that interface as well.

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Table 2. Board Stackup

	Use	Description	Thickness
Layer 1	Signal	Pin Escapes, Non critical routes	2.1
FR4			6.5
Layer 2	Power	Core power plane	1.4
FR4			3
Layer 3	GND	Solid ground plane	1.4
FR4			6.5
Layer 4	Signal	Critical routing	0.7
FR4			6.5
Layer 5	GND	Solid ground plane	1.4
FR4			6.5
Layer 6	Signal	Critical routing	0.7
FR4			6.5
Layer 7	Power	I/O Power Planes	1.4
FR4			4
Layer 8	Signal	Vertical signal routing	0.7
FR4			3
Layer 9	Signal	Horizontal signal routing	0.7
FR4			4
Layer 10	Power	I/O Power Planes	1.4
FR4			6.5
Layer 11	Signal	Critical routing	0.7
FR4			6.5
Layer 12	GND	Solid ground plane	1.4
FR4			6.5
Layer 13	Signal	Critical routing	0.7
FR4			6.5
Layer 14	GND	Solid ground plane	1.4
FR4			3
Layer 15	Power	Core power plane	1.4
FR4			6.5
Layer 16	Signal	Pin escape breakout, Non critical routes	2.1
		Total	**101.6**

Trace characteristics:

- Copper is 1 oz. on plane layers and 0.5 oz. on trace layers.
- Characteristic impedance of layers 1 and 16: 50 Ω ±10% at 10 mils wide.
- Characteristic impedance of layers 4, 6, 11, and 13: 50 Ω ±10% at 4.5 mils wide.
- Characteristic impedance of layers 8 and 9: 50 Ω ±10% at 4 mils wide.
- Differential impedance of layers 4, 6, 11, and 13: 100 Ω ±10% at 4 mil track with 6 mil spacing.

Note that the surface layers (1 and 16) do not have ground reference layers. DDR2 routing on these layers is not permissible beyond very short traces between pads and vias. If DDR2 routing is required on the surface layers, a ground "island" will be needed on the adjacent layers. This ground island will need sufficient vias connecting it to the internal ground planes. These vias should be connected to DVDD18 decoupling capacitors.

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5.1 Ground Reference Planes

It is critical that all signal routing layers have a solid ground reference plane adjacent to all DDR2 signal routes; meaning that there is a full, contiguous ground plane next to every DDR2 routing layer. Two routing layers can share a ground plane (one signal layer above and one signal layer below the ground plane). Ground-plane cuts are not allowed in the DDR2 region. (Ground-plane cuts are generally a bad idea that should only be done very carefully and if absolutely necessary on other areas of the PCB.) The purpose of the ground plane is to provide a path for return currents to minimize crosstalk and EMI. Power planes cannot be used as signal returns for the DDR2 interface. *Improper ground-plane stackup will likely cause the DDR2 interface to fail or operate unreliably.*

5.2 Stackup Routing Impacts

The internal routing planes (stripline) have different flight times than top/bottom (microstrip) routing planes. Ideally, the trace routes within the same net class (covered in detail in Section 7.3.1) should either all be microstrip or stripline so that trace length matching can be done. If a combination of microstrip and stripline is used within a net class, the trace length should be adjusted to offset the delay difference. The trace flight times for microstrip and stripline should be determined for the specific board stackup being used.

6 Placement

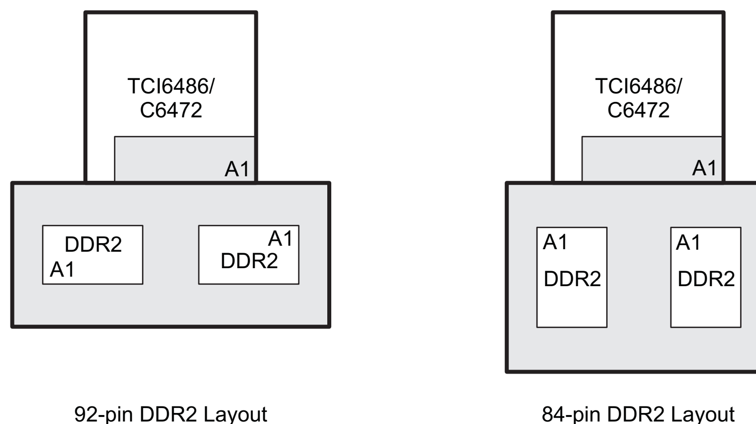
6.1 Minimizing PCB Area

The maximum placement area and minimum PCB stackup uses the lowest cost PCB technology and generally results in the lowest unit cost PCB at the penalty of the largest footprint for the DDR2 interface. Customers need to evaluate the cost/benefit tradeoffs of smaller feature sizes and additional signal layers for their systems. Note that the minimum feature size and stackup may be limited by other circuitry on the PCB.

6.2 DDR2 Placement and Keep Out Region

Figure 3 shows example DDR2 placements with keep-out regions shaded. The keep-out region will vary with the individual design. Its purpose is to ensure other signals do not interfere with the DDR2 interface. The only signals allowed in this region on the DDR2 signal layers are those for this interface. The 1.8-V DV_{DD18} plane and the reference ground planes must encompass at least the entire DDR2 keep-out region. Non-DDR2 signals can be routed in this region provided they are routed on layers separated from DDR2 signal layers by a solid ground plane. No breaks are allowed in the reference ground layers in this region.

Figure 3. DDR2 Placement and Keep Out



The placements shown in Figure 3 work well when implementing either a pair of x16 or x8 memory devices on the same side of the PCB as the C6472/TCI6486. When implementing four of the x8 devices, two may be placed on the top in the above orientation and two directly underneath on the bottom to meet the trace length requirements. There may be other solutions.

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6.3 Resistors and Resistor Packs

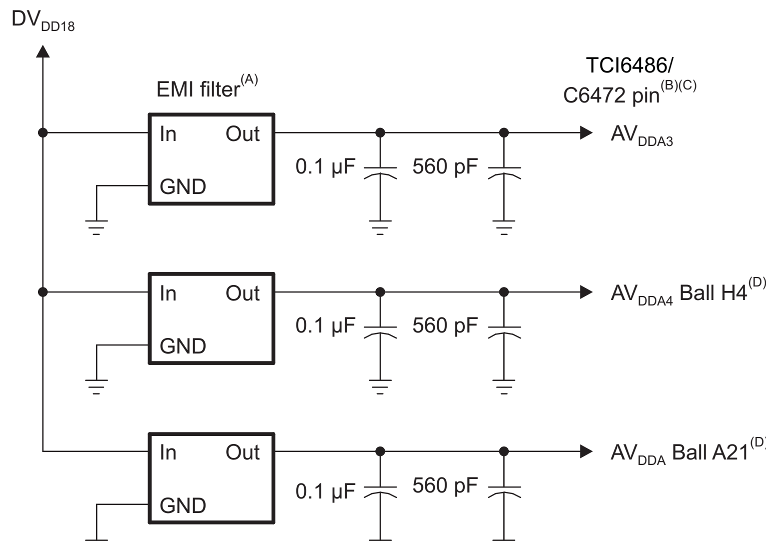
The C6472/TCI6486 DDR2 interface uses resistors for V_{REF} generation and can use resistors or resistor packs for signal terminations. Specific placement requirements for these components are specified by the routing rules for V_{REF} and the other net classes of the interface. These routing rules are presented in Section 7.2.

Generally speaking, termination resistors can be either discrete resistors or resistor packs and they are placed between the DDR2 memories and the C6472/TCI6486 device. The V_{REF} divider resistors are placed somewhere between the DDR2 devices and the C6472/TCI6486 device.

6.4 PLL and DLL Filters

The PLL and DLL power supply pins on the C6472/TCI6486 device draw small currents, but they are noise sensitive. All the PLL and DLL power supplies are derived from the DV_{DD18} supply. Each supply filters the DV_{DD18} using a filter circuit and two capacitors. Figure 4 shows the placement and routing rules for the PLL and DLL power supplies. The filter capacitors are 0402 in physical size.

Figure 4. PLL and DLL Filters Requirements



A The center of EMI filter component should be placed no more than 350 mils from the associated C6472/TCI6486 ball.

B Capacitors shown in this figure should be placed between the EMI filter and the C6472/TCI6486 ball.

C Traces for the nets in this figure should be 15 mils wide, minimum. Necking down for BGA fanout is acceptable.

D The two AV_{DDA4} power inputs can be fed from a single filtered power source if copper track can be routed directly with sufficient isolation.

6.5 Decoupling Capacitors

Decoupling capacitors are critical to the reliable operation of a high-speed PCB. Great care should be taken to ensure these guidelines are followed. Failure to follow these guidelines will likely result in an unstable system.

For details on the overall quantity and type of decoupling and bulk capacitors refer to the *TMS320C6472/TMS320TCI6486 Hardware Design Guide* (SPRAAQ4). The small decoupling capacitors should be 0402 size or smaller.

Exact placement of capacitors is not critical. Decoupling capacitors should be placed near the device being decoupled. Distance from the capacitor to the power pins being decoupled should not exceed 125 mils.

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Each decoupling capacitor requires two vias, one for each pin. Via sharing for decoupling capacitors is not permitted. This is due to the inductance of the vias. Via sharing seriously compromises the performance of the decoupling capacitor due to this inductance. For the same reason, sharing of vias by power and ground pins of the C6472/TCI6486 or DDR2 devices is also not permitted. Vias used for decoupling capacitor and device power connections are referred to as power vias.

To minimize inductance, power vias should be as large as possible. Use care to ensure power vias are not so large as to inadvertently cut planes. Power vias should be connected to the device pads with the shortest possible traces that are as wide as possible. Ideally, the trace length from the power via to the device pad should not exceed 30 mils. Maximum trace length from power via to decoupling capacitor is 60 mils. Maximum trace length from power via to power ball pad is 35 mils.

6.6 DDR2 Signal Terminations

Series terminations are required if the DDR device is operated at 100% strength. The combination of series terminations and 100% drive strength can provide operation up to 267 MHz. Termination is not required to meet reflection and overshoot specifications provided the DDR2 device is operated at 60% strength.

Recommended terminations are shown in Table 3. Termination values may have to be adjusted once hardware is available to pass EMI regulations.

Table 3. DDR2 Signal Terminations

Net Class	Termination
CK	22-Ω series resistor/resistor packs located near DSP
ADDR_CTRL	22-Ω series resistor/resistor packs located near DSP
DQB0 (BED0-BED7)	22-Ω series resistor/resistor packs located near DDR2
DQB0 (BSDDQM0)	22-Ω series resistor/resistor packs located near the C6472/TCI6486 device
DQSB0	22-Ω series resistor/resistor packs located near DDR2
DQB1 (BED8-BED15)	22-Ω series resistor/resistor packs located near DDR2
DQB1 (BSDDQM1)	22-Ω series resistor/resistor packs located near the C6472/TCI6486 device
DQSB1	22-Ω series resistor/resistor packs located near DDR2
DQB2 (BED16-BED23)	22-Ω series resistor/resistor packs located near DDR2
DQB2 (BSDDQM2)	22-Ω series resistor/resistor packs located near the C6472/TCI6486 device
DQSB2	22-Ω series resistor/resistor packs located near DDR2
DQB3 (BED24-BED31)	22-Ω series resistor/resistor packs located near DDR2
DQB3 (BSDDQM3)	22-Ω series resistor/resistor packs located near the C6472/TCI6486 device
DQSB3	22-Ω series resistor/resistor packs located near DDR2
DQGATEL	22-Ω series resistor/resistor packs located near BSDDQGATE1
DQGATEH	22-Ω series resistor/resistor packs located near BSDDQGATE2

7 Routing

7.1 Required PCB Feature Sizes

The minimum PCB feature sizes referenced in this document are the largest that can be accommodated in order to physically route the PCB due to the size of the BGA packages. Maximum PCB trace width/space for BGA escape is 4 mils. Dog-bone BGA escape requires via sizes on the order of 8-mil holes with 18-mil pads, if conventional vias are used. Smaller feature sizes can also be used as well to improve PCB density as long as all routing rules are followed. The minimum PCB trace width and trace spacing is used throughout this document as a unit of measure to determine spacing between groups of tracks that may experience impairments caused by signal crosstalk. It is referred to as the length w.

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It is also a good idea to maximize the size of the vias used for bypass capacitors and power pins. This is done to minimize via inductance. It is the via and bypass capacitor stray inductance that limits the performance of the bypass capacitors. Use care to ensure that vias are not sized so large as to cut off a portion of a plane.

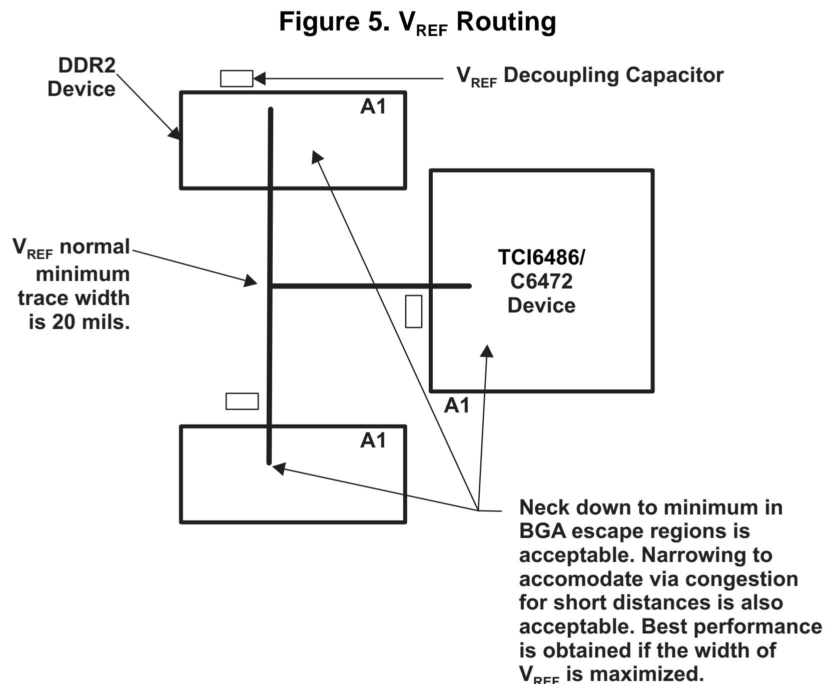
PCB BGA feature size selection is critical for PCB yield and reliability. Generally, it is best if the pad on the PCB has the same area as the pad on the BGA package. Before layout begins, the device manufacturer, PCB fabricator, and PCB assembler should be consulted with respect to BGA pad stacks and other critical BGA PCB mechanical details. As a general warning, the recommended BGA pad size is generally *not* equal to the BGA ball size.

The PCB BGA pad requirements for the C6472/TCI6486 device are documented by the *Flip Chip Ball Grid Array Package Reference Guide* (SPRU811), available at www.ti.com. The C6472/TCI6486 device is a 0.8-mm ball pitch part and should follow the 0.8-mm guidelines. The PCB BGA pad requirements for the DDR2 device should follow its manufacturer's guidelines.

7.2 V_{REF}

V_{REF} is used by the input buffers of the DDR2 memories as well as C6472/TCI6486's DDR2 interface to determine logic levels. V_{REF} is specified to be one-half the power supply voltage and is created using a voltage divider constructed from two 1K Ω, 1% tolerance resistors (see Figure 1). V_{REF} is not a high-current supply, but it is important to keep it as quiet as possible with minimal inductance. The minimum nominal trace width for V_{REF} is 20 mils. There should also be a 20-mil separation from V_{REF} and all adjacent traces. Necking down V_{REF} to accommodate BGA escape and localized via congestion is acceptable, but care should be taken to keep V_{REF} 20 mils wide as much as possible. V_{REF} is a DC net and as such, trace delay is not critical, however, overall trace length should be kept to a minimum. The four or five decoupling capacitors on the V_{REF} net are intended to reduce AC noise. Two are used at the divider, and one each is used near the V_{REF} input of the three loads (2 DDR2s and the C6472/TCI6486 device) (see Figure 5).

Figure 5. V_{REF} Routing



7.3 DDR2 Routing

This section describes the specific guidelines for placement used to drive the trace routes used in DDR2 simulations. This placement assumes logic analyzer connectors in order to analyze what is considered a worst-case implementation. The customer's DDR2 topology should be the same or better (shorter, fewer vias) than this topology.

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The trace lengths and number of vias used in simulations are given in Table 6. The last column gives the range of length matching. The AC timing analysis assumed the worst-case matching. Not included in this table is a 0.2-in. stub on each trace to account for the connection to a logic analyzer pad.

7.3.1 Net Classes

The routing rules for the C6472/TCI6486 DDR2 system design are divided among net classes. Each net class contains all the signals within a clock domain. There are five clock domains: CK, DQS0, DQS1, DQS2, and DQS3. The general requirement is to skew match within a domain and to minimize crosstalk. Crosstalk across domains is especially troublesome and steps should be taken to minimize coupling between signals in different domains.

7.3.1.1 Clock Domain Net Classes

Net classes are used to associate the assorted groups of nets in the DDR2 interface with their clock domain. These net classes are used in the DDR2 routing rules. The DDR2 interface has five clock domains, four of which are bi-directional. The clock domain net classes are shown in Table 4.

All of the clock signals in the C6472/TCI6486 DDR2 interface are differential signals. Each clock domain net class needs to be routed as a differential signal pair with matched lengths for the non-inverting and inverting signals. Differential impedance must also be controlled at 100 Ω.

Table 4. Clock Domain Net Classes

Clock Net Class	Description	DSP Pin Names
CK	DDR2 Interface Clock	BECLKOUTP, BECLKOUTN
DQSB0	DQS for byte 0	BSDDQS0P, BSDDQS0N
DQSB1	DQS for byte 1	BSDDQS1P, BSDDQS1N
DQSB2	DQS for byte 2	BSDDQS2P, BSDDQS2N
DQSB3	DQS for byte 3	BSDDQS3P, BSDDQS3N

7.3.1.2 Signal Net Classes

Table 5 shows the seven additional net classes that use the clock net classes as their reference. Generally speaking, the nets within a net class and their associated clock domain should be skew matched to each other. The goal is to minimize the skew within each clock domain and crosstalk between signals – especially between signals of differing clock domains.

Table 5. Signal Net Classes

Net Class	Clock Domain	Description	DSP Pin Names
ADDR_CTRL	CK	Bank Address, Address, Control	BBA0-BBA2, BEA00-BEA13, $\overline{\text{BSDCAS}}$, $\overline{\text{BSDRAS}}$, $\overline{\text{BSDWE}}$, BSDCKE
DQB0	DQSB0	DQs for byte 0	BED00-BED07, BSDDQM0
DQB1	DQSB1	DQs for byte 1	BED08-BED15, BSDDQM1
DQB2	DQSB2	DQs for byte 2	BED16-BED23, BSDDQM2
DQB3	DQSB3	DQs for byte 3	BED24-BED31, BSDDQM3
DQGATEL	CK, DQSB0-1	DQ gate timing loop for lower word	BSDDQGATE0, BSDDQGATE1
DQGATEH	CK, DQSB2-3	DQ gate timing loop for upper word	BSDDQGATE2, BSDDQGATE3

7.3.1.3 A Word About Trace Separation and BGA Escapes

The net class routing rules in the next section give minimum trace separation requirements for the respective net class. It is understood that in the region near the BGA devices, the traces have to be routed very close together, often at minimum trace separation. Minimum separation routing should be kept to a minimum and the total minimum separation routed length should not exceed 500 mils for each net.

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7.4 Net Class Routing Rules

7.4.1 Routing Rules Overview

In order to define the routing rules, a worst-case placement is used. Trace routes are created based on this. Comprehensive simulations and timing analysis are done to guarantee timing is met for these conditions. As long as the actual placement and routing are the same, or better than, these rules, the signal integrity and timing requirements are met.

The assumed placement is shown in Figure 6 and includes connections for logic analyzer headers. The stubs for the logic analyzer pads can be no more than 0.2 inches. The rest of the maximum routing rules derived from this placement and included in the analysis are described in Table 6 and in the following sections. This layout, with logic analyzer pads, is only recommended when implementing two memory devices.

Figure 6. Worst-Case Placement Reference

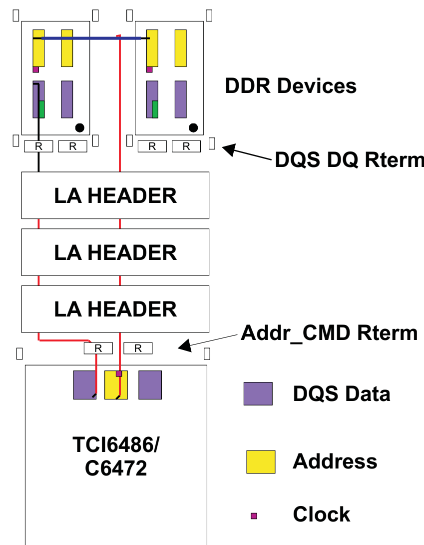

Table 6. Summary of Routing Guidelines

Net Class	Series Resistor Location (Near)	Maximum No. of Vias	Maximum Length	Maximum Allowable Length Mismatch
CK(1)	DSP	5	3.1 inches	Each pair matched within 10 mils
ADDR_CTRL(1)	DSP	5	3.1 inches	± 100 mils relative to CK
DQSBn	Memory Device	5	2.5 inches	± 10 mils within a pair
DQBn (BEDn)	Memory Device	5	2.5 inches	± 50 mils relative to others in byte lane and to associated DQSBn pair
DQBn (BSDDQMn)	DSP	5	2.5 inches	± 50 mils relative to others in byte lane and to associated DQSBn pair
DQGATEn	DSP	7	5.6 inches	± 100 mils relative to CK + DQSBn

(1) Maximum track length from the C6472/TCI6486 device and any memory device input is 1.8 inches when implementing four memory devices.

Vias add a significant delay. Within a net class, the number of vias on each net should ideally be kept the same. An allowance of 1 mismatch in the number of vias is acceptable for single-ended signals. Differential signals must have the same number of vias on each side of the differential pair:

- CK must have the same number of vias as $\overline{\text{CK}}$.
- DQS must have the same number of vias as $\overline{\text{DQS}}$.

Trace routes should be made as short and direct as possible. All trace routes must be less than the maximum lengths shown in Table 6 when measured from source to destination (not including the full "T" trace length).

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7.4.2 CK and ADDR_CTRL

The CK and ADDR_CTRL net classes are completely sourced by the C6472/TCI6486 DSP to the DDR2 devices (see Figure 7). The ADDR_CTRL nets are balanced "T" routes. Ideally, the PCB delay of the CK net class is identical to the delay for the ADDR_CTRL net class. All nets in the CK and ADDR_CTRL net classes should be matched in length to each other within 100 mils. The nets in the CK net class must be laid out as a differential pair. The trace separation between the differential pair of net class CK should be such as to maintain the desired differential impedance. Other traces should be kept away from the CK net class traces by at least 4 w center-to-center spacing (recall that w = minimum trace width/space). Traces within the ADDR_CTRL net classes should be spaced at least 3 w center-to-center from each other. Traces of other net classes should be kept 4 w away from the ADDR_CTRL net class. The length of segment A should be maximized and the overall length from A to B or A to C should be minimized.

This discussion about the two segments, B and C, can be expanded to four segments to support the x8 device implementation without loss of intent.

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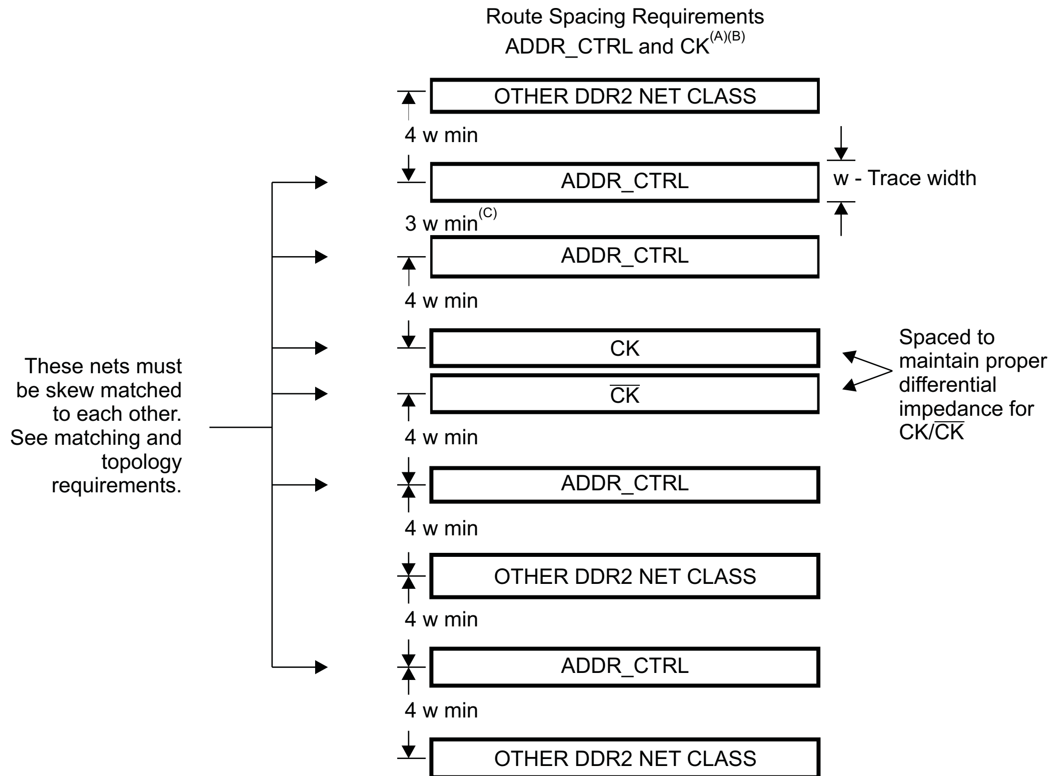
Figure 7. CK and ADDR_CTRL Routing Requirements



Matching and Topology Requirements
ADDR_CTRL

DSP — A — B — DDR2
DSP — A — C — DDR2

CK

DSP — A — B — DDR2
DSP — A — C — DDR2

A For ADDR_CTRL and CK:

- Length B should match length C within 100 mils.
- Length A should be maximized while meeting the above specifications.
- Total lengths of A + B and A + C should be no more than the length shown in Table 6 and use no more than 5 vias.
- Length A + B and A + C should match within 100 mils for the ADDR_CTRL net class and the CK net class.
- If implemented, a single series-terminating resistor should be located as close to the DSP as possible as part of segment A. Alternately, a pair of series-terminating resistors can be implemented, one in segment B and one in segment C, where they share the same via at the junction to segment A.

B In addition, for CK:

- The length of CK should match the length of net $\overline{CK}$ within 10 mils and have a differential impedance of 100 Ω.

C To escape the BGA and mitigate routing congestion, spacing can be reduced to 2 w for a total routed length of 500 mils.

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7.4.3 DQSBn and DQBn

The 8 net classes that make up the 4 DQSs and 4 DQ bytes have the same routing rules. Note that the individual byte net classes do not have to be matched to each other. Skew matching is only required between the DQBn net class and its associated DQSBn net class. The length of the DQSBn classes need to be within 1500 mils of the CK class nets. Figure 8 shows the topologies for the DQSBn and DQB nets.

These net classes are sourced by the C6472/TCI6486 device during writes and are sourced by the DDR2 devices during reads. The DQS acts as the data strobe as it is always sourced with the DQs. For write cycles, the DQS transitions in the middle of the bits cells on DQ. For read cycles, the DQS transitions at the same time as the DQ. The interface is more sensitive to DQS ↔ DQ crosstalk during reads. The data mask bits (BSDDQMn) are static during reads, therefore, they can be used as shields between the DQ and DQS to improve read crosstalk performance.

Ideally, the PCB delay of the DQSBn net class is identical to the delay for the DQBn net class. All nets in the DQSBn and DQBn net class should be matched in length to each other within 100 mils, centered about the length of DQSBn signals. The nets in the DQSBn net class must be laid out as a differential pair. The trace separation between the differential pair of net class DQSBn should be such as to maintain the desired differential impedance. Other traces should be kept away from the DQSBn net class traces by at least 4 w center-to-center spacing (recall that w = minimum trace width/space). Traces within the DQBn net classes should be spaced at least 3 w center-to-center from each other. Traces of other net classes should be kept 4 w away from the DQBn net class.

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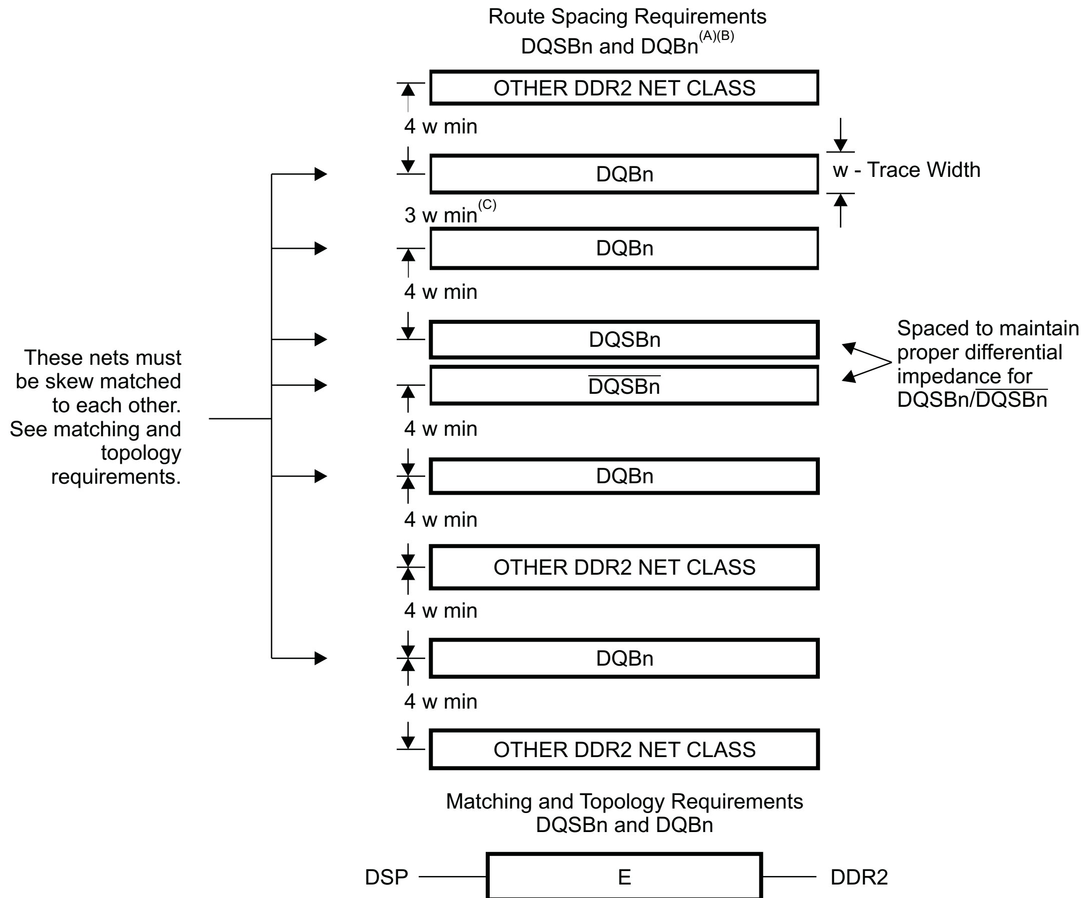
Figure 8. DQSBn and DQBn Routing Requirements



A For DQBn and DQSBn:

- Length E for DQB0 should match within ± 50 mils of DQSB0.
- Length E for DQB1 should match within ± 50 mils of DQSB1.
- Length E for DQB2 should match within ± 50 mils of DQSB2.
- Length E for DQB3 should match within ± 50 mils of DQSB3.
- Total length of E should be no more than 2.5 inches and use no more than 5 vias.
- If desired, a series-terminating resistor should be located as close to the DDR2 as possible except for BSDDQMn, which should be located close to the DSP.

B In addition, for DQSBn:

- The length of DQSBn should match the length of net $\overline{\text{DQSBn}}$ within 10 mils and have a differential impedance of 100 Ω.

C To escape the BGA and mitigate routing congestion, spacing can be reduced to 2 w for a total routed length of 500 mils.

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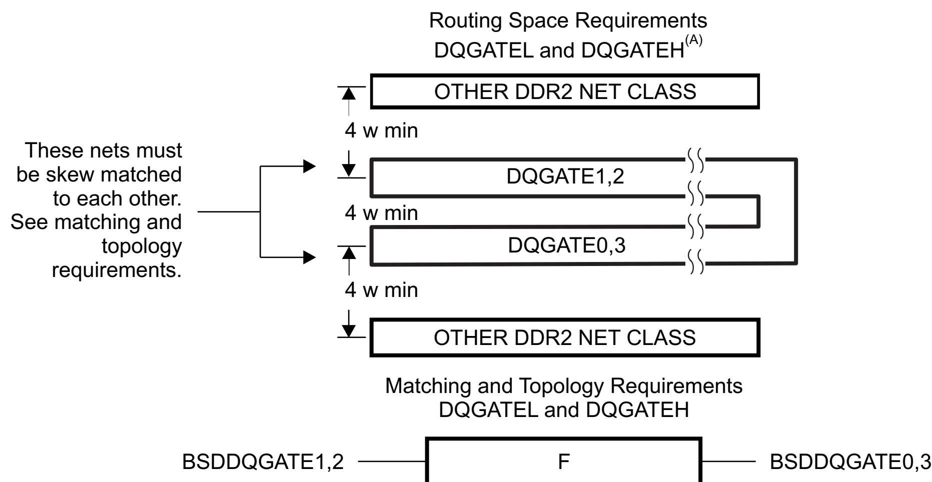
7.4.4 DQGATEL and DQGATEH

These two net classes are used by the C6472/TCI6486 to predict the round-trip delay of the PCB layout. The result is two out-and-back PCB traces that match the delay of the clock net plus the DQS. The rules for these net classes are shown in Figure 9.

For DQGATEL, the C6472/TCI6486 BSDDQGATE1 pin should be routed out and back to the C6472/TCI6486 BSDDQGATE0 pin. The total length of this route should be equal to the length of the CK net class plus the average length of the DQSB0 and DQSB1 net classes.

For DQGATEH, the C6472/TCI6486 BSDDQGATE2 pin should be routed out and back to the C6472/TCI6486 BSDDQGATE3 pin. The total length of this route should be equal to the length of the CK net class plus the average length of the DQSB2 and DQSB3 net classes.

Figure 9. DQGATEL and DQGATEH Routing Requirements



A For DQGATEL and DQGATEH:

- Length F should be equal to the length of the CK net class plus the average of the DQSB0 and DQSB1 for the DQGATEL net class.
- Length F should be equal to the length of the CK net class plus the average of the DQSB2 and DQSB3 for the DQGATEH net class.
- If desired, series-terminating resistors should be located as close to pins BSDDQGATE1,2 as possible.

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