WHITE PAPER

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Superior performance at breakthrough size, weight and power: Avionic and radar systems soar with TI's multicore DSPs

Introduction

Today's complex radar and avionics systems require high processing capabilities – but face restrictive size, weight and power (SWaP) constraints. The functions driving these systems are signal processing intensive. They benefit greatly from efficient implementations of digital signal processing (DSP) algorithms executed on size, performance and power efficient processors. These systems also have evolving requirements in design and data usage. In order to meet the requirements of SWaP efficiency and adaptability, programmable DSPs and Systems-on-Chip (SoCs) have become the processing platform of choice. They provide unmatched signal processing at very low power levels for radar and avionics, as well as software defined radios (SDR), imaging and video applications that often accompany radar and avionics.

Keeping up with the growing demand for SWaP efficient SoCs is challenging. They must cost effectively deliver performance while meeting objectives of low power consumption to address operational and environmental targets. TI's KeyStone based multicore devices are at the heart of SWaP efficiency. They provide multicore implementations of TI's leading TMS320C66x DSP cores, yielding the best power per watt in a small footprint. KeyStone devices are offered in a range of capacities with software compatibility throughout the range. This makes addressing diverse requirements or designing with future growth in mind straightforward and developmentally efficient.

Within the KeyStone platform, TI's TMS320C6657 and TMS320C6655 devices are ideal for radar and avionics systems. These devices are, respectively, pin compatible single core and dual core KeyStone DSPs.

Fixed and floating point processing

The use of multiple digital signal processor (DSP) cores is a key technology enabling increasingly sophisticated signal processing to advance the state of the art in waveform-intensive applications, such as avionics, radar, sonar, signal intelligence (SIGINT), image and video processing and software defined radio (SDR). Multicore capabilities, combined with an expanding array of AccelerationPacs and development tools for multicore DSPs, enable high performance at exceptionally low performance/watt in compact form factors.

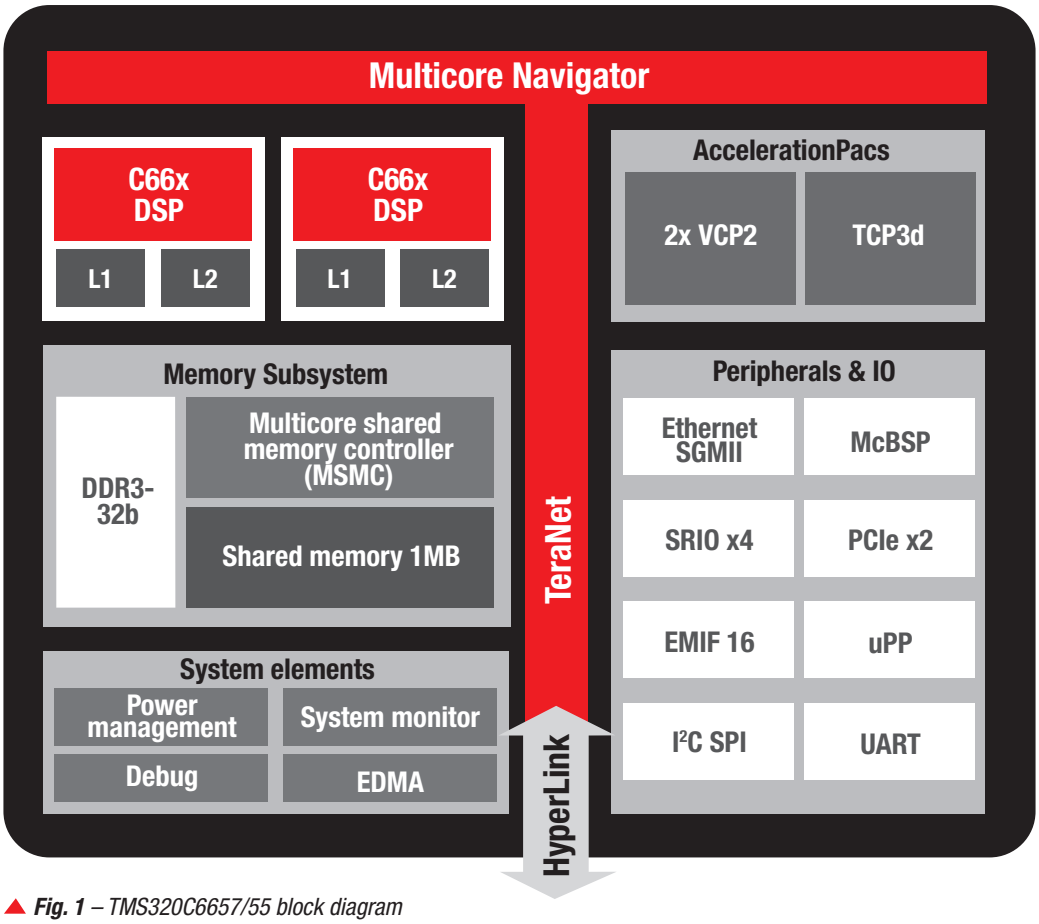
Avionics, radar and related applications need multicore DSPs to meet the advancing requirements of these mission critical applications including higher processing throughput, finer resolution, increased accuracy and the integration of advanced I/O. Many of these functions rely on floating point math to achieve the required precision. TI's KeyStone architecture provides significant flexibility to the designer by providing floating or fixed point execution within a single device on an instruction by instruction basis. And, the floating point operations execute at clock rates up to 1.25GHz – rates normally only reserved for fixed point devices. Designers no longer have to sacrifice performance to gain floating point accuracy or complicate designs with separate fixed and floating point processors.

Key features

- Based on TI's KeyStone multicore architecture for exceptional scalability and portability
- Available in single or dual TMS320C66x DSP cores
- 40 GFLOPs / 80 GMACs processing capability
- Fixed and floating point operation on each core
- Floating point performance at fixed point speeds
- Power efficient at 850 MHz to 1.25 GHz
- Leading power/performance ratio
- Integral Multicore Shared Memory Controller (MSMC)
- 1MB low latency SRAM shared by C66x cores
- TeraNet network-on-chip interconnect provides full multicore entitlement
- Multicore Navigator affords single-core simplicity to multicore SoC software design
- High-performance 40-nm process technology drives cost efficiency
- Industrial temperature ranges: -40°C to 100°C and -55°C to 100°C
- Integral Viterbi and Turbo AccelerationPacs boost communication applications

AccelerationPacs

In addition to exceptional DSP performance, the C6657/55 features Viterbi and Turbo AccelerationPacs for processing communications and waveform algorithms in low power hardware while taking advantage of the 1MB L2 memory per core and 1MB of shared memory. These AccelerationPacs operate independently from the programmable cores, freeing up DSP resources for other processing, thereby reducing latencies and streamlining software development. The KeyStone architecture's Multicore Navigator provides a hardware based abstraction layer that liberates software developers from the specifics of the underlying hardware. Multicore Navigator's queues and descriptors are used to automatically direct software tasks to the appropriate resource providing scalability and resource pooling as an integral function of the processor. Software leveraging Multicore Navigator can run on any KeyStone device providing scalability from one to many DSP cores without changes. Together, these elements provide high performance at low power levels demanded by SWaP-oriented applications. The C6657/55 is based on 40-nm process technology and deliver up to 80 GMACs and/or 40 GFLOPs at 1.25 GHz. Figure 1 below depicts a functional diagram of the C6657.



▲ ***Fig. 1*** *– TMS320C6657/55 block diagram*

High performance I/O

Quite often, these systems need to interoperate with equipment from multiple vendors and other legacy systems. The C6657/55 has a high-performance peripheral set supporting both the high data transfer rates required by modern systems as well as the flexibility to support legacy designs. Peripherals include:

- PCI Express port with two lanes supporting GEN2 up to 5 GBaud per Lane
- Four lanes of Serial RapidIO® (SRIO),compliant with RapidIO 2.1 spec for up to 5-Gbps operation per lane
- HyperLink supporting up to 50 GBaud inter connection with other KeyStone architecture devices to provide resource scalability
- Gigabit Ethernet (GbE) port with one SGMII port supporting up to 1000Mbps
- 32-bit DDR3 with ECC interfaces for up to 1,333 MHz speed
- 16-bit external memory interface (EMIF) for connecting to flash memory (NAND and NOR) and asynchronous SRAM
- Universal Parallel Port with two channels of 8 bits or 16 bits Each supporting SDR and DDR transfers
- Two Multichannel Buffered Serial Ports(McBSP)

The C6657/55 takes advantage of the rich peripherals and AccelerationPacs in the KeyStone architecture to provide full multicore entitlement in a compact and power efficient form factor.

The SRIO, PCIe, and HyperLink provide high-speed interconnects between multiple SoCs and/or FPGAs. HyperLink, an interface extension of the KeyStone architecture's internal bus, provides 50 Gbps in a point-to-point high speed interconnect. HyperLink provides a low overhead protocol and high-speed communication and connectivity to other KeyStone devices or FPGAs. It provides a solution to the scalability requirement in today's radar, SDR, and avionics systems. Alternately, SRIO and PCIe provide standards-based interconnect at lower bit rates.

The 32 bit DDR3 external memory interface (with ECC) in the C6657 provides 1,333 MHz busses with 8 GB of addressable memory space. TI's DDR3 implementation reduces latency associated with external memory access and provides the speed necessary to support the large amounts of data associated with these applications.

Size and Power

SWaP is a major requirement for the mission critical applications addressed above. TI has a rich history of providing the lowest-power DSPs and SoCs. The C6657 provides dual C66x DSP power, yet dissipates only 3.5 watts or less at 1GHz while delivering an ideal combination of performance and peripherals to address market needs. The compact 21 X 21 mm package provides the small form factor mission critical applications demand. The C6657/55/54 devices are also provided in a new low profile "thin" package (2.9mm in height), optimizing the overall system level packaging required for mission critical. In addition, these devices are available in extended temperature ranges of -55 to 100C, which are often called for in avionics applications.

Additionally, the C6657 can support the most complex waveform in software defined radios. The VCP and TCP3d accelerators, the internal share memory (up to 3MB) and the interface bandwidth provide the necessary performance to support and generate the most complex waveform used in many SDR applications.

Radar design requirements

Modern radar designs are incorporating signal-processing functions at the front end (exciter/receiver) of the radar system. This may include waveform generation, filtering, matrix-inverse operations, and signal correlation. There are also math functions in radar systems, which include recursive least-square and square-root operations. Many designers have implemented these functions in C-based processors (in fixed-decimal and/or floating-point operations). These types of designs can take advantage of the small form factor and dual fixed/floating cores provided in TI's C6657 to meet systems requirements.

For example, in adaptive-array designs and standard spatial transceiver-array processing (STAP), matrix inversion is an important element. Depending on the size of the array used in the radar system the matrix inversion can take advantage of parallel processing provided by the C6657 DSP to reduce latency and improve the power dissipation of the system. As the size of the array in the system increases, the floating-point multiplication required increases. The most likely design path for radar system designers is to implement this function using DSP and internal memory blocks. The C6657 provides up to 40 GFLOPs and 3 MB of internal memory of performance and is an excellent fit for this application.

Conclusion

The combination of peripherals and processing power provided by TI's C6657/55 DSPs brings many benefits to system design, including floating point performance at fixed point speeds, improved system flexibility, and reduced system cost and power. The peripherals included on the devices provide network connectivity (EMAC), a high-speed memory interface with ECC, standard bus interfaces (PCIe) and a high speed, low latency point-to-point interface (HyperLink). This advanced peripheral set enhances system performance and scalability and, due to integration, further reduces system cost. The combined fixed and floating point numerical performance of the C6657/55 provides a natural advantage when it comes to running the complex computationally intensive algorithms required for radar, SDR and avionics applications.

In conclusion, TI's C6657/55 DSPs offer exceptional SWaP performance for mission critical applications while reducing both chip count and board area in the overall system. To learn more about TI's multicore processors, please visit **www.ti.com/multicore**.

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