

Clocking Design Guide for KeyStone Devices

High-Performance and Multicore Processors

Abstract

This application note is intended to provide basic guidelines necessary to allow end-users to properly interconnect various types of clocking technologies to Texas Instruments high performance multiprocessor Digital Signal Processors. This document covers existing technologies and should be used in conjunction with good engineering practices. Where possible all high performance designs should be properly modeled to assure functionality in the manufactured end product. This application note covers the general concept of AC and DC clock coupling, terminations, and the impact of incorrect connections on the DSP and selected clock source.



Note—Read this entire application note including warnings and disclaimers prior to proceeding.

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Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this document.

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Terminology

| Term | Definition |
|--------------|---|
| AC | Alternating Current |
| Antipad | Open area surrounding the via in the various planes |
| CLK | Clock source, oscillator, or crystal depending on application |
| CML | Current Mode Logic |
| CMOS | Complementary metal-oxide-semiconductor |
| DC | Direct Current or Duty Cycle |
| Destination | Usually referred to as the DSP |
| Differential | Method of transmitting clock sources over a pair of traces which can improve noise immunity |
| DSP | Digital Signal Processor |
| ECL | Emitter-Coupled Logic |
| fF | femto-farad (e-15) |
| GTL | Gunning Transistor Logic (JESD8-3) |
| HPMP | High Performance Multi-Processor |
| HSTL | High Speed Transistor Logic |
| IO | Input/Output, usually referred to as a IO buffer |
| Ioh | High level Output Current |
| Iol | Low level Output Current |
| Iih | High level Input Current |
| Iil | Low level Input Current |
| LCJB | Low Jitter Clock Buffer |
| LVC MOS | Low Voltage Complementary metal-oxide-semiconductor |
| LVDS | Low Voltage Differential Signaling |
| LVPECL | Low Voltage Positive Emitter-Coupled Logic |
| LVTTL | Low Voltage Transistor-Transistor Logic |
| NRZ | Non-Return-to-Zero |
| PCB | Printed Circuit Board, also referred to as PWB or application board |
| PECL | Positive Emitter-Coupled Logic |
| pF | picofarad (e-12) |
| PWB | Printed Wiring Board, also referred to as PCB or application board |
| SONET | Synchronous optical networking |
| Single-ended | A common method for transmitting a clock source over a single trace (net) |
| Source | Usually referred to as the clock driver, oscillator, or clock buffer |
| SSTL | Stub Series Transistor Logic |
| TTL | Transistor-Transistor Logic |
| Via | An electrical/mechanical cylindrical interconnect between different PCB routing layers |
| Vil(min) | Low-Level Input Voltage (minimum) |
| Vil(max) | Low-Level Input Voltage (maximum) |
| Vih(min) | High-Level Input Voltage (minimum) |
| Vih(max) | High-Level Input Voltage (maximum) |
| Vol(min) | Low-Level Output Voltage (minimum) |
| Vol(max) | Low-Level Output Voltage (maximum) |
| Voh(min) | High-Level Output Voltage (minimum) |
| Voh(max) | High-Level Output Voltage (maximum) |

1 Introduction & General Overview

There exist two basic methods of connecting clock sources to the high-performance DSP: AC- and DC-Coupling. This is not to be confused with single-ended or differential clock sources, or with termination methods such as series or parallel which deal more with clocking standards and IO types than coupling.

This application note shall attempt to provide the basic information required to properly select a clock source, terminate, and couple it to the HPMP DSP. It also briefly explains the implications of improper clock sourcing and coupling.

2 Threshold Levels

Different interface standards utilize different threshold levels. Threshold levels, for the purpose of this application note shall be defined in two different categories: Input and Output.

2.1 Input Levels

Input levels are used to describe the minimum and maximum threshold levels necessary to obtain the correct logic state. In a clock source to DSP destination topology the input levels of concern are that of the DSP (if a clock buffer is inserted between the clock source and DSP then the same concept will need to be applied to all destination devices). Most clock source vendors as well as TI define input levels in the following manner:

Vil(min) - VIL min is the least-positive (most negative) value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

Vil(max) - VIL max is the most positive (least negative) value of low-level input voltage for which operation of the logic element within specification limits is to be expected. With regards to TI DSPs, any input logic value below this level is considered to be a logic-0.

Vih(min) - VIH min is the least positive (most negative) value of high-level input voltage for which operation of the logic element within specification limits is to be expected. With regards to TI DSPs, any logic level above this level is considered to be a logic 1.

Vih(max) - VIH max is the most positive (least negative) value of high-level input voltage for which operation of the logic element within specification limits is to be expected.



Note—TI datasheets do not typically specify a VIH(max), only a Vi is listed.

2.2 Output Levels

Output levels are used to describe the minimum and maximum threshold levels as provided on the output of clock sources to the DSP. These levels are the minimum and maximum values necessary to obtain the correct logic states. In a clock source to DSP destination topology the output levels of concern are that of the clock, clock buffer, or oscillator) between the clock source and DSP. Most clock source vendors as well as TI define input levels in the following manner:

Vol(min) - VOL min is the least-positive (most negative) value of low-level output voltage for which operation of the logic element within specification limits is to be expected.

Vol(max) - VOL max is the most positive (least negative) value of low-level output voltage for which operation of the logic element within specification limits is to be expected. With regards to TI DSPs, any input logic value below this level is considered to be a logic-0.

Voh(min) - VOH min is the least positive (most negative) value of high-level output voltage for which operation of the logic element within specification limits is to be expected. With regards to TI clock sources, any logic level above this level is considered to be a logic 1.

Voh(max) - VOH max is the most positive (least negative) value of high-level output voltage for which operation of the logic element within specification limits is to be expected.



Note—TI datasheets do not typically specify a VOH(max), only a Vo is listed.

2.3 Threshold Limits

Table 1 and Figure 1 identify various threshold limits for different technologies used within Texas Instruments DSP and clocking products. As with all design efforts, input (VIH/VIL) and output (VOH/VOL) levels should be verified (against temperature & voltages as well as technology) prior to releasing your design. Refer to each respective data sheet for threshold levels.

Table 1 Texas Instruments Threshold Limits

| Technology | TI DSP Inputs | | | | TI Clock Source Outputs | | | | VCM | V. Swing (Single ended) | Vcc |
|---|---------------|-----------|-----------|-----------|-------------------------|-----------|-----------|-----------|-------|-------------------------|---------|
| | VIH (min) | VIH (max) | VIL (min) | VIL (max) | VOH (min) | VOH (max) | VOL (min) | VOL (max) | | | |
| PECL | 3.835 | 4.120 | 3.190 | 3.525 | 4.020 | 4.190 | 3.050 | 3.370 | | 5.000 | 5.000 |
| CMOS (5.0 V) | 3.500 | 5.000 | 0.000 | 1.500 | 4.400 | 5.000 | 0.000 | 0.330 | 2.500 | 5.000 | 5.000 |
| TTL | 2.000 | 5.000 | 0.000 | 0.800 | 2.000 | 5.000 | 0.000 | 0.800 | | 5.000 | 5.000 |
| GTL | 0.834 | | | 0.950 | 1.500 | | | 0.550 | | 5.000 | 5.000 |
| LVPECL | 2.135 | 2.420 | 1.490 | 1.825 | 2.400 | 2.790 | 2.170 | 1.600 | 2.000 | 0.800 | 3.300 |
| LVC MOS | 1.890 | 2.520 | 0.540 | 0.720 | 2.600 | 3.500 | 0.000 | 0.100 | 1.650 | 3.300 | 3.300 |
| CMOS (3.3 V) | 2.000 | 3.300 | 0.000 | 0.800 | 2.400 | 3.300 | 0.000 | 0.400 | | 3.300 | 3.300 |
| LVDS (3V3 / 2V5) | 2.000 | | | 0.800 | 1.450 | | | 0.950 | 1.200 | 0.350 | 3.3/2.5 |
| LVDS (1V8) | 1.800 | | | 0.635 | 1.150 | | | 0.650 | 0.900 | 0.350 | 1.800 |
| CML (3.3 V) | 3.300 | | | 2.900 | 3.300 | 3.300 | 2.200 | 2.900 | 3.100 | 0.800 | 3.300 |
| LVTTTL (3.3 V) | 2.000 | 2.500 | 0.400 | 0.800 | 2.000 | 2.400 | 0.000 | 0.400 | 1.650 | 3.300 | 3.300 |
| CMOS (2.5 V) | 1.700 | Vdd+0.3 | -0.300 | 0.875 | 1.800 | | | 0.600 | | 2.500 | 2.500 |
| CMOS (1.8 V) | 1.170 | | | 0.630 | 1.350 | | | 0.450 | | 1.800 | 1.800 |
| CML (1.8 V) | 1.800 | | | 1.400 | 1.800 | 1.800 | 1.300 | 1.400 | 1.600 | 0.400 | 1.800 |
| HSTL (CL1) | 0.850 | | | 0.650 | 1.100 | | | 0.400 | | 0.200 | 1.500 |
| Note: Logic levels may vary at different temperatures - check data sheets | | | | | | | | | | | |

End of Table 1
 Note: Vcc = Vcc ± tolerance
 Note: TTL and standard CMOS levels will vary depending on technology, refer to data sheet for specifications

Another quick method to view appropriate interface logic levels can be obtained by using the chart in Figure 1.

Figure 1 Logic Threshold Chart

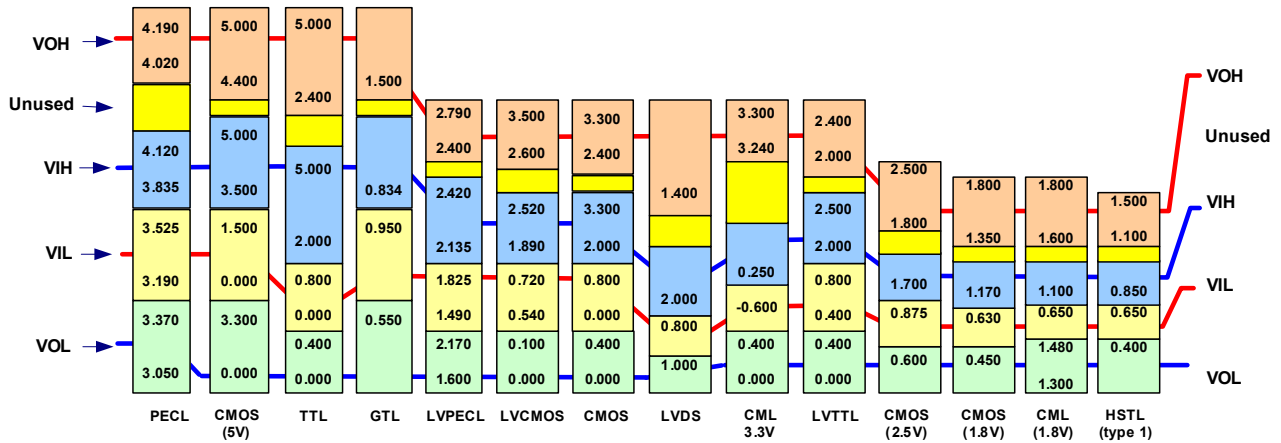
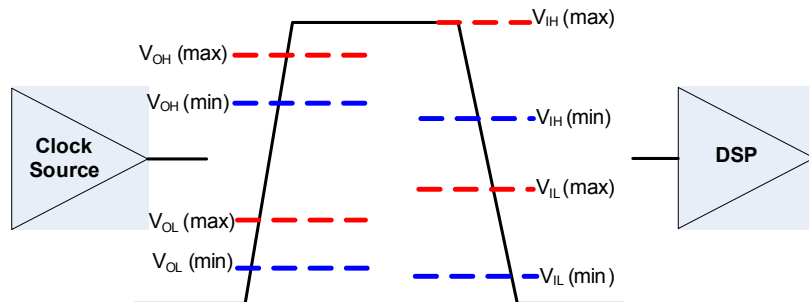


Figure 2 diagrammatically illustrates the relationship between input and output levels.

Figure 2 Input - Output Relationship



3 DSP Clock Inputs and Sources

The following section describes the most common Clock inputs (pins) to the HPMP DSP. Clocking input types (technologies) differ across DSP generations and should be verified prior to releasing your design to production.

3.1 DSP Clock Input Pins

The DSP may have any combination of the following clock input pins ([Table 2](#)). In some instances, many may have been already multiplexed on the DSP.

Table 2 DSP Clock Input Requirements (Pins)

| DSP Clock Input Pin | DSP Pin Definition | Interconnection Technology | Clock Source Req. |
|---------------------|--------------------------------|--|-------------------|
| SYCLK | System Clock | External Clock Supplied | Yes |
| CORECLK | System Clock | External Clock Supplied | Yes |
| ALTCORECLK | Alternate Core Clock | Differential External Clock Supplied | Optional |
| DDRREFCLK | DDR(/2/3) Reference Clock | Differential External Clock Supplied | Yes |
| RIOCLK(p/n) | Serial RapidIO Source Clock | External Clock Supplied | Yes |
| SGMIICKL | | External Clock Supplied | Yes |
| AIFCLK | Antenna Interface Source Clock | External Clock Supplied | Yes |
| FSYNCLK | | Differential External Clock Supplied | Yes |
| ALTFSYNCLK | | External Clock Supplied | Optional |
| TRTCLK | | External Clock Supplied by DSP or LB | No |
| TCLK | Emulation/JTAG clock | Clock supplied by external emulator | No |
| CLKSx | Timer Clocks | Internally Generated for External Clocks | No |
| CLKINx | Typically for PLL Clock Inputs | External Clock Supplied | Yes |
| CLKXx | McPSB Transmit Clock | Internally Generated Clock | No |
| UXCLK | Utopia Clock Source | Internally Generated Clock | No |
| MTCLK | MII Transmit Clock Source | Internally Generated Clock | No |
| GMTCLK | GMII Transmit Clock Source | Internally Generated Clock | No |
| SCL | I2C Clock Source | Externally Supplied, part of bus | No |
| VCLK | YLYNQ Clock Source | Internally Generated Clock Source | No |
| CLKRx | McPSB Receive Clock | Internally Generated Clock | No |
| PCLK | PCI Clock Source | Can be Internally or Externally Supplied | Yes |
| AECLKIN | EMIF Clock Source | External Clock Supplied | |

End of Table 2

3.2 DSP Clock Sources

Defining the clock source should first start by identifying the DSP input requirements (single-ended or differential), then by determining which clocking technology is required (refer to the respective data sheet and hardware design guides where possible). Many Texas Instruments DSPs will accommodate either a single-ended or differential clock source, and in most newer DSPs many of the clocking inputs have been reduced to a smaller number, thereby decreasing the number of external clock sources required. [Table 3](#) defines the most common clock input types used with TI DSPs today as well as other technologies that may be used if coupled properly.

Table 3 Common Clock Inputs

| COMMON CLOCKING TECHNOLOGIES | | |
|--|----------------------------|--|
| Clocking Technology | Clock Configuration | Input Clocking Supply Voltage Levels (dc) |
| LVPECL | Differential Clock Output | 2.5 V – 3.3 V |
| LVC MOS | Single Ended Clock Output | 1.2 V – 3.3 V |
| LVDS | Differential Clock Output | 1.8 V – 3.3 V |
| CML | Differential Clock Output | 1.8 V – 3.3 V |
| HSTL | Differential Clock Output | 1.5 V |
| SSTL | Differential Clock Output | 1.2 V – 1.8 V |
| LVTTL | Single Ended Clock Output | 3.3 V |
| UNUSED BUT COMMON CLOCKING TECHNOLOGIES | | |
| Clocking Technology | Clock Configuration | Voltage Input Levels |
| PECL | Differential Clock Output | 5.00 V |
| CMOS (5.0 V) | Single Ended Clock Output | 5.00 V |
| TTL | Single Ended Clock Output | 5.00 V |
| GTL | Single Ended Clock Output | 3.3 V – 5.0 V |
| End of Table 3 | | |

4 DC-Coupling Concepts and Techniques

The use of DC-Coupling involves direct connection between the clock source and clock destination. DC-Coupling primarily occurs in systems where there is a need for wide bandwidths. In all cases both the clock source and clock destination must have identical ground potentials, and should be located on the same application platform and within close proximity to one another (source and destination). DC-Coupling does not require any coupling capacitors (see AC-Coupling) and in most cases incorporates series termination resistors to optimize over and under shoots encountered with the faster edge rates of higher frequency clock sources.

Many of the following figures incorporate capacitors in the range of 200fF to 700fF. These individual components are not required as they represent vias and component pads for simulation purposes.

4.1 DC-Coupling Pros and Cons

4.1.1 Pros

- Components are directly connected together (use of discrete components)
- No need for additional components (except possibly series termination resistors)
- Board design is simpler to route
- Works well with telecommunication architectures like Synchronous Optical Networking and non-return to zero (NRZ) applications
- DC wander or DC drift is minimized due to same ground potential and proximities

4.1.2 Cons

- Both the clock source and the DSP must be at the same ground potential
- Both the DSP and clock source should be on the same application board
- Possibility of large over and under shoots without the use of termination resistors
- Requires proper power supply design (including a clean and tight tolerance input supply)
- In some applications, specific slew rates may be required.

4.2 DC-Coupling Interface Schemes and Examples

This subsection provides examples for interfacing common technologies (in a TI DSP application) using DC-Coupling. All illustrations assume the DSP to be the clock destination (unless otherwise noted). The following interface combinations are provided (other combinations are also available but uncommon in HPMP DSP applications):

| | | |
|---------------|---------------|-------------|
| LVPECL → LVDS | LVDS → LVDS | CML → HSTL |
| LVPECL → CML | LVDS → CML | CML → LVDS |
| LVPECL → HSTL | LVDS → HSTL | HSTL → HSTL |
| CMOS → LVDS | CML → CML | HSTL → LVDS |
| CMOS → LVPECL | LVTTL → LVTTL | |

4.2.1 LVPECL Clock Source – DC-Coupling

LVPECL by definition can be supplied by either a 3.3 Vdc or 2.5 Vdc source (depends on component selected).

The following recommended scheme (Figure 3) denotes the component values to use in a 3.3 Vdc LVPECL → LVDS application. The series termination resistors (33 Ω) are required to properly level set the LVPECL output to the DSP LVDS input. If an intermediate LVDS clock buffer is to be used to distribute the single clock input source to multiple DSP processors (much like the CDCLVD110A) the recommended configuration would be similar to Figure 4. Simulation results for each of these recommended configurations are included in Section 7, Simulations 1 & 2.

Figure 3 DC-Coupling (LVPECL → LVDS)

DesignFile Untitled
HyperlynxSimV80

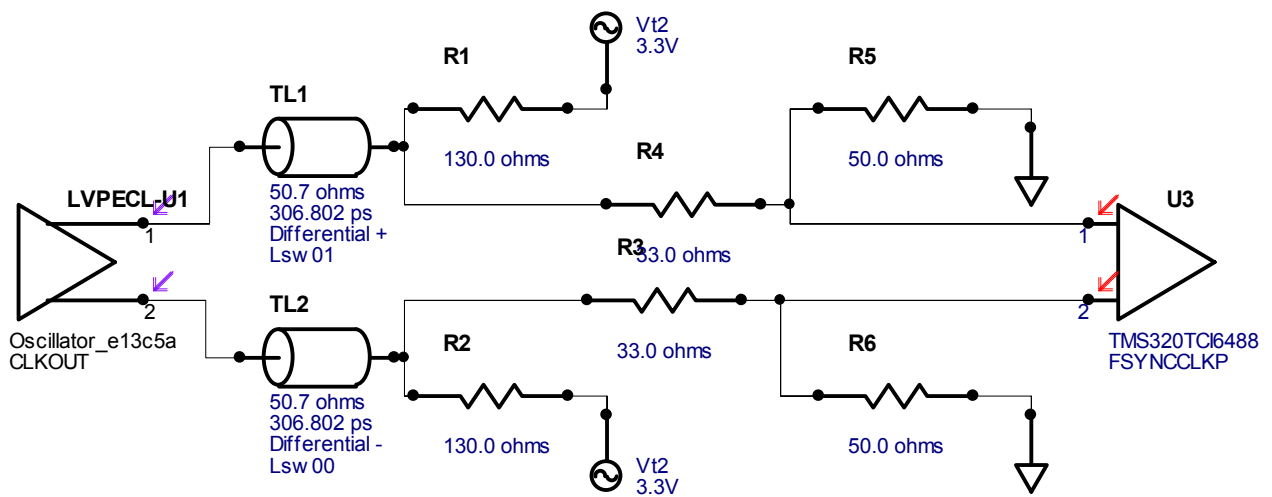
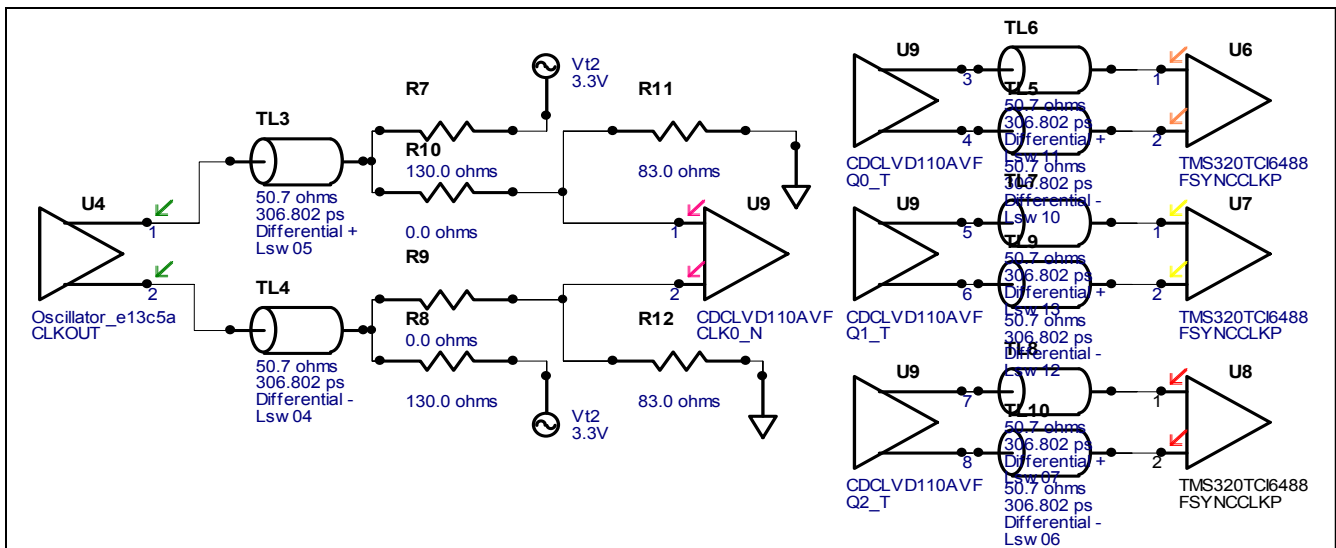
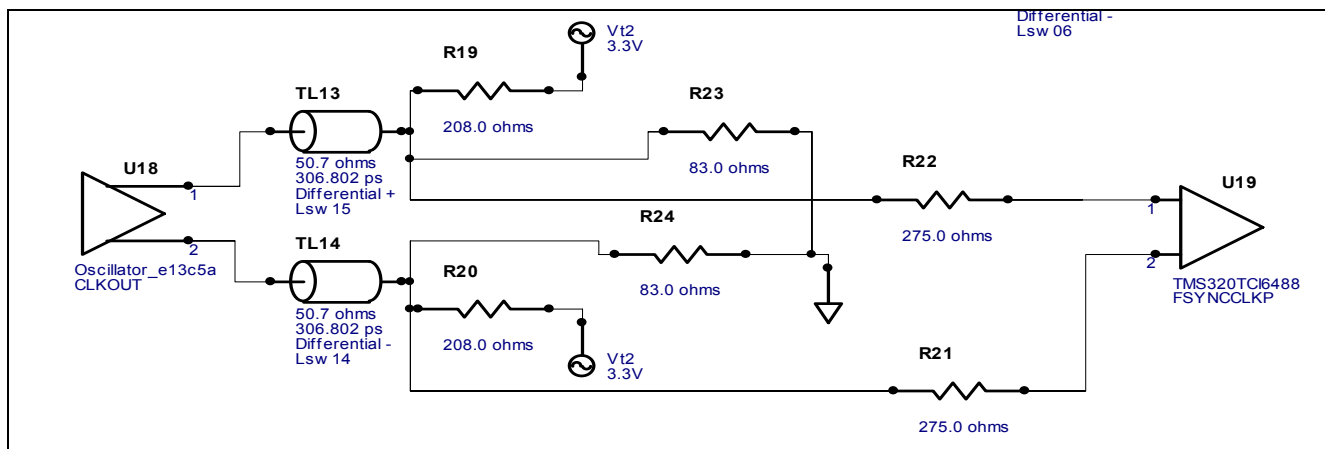


Figure 4 DC-Coupling (LVPECL → LVDS (Buffer) → LVDS (DSP))



Many DSPs contain or support a CML input. To properly connect a LVPECL clock source to a CML input, Figure 5 illustrates the preferred connection. The simulation result for the following LVPECL → CML input is included in Section 7, Simulation 3.

Figure 5 DC-Coupling (LVPECL (Clock) → CML (DSP))

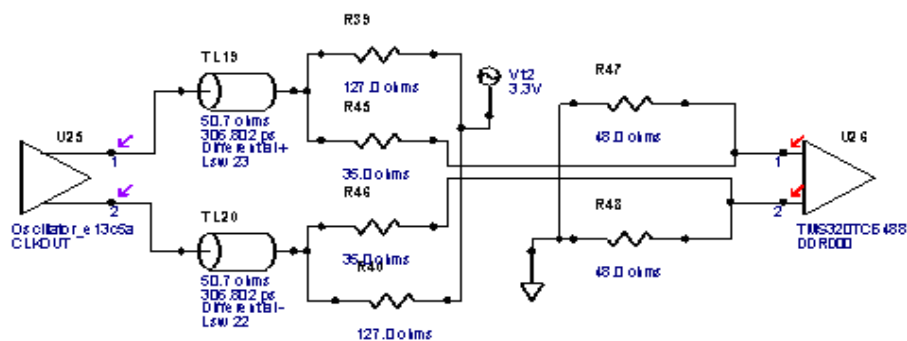


To properly interconnect an LVPECL clock source to a DSP HSTL input buffer, Figure 6 illustrates the preferred component selection (provided the V_{dd} level is 3.3 V). The simulation result for the following LVPECL → HSTL input is included in Section 7, Simulation 4.

Note:

- For V_{CC} = 3.3 V, use R1 = 127 Ω, R2 = 35 Ω, R3=48 Ω
- For V_{CC} = 2.5 V, use R1 = 100 Ω, R2 = 40 Ω, R3=60 Ω

Figure 6 DC-Coupling (LVPECL (Clock) → HSTL (DSP))

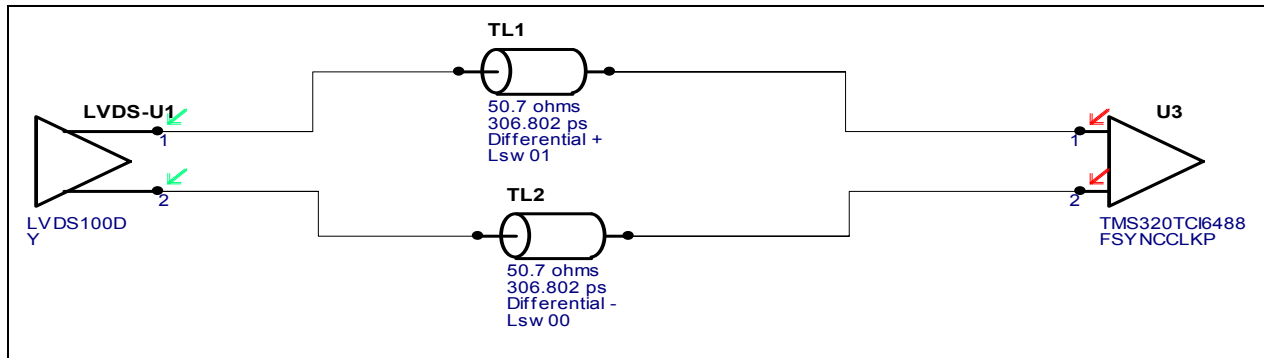


4.2.2 LVDS Clock Source – DC-Coupling

LVDS clock sources are differential by design and include two (2) outputs (+ & -). In most cases the DSP will already incorporate an internal 100 Ω termination resistor – therefore an external termination resistor (typically required) between the two destination inputs is not required. In either case (external or internal 100 Ω termination) the common mode voltage should be around 1.2 V. If an external 100 Ω termination resistor is required it must be positioned as close to the DSP input pins as possible.

Most current HPMP DSPs incorporate or support a LVDS input. To properly connect a LVDS clock source to a LVDS input, [Figure 7](#) illustrates the preferred connection. The simulation result for the a LVDS → LVDS input is provided in [Section 7, Simulation 5](#). Refer to the warnings and simulation sections for additional information before selecting this method.

Figure 7 DC-Coupling (LVDS (Clock) → LVDS (DSP))



[Figure 8](#) illustrates the preferred connection between an LVDS clock source and CML input to the DSP. The simulation result for the following LVDS → CML input is included in [Section 7, Simulation 6](#).

Figure 8 DC-Coupling (LVDS (Clock) → CML (DSP))

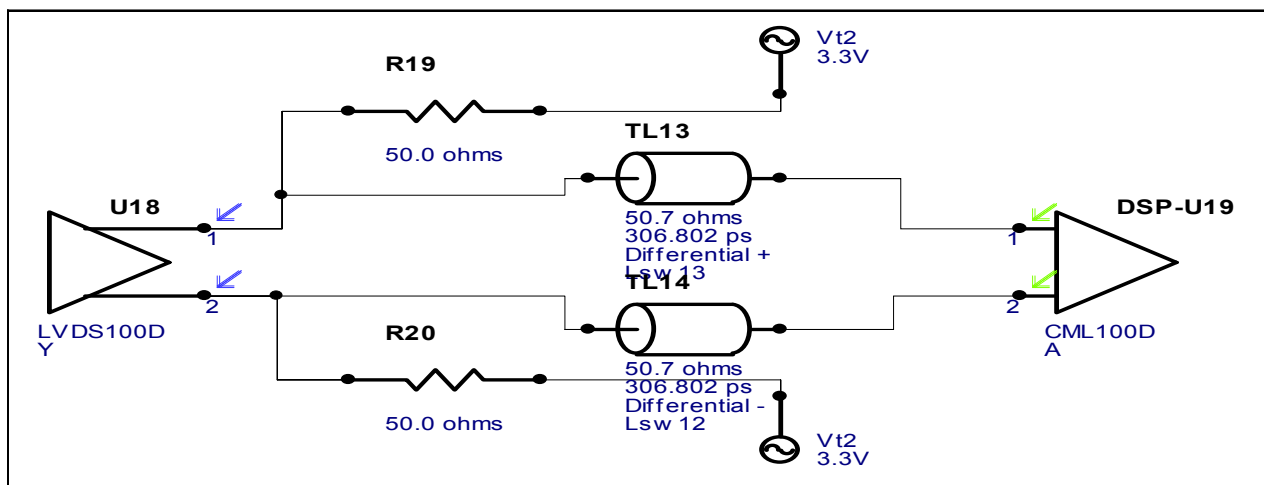
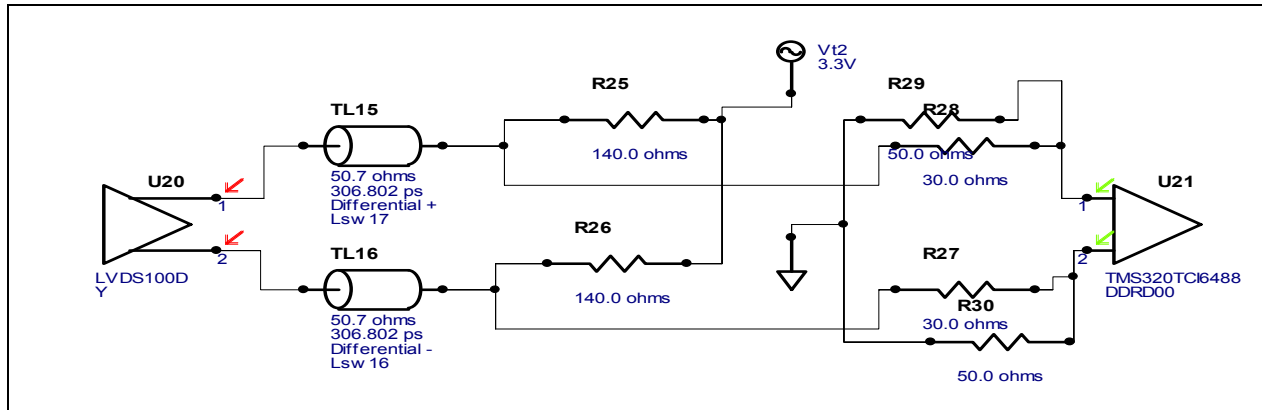


Figure 9 illustrates the preferred connection between an LVDS clock source and HSTL input to the DSP. The simulation result for the following LVDS → HSTL input is included in Section 7, Simulation 7.

Figure 9 DC-Coupling (LVDS (Clock) → HSTL (DSP))



Note: For Vcc = 3.3 V; R25 & R26 = 140 Ω, R27 & R28 = 30 Ω, R29 & R30 = 50 Ω
 For Vcc = 2.5 V; R25 & R26 = 100 Ω, R27 & R28 = 36 Ω, R29 & R30 = 60 Ω

4.2.3 CML Clock Source – DC-Coupling

The CML clock sources typically provide for important features including adjustable output logic swing, high-speed capabilities, level adjustment, and slew rate adjustment. Most CML clock sources incorporate an open-drain differential output pair (+ & -) and require pull up resistors to Vdd (output transistors can only drive on falling edges and pull ups are required to allow the output to drive on rising edges).

Figure 10 illustrates the preferred connection between a CML clock source and LVDS input to the DSP. The simulation result for the following CML → LVDS input is included in Section 7, Simulation 8.



Note—DC-Coupling is allowed when the output CML common mode level is within the LVDS common mode input range.

Figure 10 DC-Coupling (CML (Clock) → LVDS (DSP))

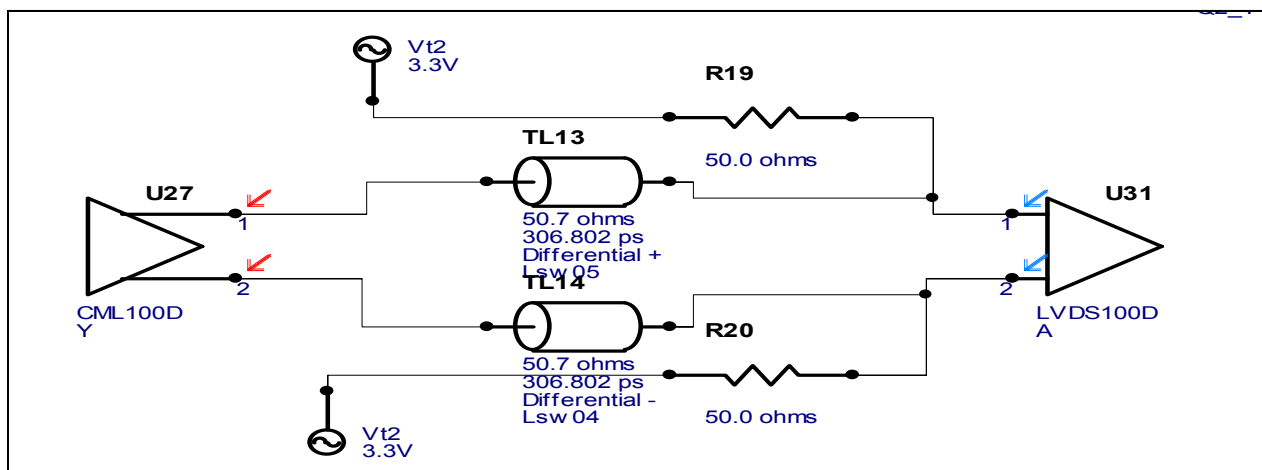


Figure 11 illustrates the preferred connection between a CML clock source and CML input to the DSP. The simulation result for the following CML → LVDS input is included in Section 7, Simulation 9.

Figure 11 DC-Coupling (CML (Clock) → CML (DSP))

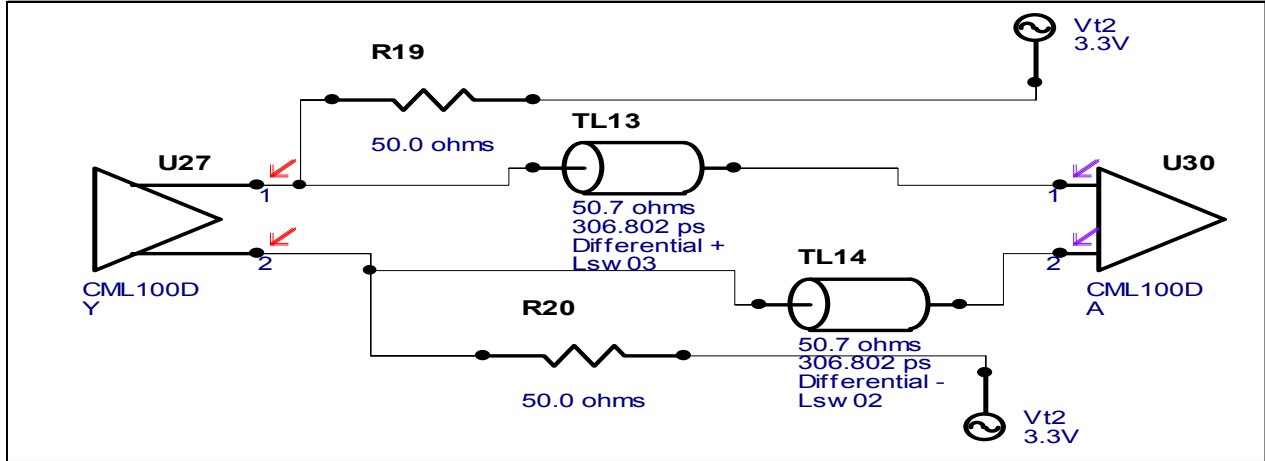
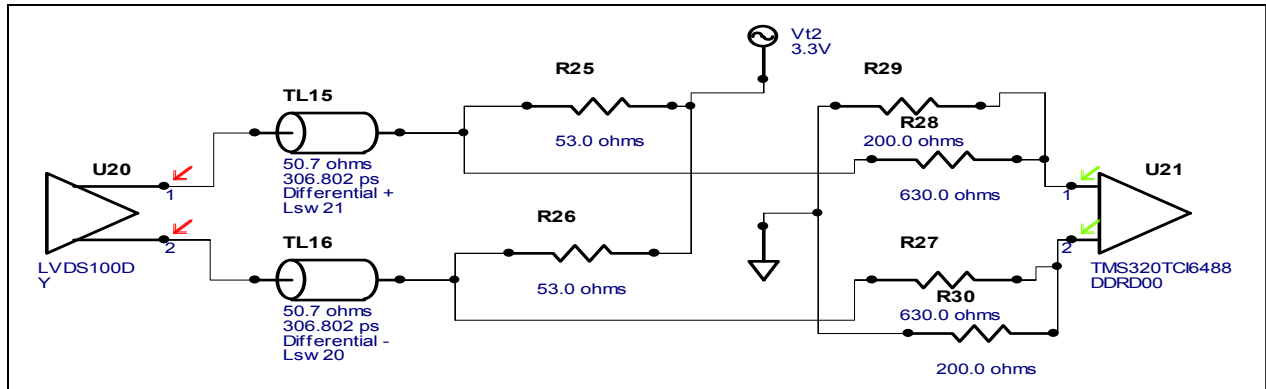


Figure 12 illustrates the preferred connections between a CML clock source and HSTL input to the DSP. The simulation result for the following CML → LVDS input is included in Section 7, Simulation 10.

Figure 12 DC-Coupling (CML (Clock) → HSTL (DSP))



4.2.4 HSTL Clock Source – DC-Coupling

Figure 13, the proper interconnection between a HSTL clock source and HSTL input to the DSP is provided. The simulation result for the following HSTL → HSTL input is included in Section 7, Simulation 11.

Figure 13 DC-Coupling (HSTL (Clock) → HSTL (DSP))

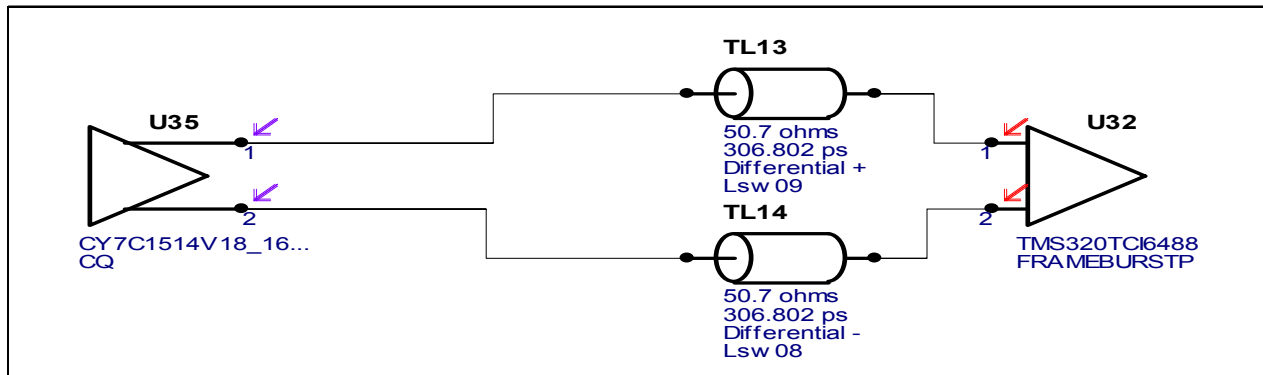
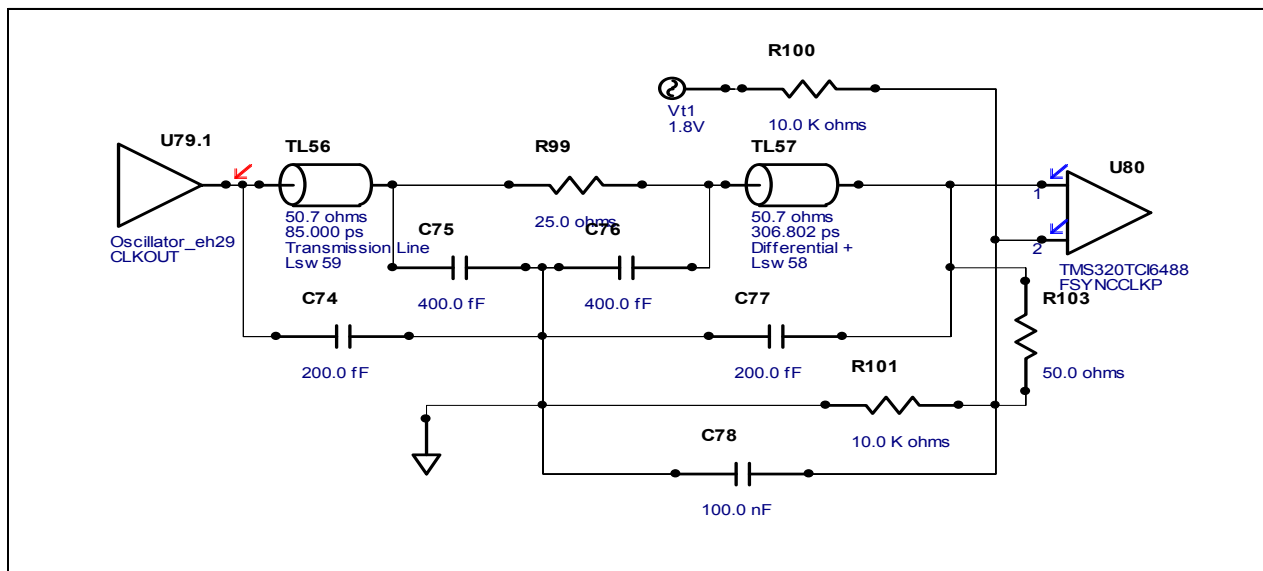


Figure 14 illustrates the interface between a single-ended HSTL or SSTL clock source into a DSP with a differential LVDS input. The simulation result for the following HSTL → LVDS input is included in Section 7, Simulation 12.

Figure 14 DC-Coupling (HSTL (Clock) → LVDS (DSP) – single-ended)



4.2.5 LVTTTL / CMOS Clock Source – DC-Coupling

When using a LVTTTL (or CMOS) single ended clock source it is mandatory that the output of the clock source be of the correct voltage level (e.g., a 1.8 Vdc DSP input clock buffer will not functional properly when supplied with a 3.3 V or 5.0 V clock source). Improper voltage levels to the DSP may affect its reliability and will void all warranties. The following three figures illustrate the effects of improper termination placement. Figure 15 is constructed with the series termination closest to the destination (DSP),

whereas Figure 16 has the termination placed closer to the source (clock). Figure 17 has the termination placed at the midpoint of the transmission line. The respective simulations for each of these concepts are included in Section 7, Simulations 13, 14, and 15.

Figure 15 DC-Coupling (LVTTTL (clock) → LVTTTL (DSP)) #1

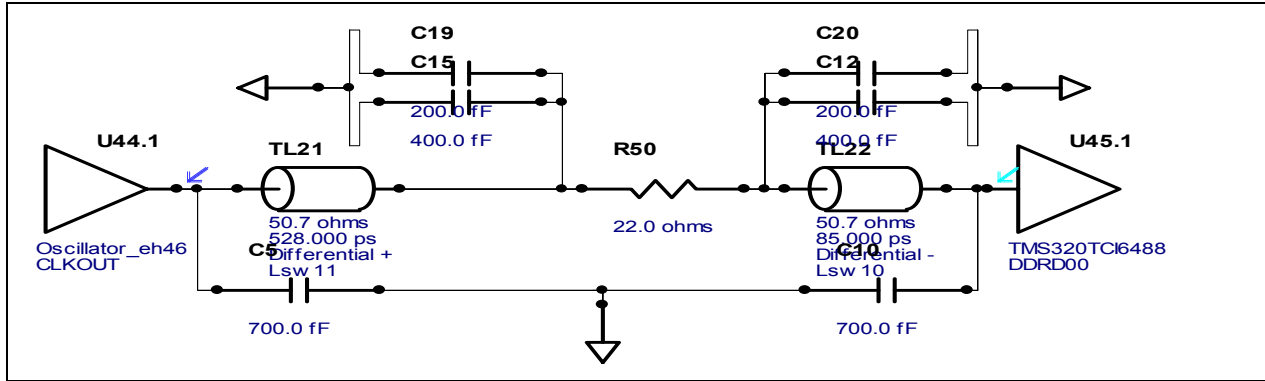


Figure 16 DC-Coupling (LVTTTL (clock) → LVTTTL (DSP)) #2

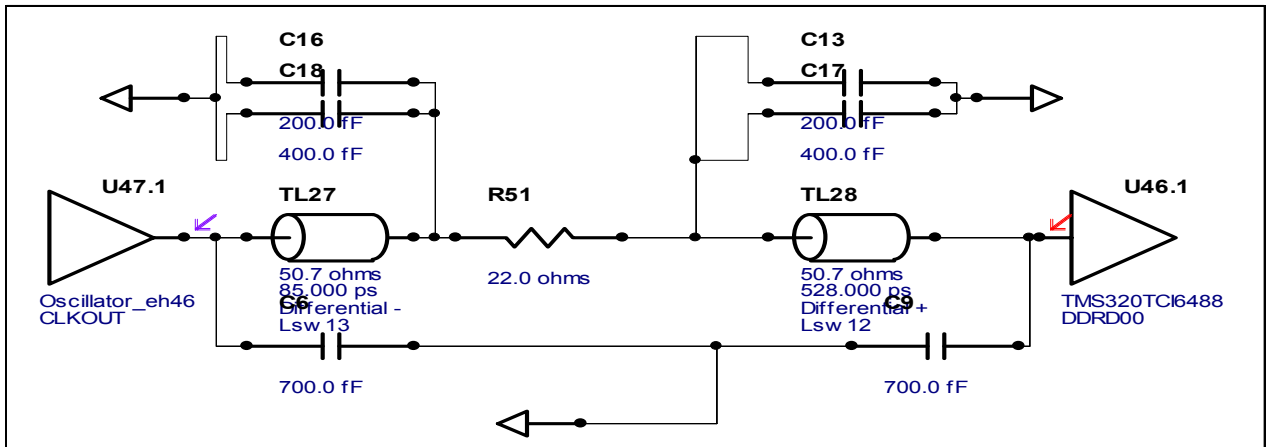
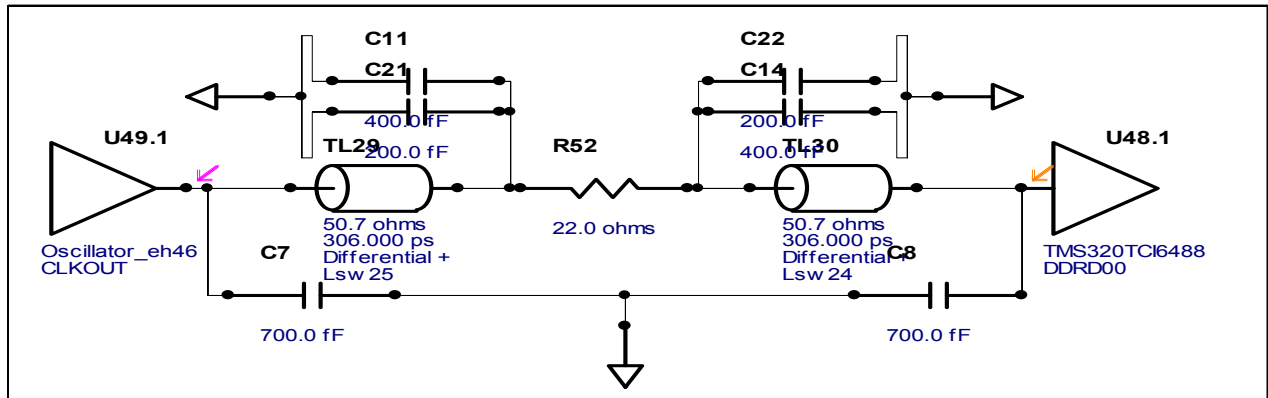
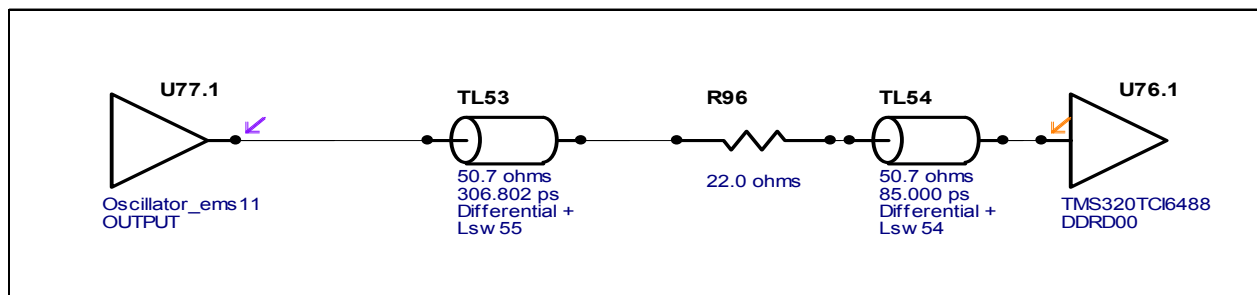


Figure 17 DC-Coupling (LVTTTL (clock) → LVTTTL (DSP)) #3



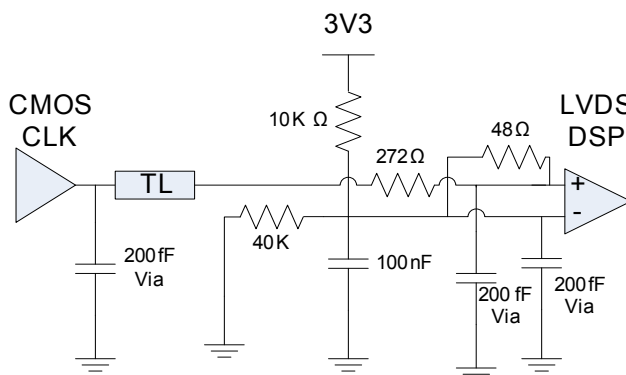
In [Figure 18](#) the preferred connection is shown for a 1.8 V LVTTTL/CMOS clock source and 1.8 V LVTTTL/CMOS input to the DSP.

Figure 18 DC-Coupling (LVTTTL (clock) → LVTTTL 1.8V (DSP))



In [Figure 19](#) the preferred connection is shown for a 3.3 V LVTTTL/CMOS clock source and 3.3 V LVTTTL/CMOS input to the DSP. The simulation result for the following 3.3 V LVTTTL/CMOS → 3.3 V LVTTTL/CMOS input is included in [Section 7](#), Simulation 16.

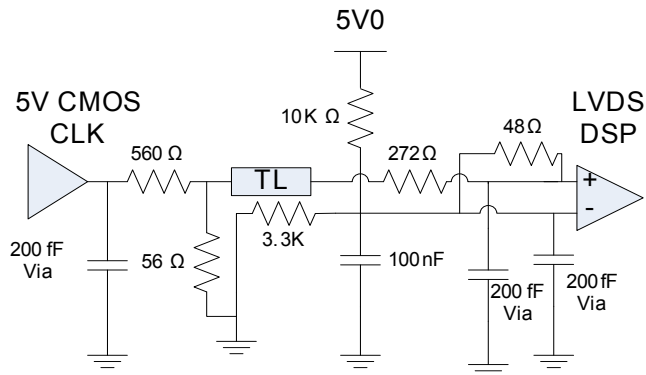
Figure 19 DC-Coupling (3.3 V CMOS (clock) → LVDS (DSP))



Note—Although it is possible to adapt single-ended clock sources to differential inputs, it is not always recommended – component tolerance, input levels and the like can affect signal integrity and swing. It is always better to use matching clock sources to IO input types (e.g., LVDS → LVDS, etc.).

In [Figure 20](#) the preferred connection is shown for a 5.0 V LVTTTL/CMOS clock source and 5.0 V LVTTTL/CMOS input to the DSP. The simulation result for the following 5.0 V LVTTTL/CMOS → 5.0 V LVTTTL/CMOS input is included in [Section 7](#), Simulation 17.

Figure 20 DC-Coupling (5.0 V CMOS (clock) → LVDS (DSP))



5 AC-Coupling Concepts and Techniques

The use of AC-Coupling primarily occurs in systems where there is a need for wide bandwidths, or where interconnections between different layers (application board) is required. AC-Coupling is used to change the common-mode voltage level by using series capacitors. AC-Coupling using capacitors removes the DC component of the signal (common mode voltage) while retaining the AC component or voltage swing.

For high-speed applications, the use of AC-Coupling is typically recommended for DC-balanced signals like clock signals (50/50% to 45/55% duty cycle), and 8B/10B encoded data.

5.1 AC-Coupling Pros and Cons

5.1.1 Pros

- Blocks DC component of waveform
- Components are connected together using capacitors
- Minimal components required to implement
- Improves performance at higher frequencies
- Provides level shifting
- The DSP and clock source can be in different locations of the same application board
- Both the clock source and the DSP must be at the same ground potential
- Removes common mode errors

5.1.2 Cons

- Degrades low frequency performance
- Tight tolerance band (window)
- Interconnecting technologies (clock to DSP) may differ
- Does not work well in clocking or data schemes where DC varies greater than 45/55%

5.2 Interface Schemes and Examples

This subsection provides examples for interfacing common technologies (in a TI HPMP DSP application) using AC-Coupling. All illustrations assume the DSP to be the clock destination (unless noted). The following interface combination examples are provided (other combinations are also available but uncommon in HPMP DSP applications):

| | | |
|---------------|-------------------------|-----------------|
| LVPECL → LVDS | LVDS → LVDS | HSTL → HSTL |
| LVPECL → CML | CML → LVDS | HSTL → LVTTTL |
| LVPECL → HSTL | CML → CML | LVTTTL → LVTTTL |
| LVDS → LVDS | CML → HSTL | |
| LVDS → CML | HSTL → CMOS & TTL logic | |

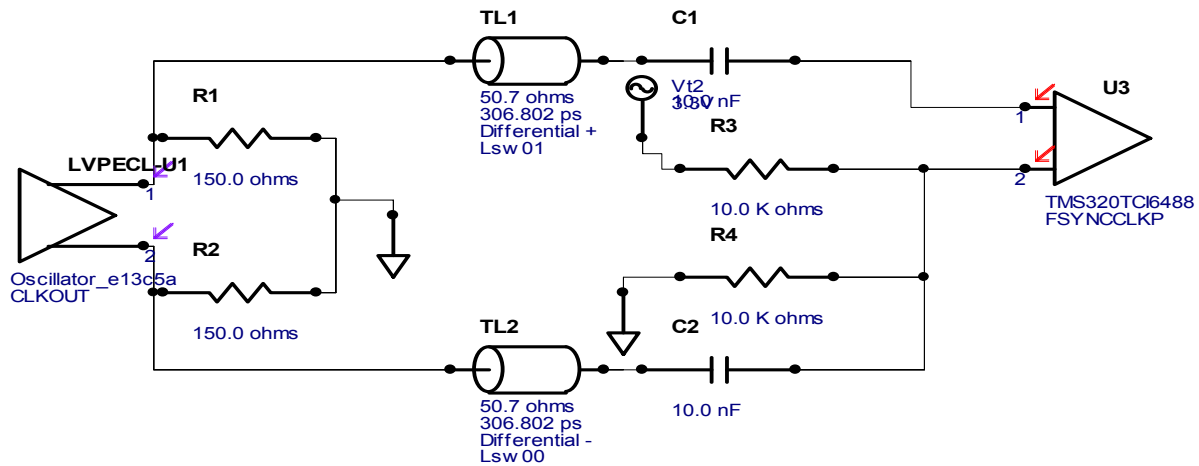
5.2.1 LVPECL Clock Source – AC-Coupling

LVPECL clock sources have gained wide acceptance due to their reduced supply voltage (3.3 V as opposed to traditional 5.0 V PECL or ECL logic levels) and reduced power consumption. In all cases (to date) the individual trace impedance should be kept at 50 Ω each.

In [Figure 21](#), each complementary clock output signal is connected to a 150 Ω resistor to ground in order to properly dc-bias the LVPECL output and provide a dc current path for the source current. The external or internal 100 Ω termination resistor terminates the differential 100 Ω transmission line and provides for a sufficient signal swing necessary to drive the LVDS input IOs. In all cases where DC biasing resistors are used they must be placed as close to the clock source pins as possible.

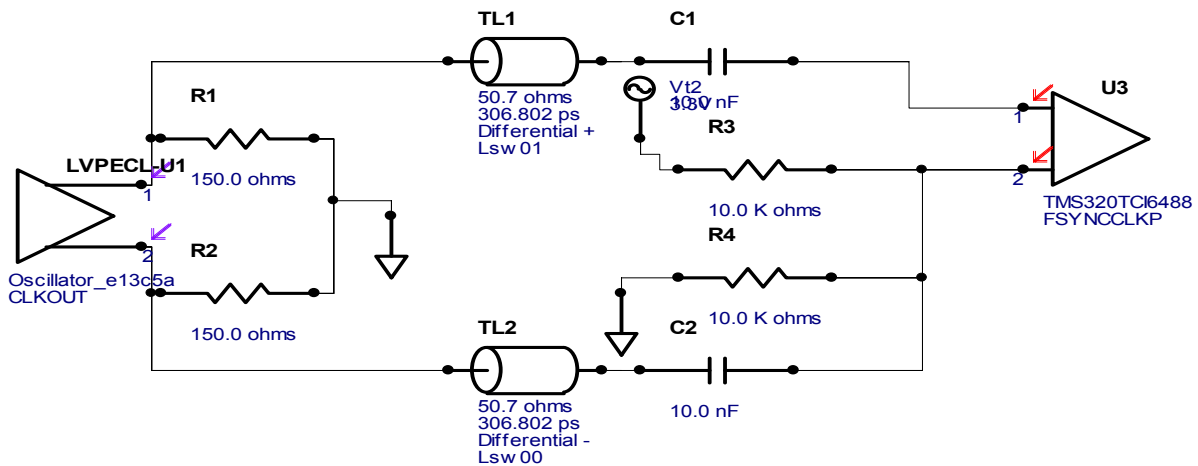
The use of two 10 KΩ resistors (pull up and pull down) creates a voltage divider on the negative differential input and allows for the DSP's common-mode (receiver) voltage to be set to 1.65 V. In [Figure 21](#) the preferred connection is shown. The simulation result for the following LVPECL → LVDS input is included in [Section 7](#), Simulation 18.

Figure 21 AC-Coupling (LVPECL (Clock) → LVDS (DSP)) - bias



In many cases the addition of the 10 KΩ pull up and pull down resistor is not required (depends on the DSP input IO buffer type and desired common mode input voltage). [Figure 22](#) illustrates the LVPECL → LVDS connection without the used of the added resistors. The simulation result for the following LVPECL → LVDS input (without biasing) is included in [Section 7](#), Simulation 19.

Figure 22 AC-Coupling (LVPECL (Clock) → LVDS (DSP))



When designing for a LVPECL to CML interface, the following connection (Figure 23 & Figure 24) schemes are recommended. The difference between the two schemes below is an additional series termination which is applied directly after the biasing resistor (refer to Figure 23 for designs without biasing resistors).

In all cases where the LVPECL clock output is greater than the DSP CML input the addition or the optional series resistors are required to properly attenuate the LVPECL clock source. For this reason and verified looking at the generated waveforms (Simulation 20 & 21) you can see the need for the added attenuation resistors.

Figure 23 AC-Coupling (LVPECL (clock) → CML (DSP)) A

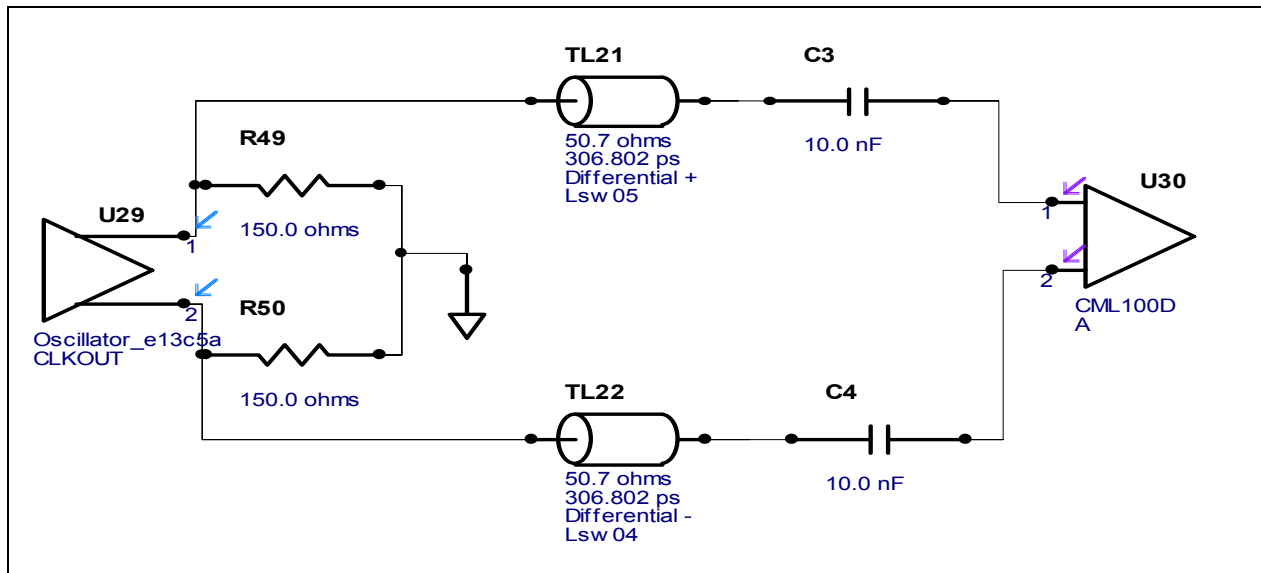


Figure 24 AC-Coupling (LVPECL (clock) → CML (DSP)) B

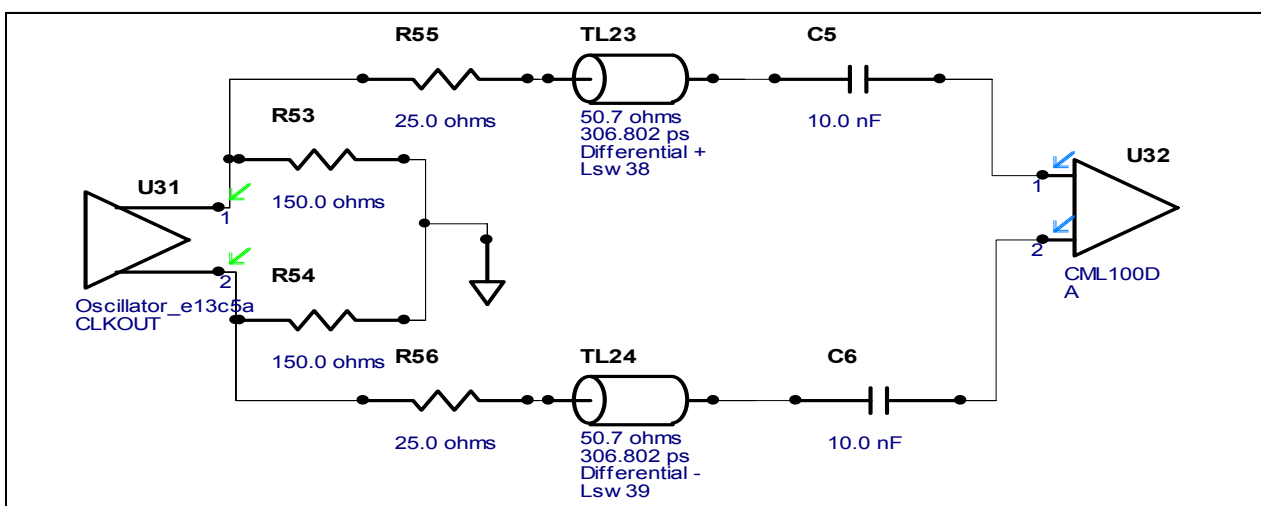
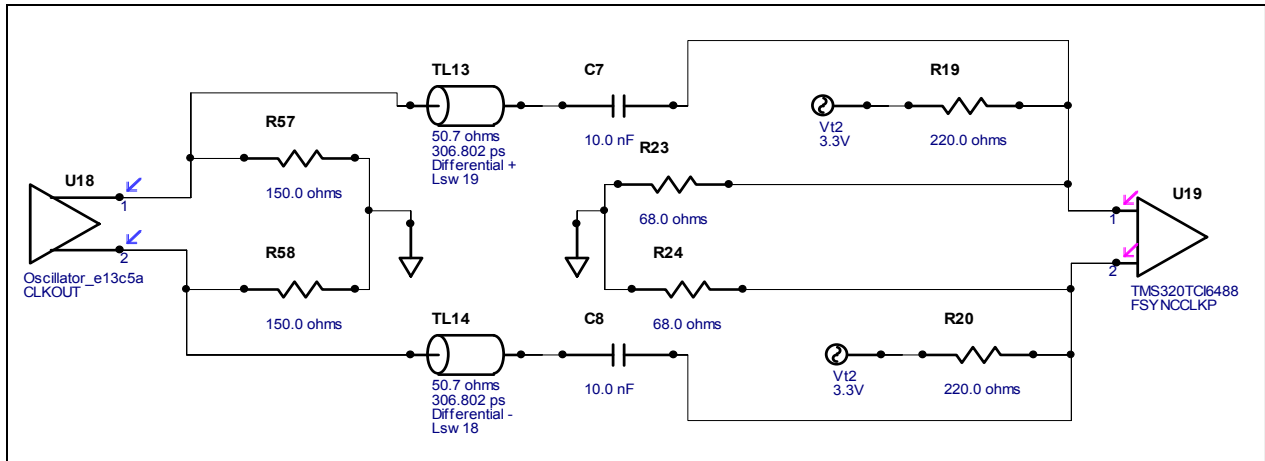


Figure 25 illustrates the proper connection for a LVPECL clock source to HSTL DSP input IO buffer. The simulation result for the following LVPECL → HSTL input is included in Section 7, Simulation 22. Proper selection of component values is mandatory.

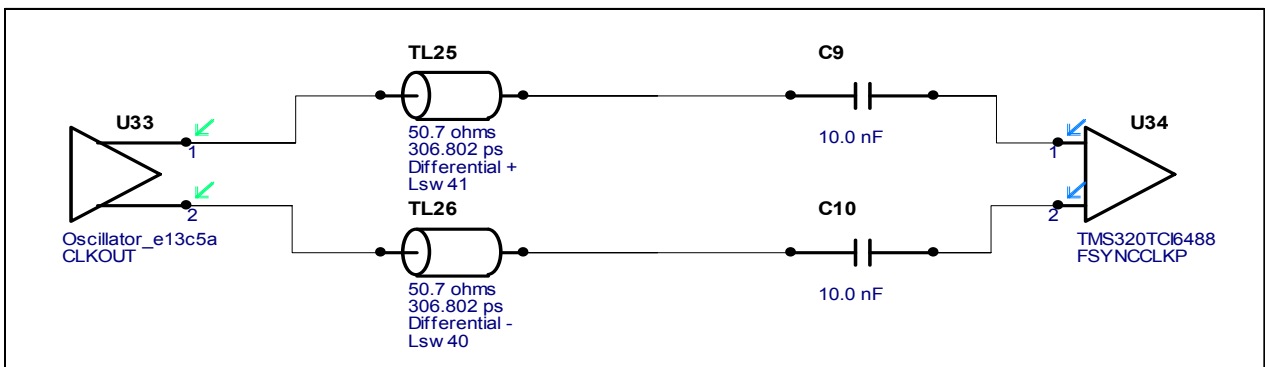
Figure 25 AC-Coupling (LVPECL (clock) → HSTL (DSP))



Note: For Vcc = 3.3 V, use R1 = 220, R2 = 68
 For Vcc = 2.5 V, use R1 = 167, R2 = 71
 For Vcc = 1.5 V, use R1 = R2 = 1000

When connecting an LVPECL clock source to a LCJB DSP input IO buffer(s), [Figure 26](#) denotes the recommended AC connection preferred. The simulation result for the following LVPECL → LJCB input is included in [Section 7](#), Simulation 23.

Figure 26 AC-Coupling (LVPECL (clock) → LCJB (DSP))



To properly size the AC termination capacitor the following formula should be used:

$$C \geq 1 / 2 * \text{Pi} * \text{System(impedance)} * (\text{FMHZ (clk input)} / 100) \geq \text{AC value}$$

For a 100MHz 50 Ω design the following AC termination is calculated:

$$C \geq 1 / 2 * \text{Pi} * \text{System}_{(\text{impedance})} * (\text{F}_{\text{MHZ (clk input)}} / 100) \geq \text{AC value}$$

$$C \geq 1 / 2 * \text{Pi} * 50 \Omega * (150\text{e}6 / 100) \geq \text{AC value}$$

$$C \geq 1 / 471.2389\text{e}6 \geq \text{AC value}$$

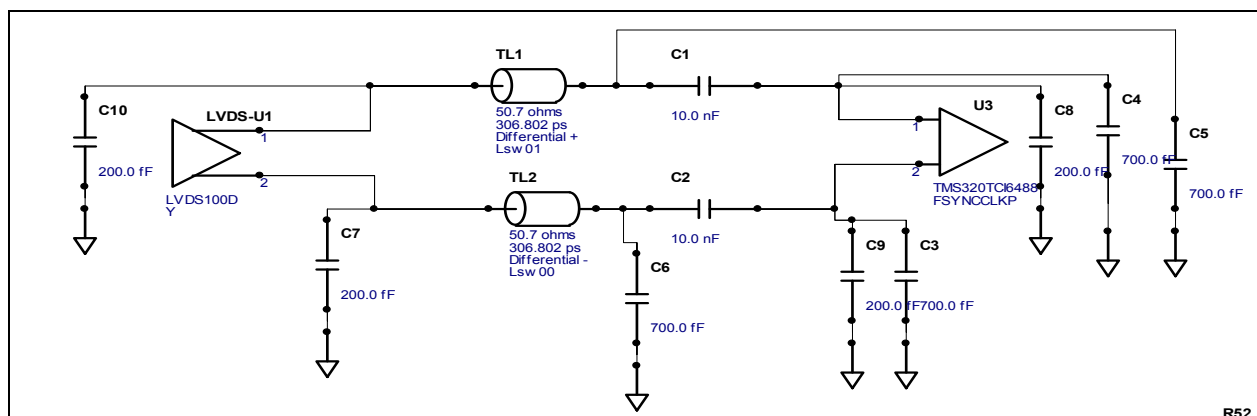
$$C \geq 2.1221\text{e-}9 \text{ (10 nF minimum is recommended)}$$

5.2.2 LVDS Clock Source – AC-Coupling

LVDS clock sources are differential by design and include two (2) outputs (+ & -). In most cases the DSP already will incorporate an internal 100 Ω termination resistor. Therefore, an external termination resistor between the two inputs is not required. In either case (external or internal 100 Ω termination) the common mode voltage should be around 1.2 V. If an external 100 Ω termination resistor is required it must be positioned as close to the DSP input pins as possible.

Figure 27 illustrates the proper connection for an LVDS clock source connected to an LVDS DSP input IO buffer. The simulation result for the following LVDS → HSTL input is included in Section 7, Simulation 24.

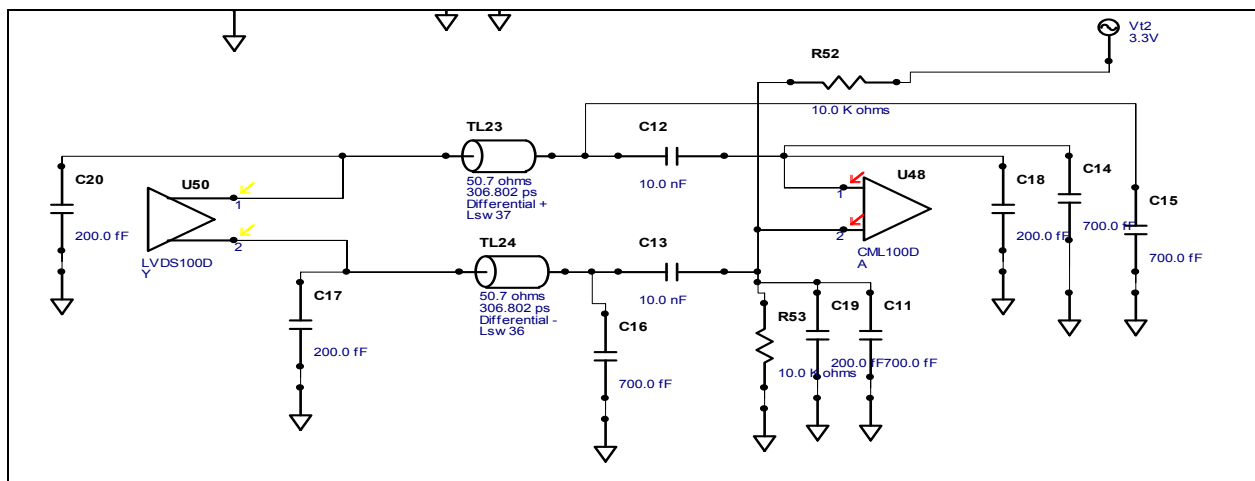
Figure 27 AC-Coupling (LVDS (clock) → LVDS (DSP))



When the DSP is supplied with an LVDS clock source and the DSP input is considered to be of the CML type (Figure 28) the use of two 10 KΩ resistors as illustrated below is recommended. These resistors properly set the DSP’s common-mode (receiver) voltage to be 1.65 V.

The simulation result for the following LVDS → CML input is included in Section 7, Simulation 25.

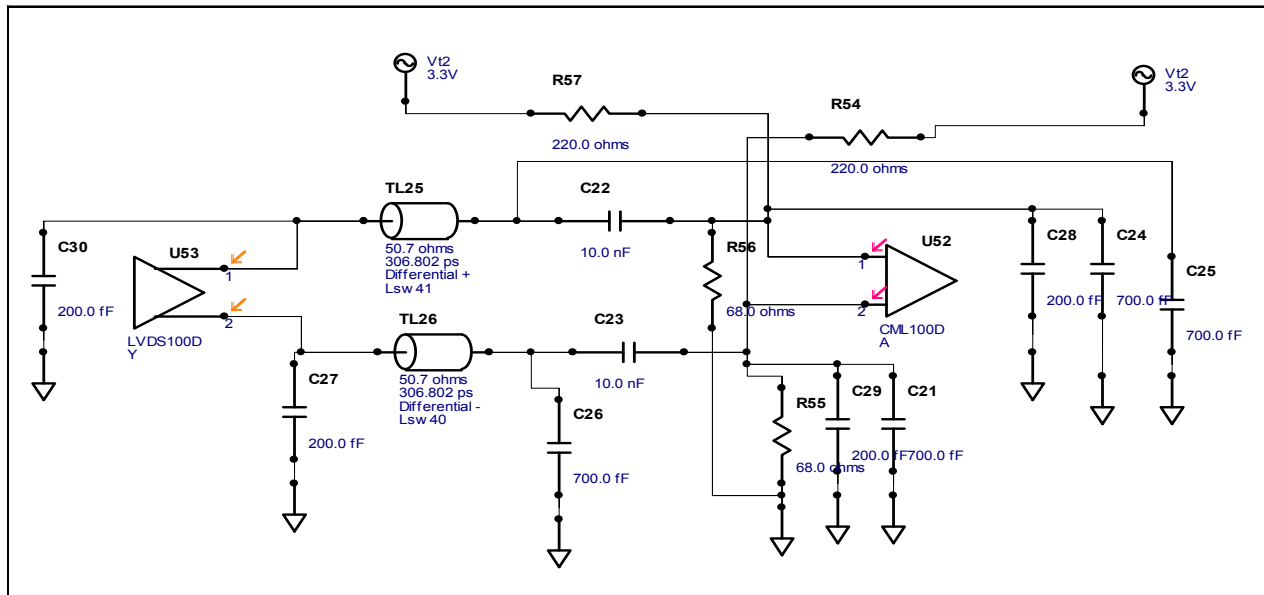
Figure 28 AC-Coupling (LVDS (clock) → CML (DSP))



As indicated by [Figure 29](#), when connecting between an LVDS clock source and HSTL input IO buffer it is necessary to level shift the input to the appropriate HSTL threshold levels. This is obtained by selecting the proper resistor divider network. The figure illustrates the proper connection for an HSTL input where Vcc is set to 3.3 V.

The simulation result for the following LVDS → HSTL input is included in [Section 7](#), Simulation 26.

Figure 29 AC-Coupling (LVDS (clock) → HSTL (DSP))



For other Vcc levels the following components can be selected:

- Where Vcc =
- 3.3 V: R54 & R57 = 220 Ω and R55 & R56 = 68 Ω
 - 2.5 V: R54 & R57 = 167 Ω and R55 & R56 = 71 Ω
 - 1.5 V: R54 & R57 = 1.0K Ω and R55 & R56 = 1.0K Ω

5.2.3 CML Clock Source – AC-Coupling

The CML clock sources typically provide for important features including adjustable output logic swing, high-speed capabilities, level adjustment, and slew rate adjustment. Most CML clock sources incorporate an open-drain differential output pair (+ & -) and require pull up resistors to Vdd (output transistors can only drive on falling edges and pull ups are required to allow the output to drive on rising edges).

[Figure 30](#) illustrates the recommended connection between a CML clock source and an LVDS DSP input IO buffer(s). The simulation result for the following CML → LVDS input is included in [Section 7](#), Simulation 27. AC-Coupling is required when output CML common mode level differs from LVDS common mode input range.

Figure 30 AC-Coupling (CML (clock) → LVDS (DSP))

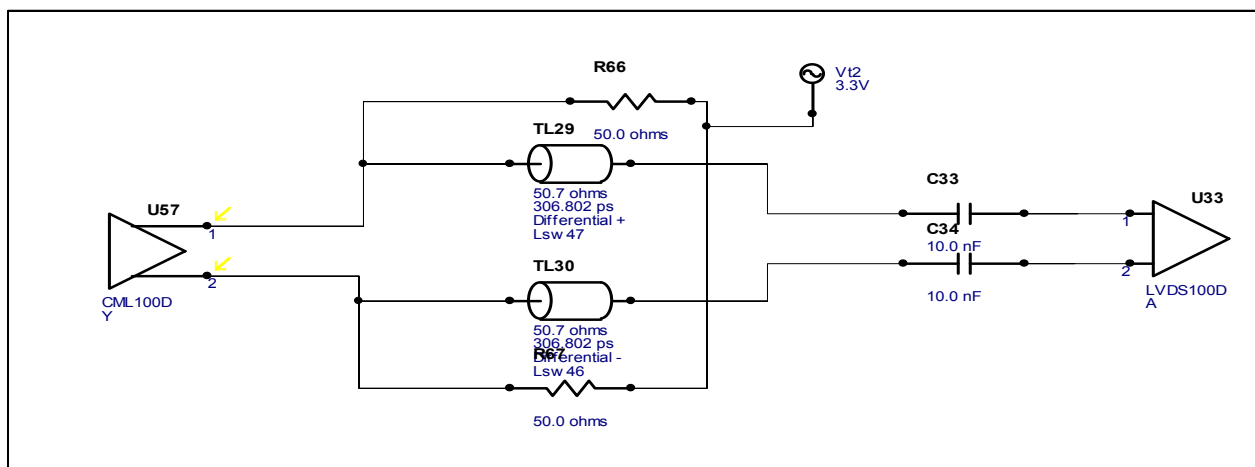
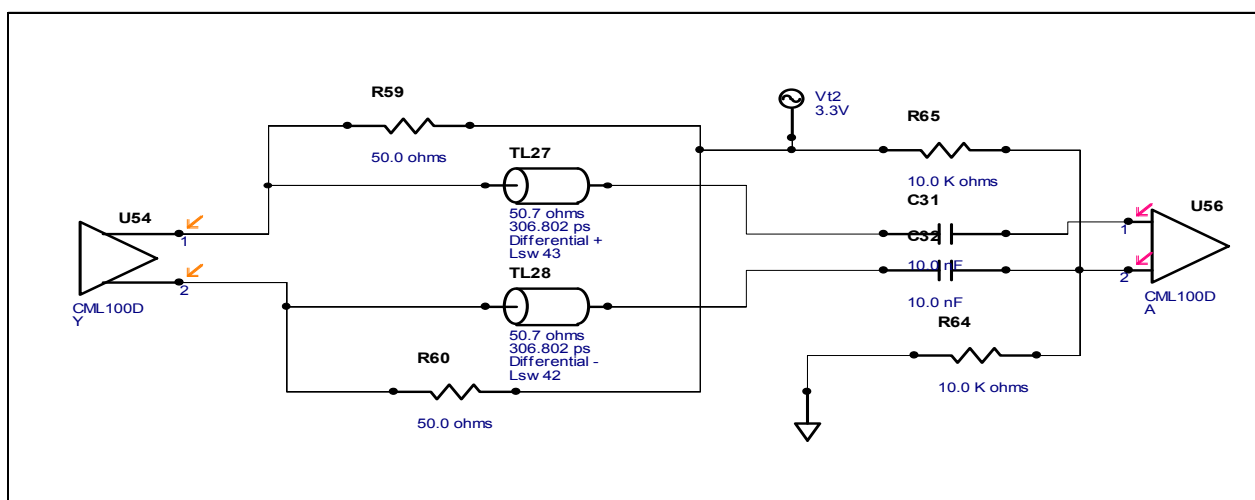


Figure 31 denotes the recommended connection between a CML clock source and a CML DSP input IO buffer. The simulation result for the following CML → LVDS input is included in Section 7, Simulation 28.

Figure 31 AC-Coupling (CML (clock) → CML (DSP))



In the event the CML clock source and DSP (clock input) have different vdd levels, it may be necessary to supply additional pull-up resistors connected to the DSP Vdd rail (voltage where Vdd is set to the DSP common mode input voltage).

Figure 32 illustrates the suggested connection between a CML clock source and an LVDS DSP input IO buffer when level shifting is required (to 3.3 V). The simulation result for the following CML → LVDS input is included in Section 7, Simulation 29.

Figure 32 AC-Coupling (CML (clock) → LVDS (DSP)) – 3.3 V

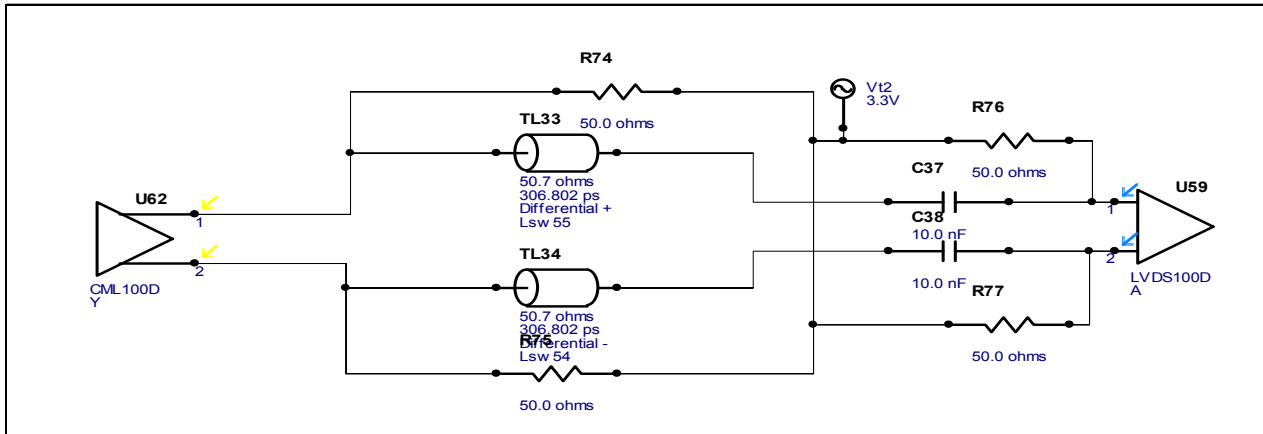
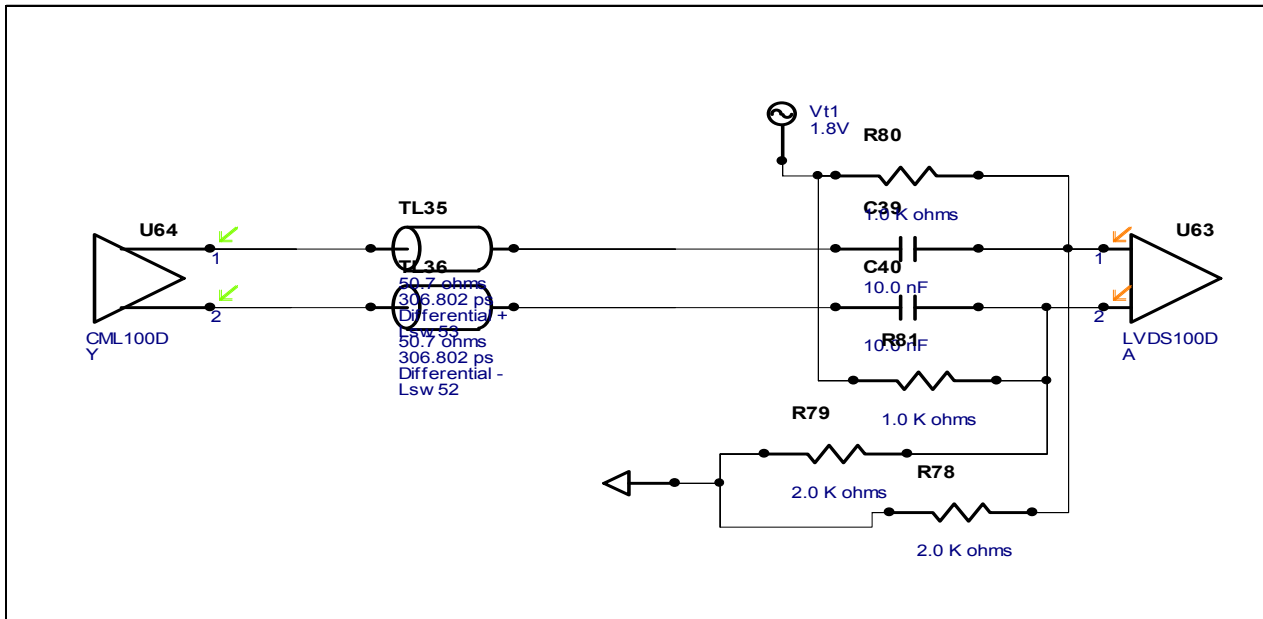


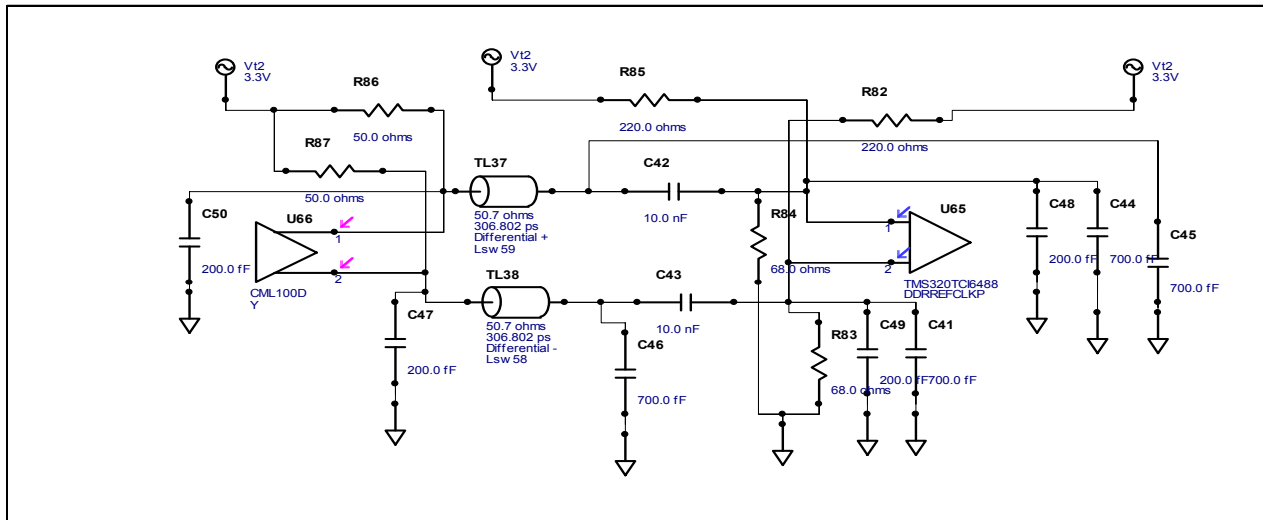
Figure 33 illustrates the suggested connection between a CML clock source and an LVDS DSP input IO buffer when level shifting is required (to 1.8 V). The simulation result for the following CML → LVDS input is included in Section 7, Simulation 30.

Figure 33 AC-Coupling (CML (clock) → LVDS (DSP)) – 1.8 V



When connecting between a CML clock source and HSTL DSP input IO buffer the Figure 34 method is recommended. The simulation result for the following CML → HSTL input is included in Section 7, Simulation 31.

Figure 34 AC-Coupling (CML (clock) → HSTL (DSP))



5.2.4 HSTL Clock Source – AC-Coupling

Figure 35 illustrates the recommended method for connecting between an HSTL clock source and LVDS DSP input buffer. The simulation result for the following HSTL → LVDS in the following figure is included in Section 7, Simulation 32.

Figure 35 AC-Coupling (HSTL (clock) → LVDS (DSP))

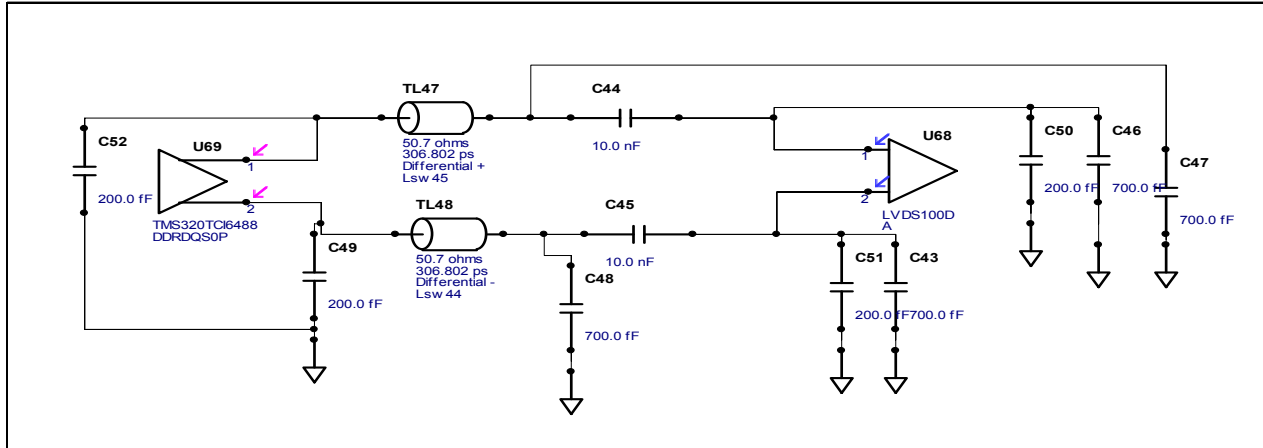


Figure 36 illustrates the preferred connection between an HSTL clock source and a CML DSP input IO buffer. The simulation result for the following HSTL → CML input is included in Section 7, Simulation 33.

Figure 36 AC-Coupling (HSTL (clock) → CML (DSP)) – 3.3 V

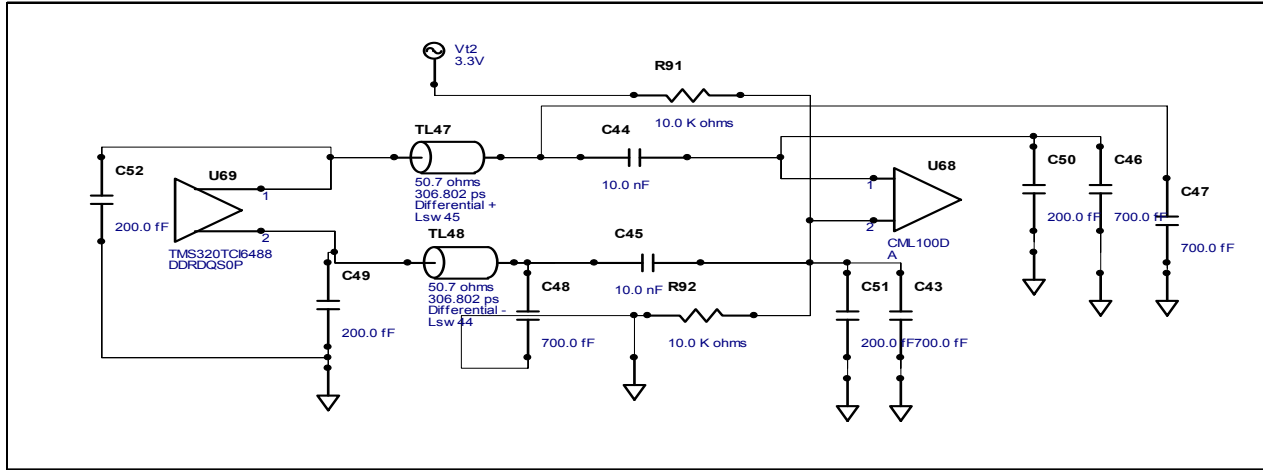
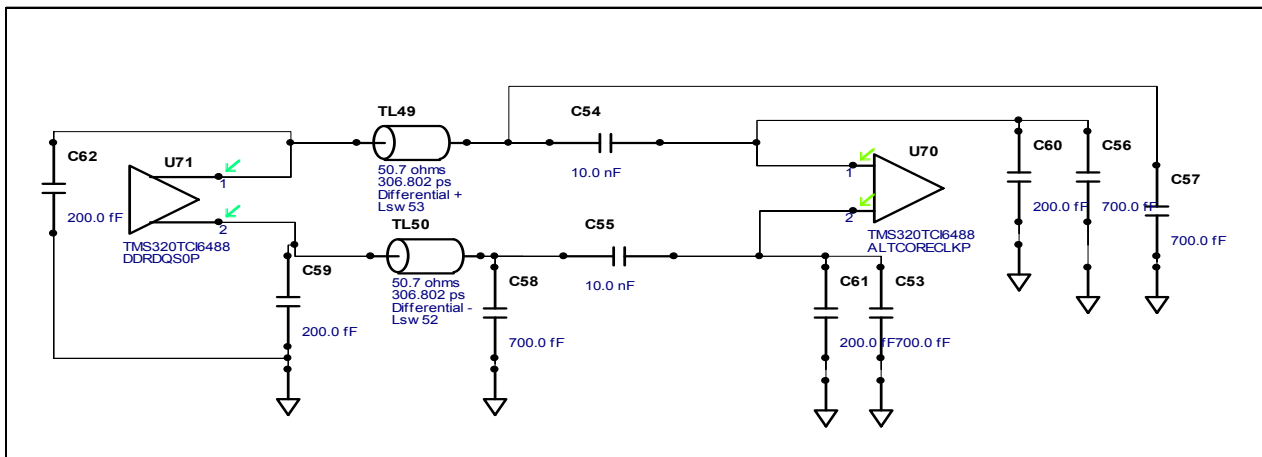


Figure 37 illustrates a method to connect between an HSTL clock source and an HSTL DSP input IO buffer.

Figure 37 AC-Coupling (HSTL (clock) → HSTL (DSP))

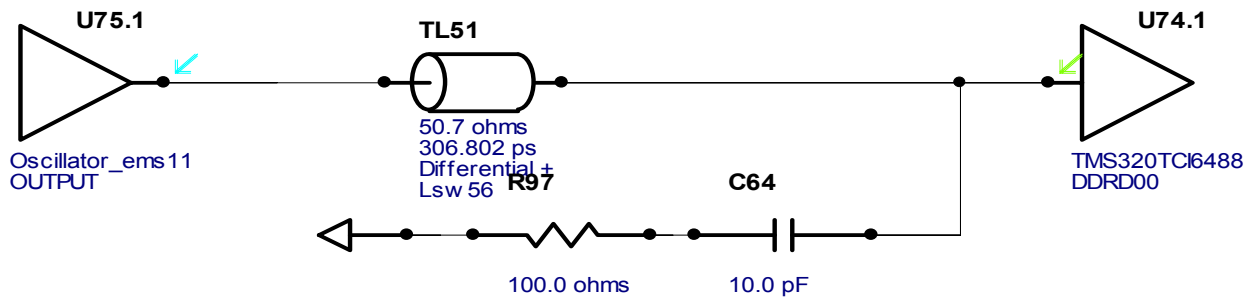


5.2.5 LVTTTL / CMOS Clock Source – AC-Coupling

When using a LVTTTL (or CMOS) single-ended clock source it is mandatory that the output of the clock source be of the correct voltage level (e.g., a 1.8 Vdc DSP input clock buffer will not functional properly when supplied with a 3.3 V or 5.0 V clock source). Improper voltage levels to the DSP may affect its reliability and will void all DSP warranties.

Figure 38 illustrates the recommended connection between a single-ended LVTTL / CMOS clock source and a single ended LVTTL / CMOS DSP input IO buffer by using an AC termination. Proper sizing of the discrete components is important; refer to the section on simulation and modeling and component selection for additional information. The simulation result for the following LVTTL / CMOS → LVTTL / CMOS input is included in Section 7, Simulation 34.

Figure 38 AC-Coupling (LVTTL (clock) → LVTTL/CMOS – AC Termination (DSP))



6 Assembly Considerations

The following subsection provides a brief description of relevant issues to consider when designing the application board. This is not a totally inclusive list of issues to consider and should not be the only single guideline used.

6.1 Routing

Component placement and signal or trace routing, commonly referred to as *board topology* plays a major, if not the most important, role on performance of a clocking system.

6.1.1 Component Placement

Key component placement concepts must take into account the termination method selected. Important facts to consider include the following points as illustrated in Figures 3 through 38. Comments below apply in general except where noted.

Factors to consider include:

- Series termination placement – Performance is impacted by reflections and slew rates, termination placement within the transmission line should always be modeled for verification. If modeling tools are not available basic calculations for propagation delays should be performed to verify that any induced reflection will not occur within the logic switching regions. As a rule of thumb, AC-Coupling capacitors must be placed in close proximity to the respective pins on the DSP.
- Differential termination placement – The individual series termination placement in a differential configuration should be identical. Mismatching the placement of terminations in this configuration can create a potentially unbalanced differential signal at the destination end (DSP).
- Biasing and voltage divider component placement – The use of biasing or voltage divider components induces stubs in the clock line; these stubs should be minimized or eliminated where possible. Clock source biasing and clock source voltage divider components should be placed as close to the clocking source as possible. Conversely, DSP clock input buffer biasing and DSP input buffer voltage divider components should be placed as close to the DSP pin as possible.
- Length of trace – All signal routes should be as short as possible, differential signals should be matched. Each pull-up and pull-down component tied to its respective ground or power rail ideally would have a zero trace length (pad tied directly to the respective plane). If a trace is required, it should be extremely short and as wide as possible.
- Spacing – Single-ended traces, especially those of the high-speed type, should be spaced properly from other signals to avoid coupling. Differential traces should have proper line-to-line spacing. An increase in the separation between parallel traces reduces the coupling effects. In microstrip designs, coupling is a linear function to spacing. In a stripline configuration, coupling is approximately a square function of spacing. Minimal line-to-line separation can account for a two- to four-fold reduction in potential crosstalk.
- Skew – Complementary differential traces must be skew matched. Traces that comprise a bus (EMIF, DDR, HPI, etc.) should be skew matched to minimize the impact on timing performance.

Simulation examples (Section 7) number 13 – 15 are provided as an example of the potential impact on a single termination placement in three different transmission line locations.

6.2 Application Board (PCB) Layers

Different applications dictate different layer design (stack up). Most HPMP application boards range between 10 and 18 layers. Choice of signal routing layers can impact single quality, skew, and propagation delays.

Differential signals must always be routed on the same layer. Criteria for determining whether the clock signals are routed on an internal layer (strip line) or external layer (micro strip) depend on the application and requirements. If propagation, visibility, accessibility, or timing is a major concern, then remember that signals routed on an outer layer (micro strip) travel a bit faster than signals routed on an inner layer (strip line). If noise immunity or noise susceptibility is a concern, then a strip line (internal trace) buried between parallel power and ground planes would be the proper choice. If signal integrity or performance is the criteria, then either is acceptable provided proper spacing is maintained, and the impact of parasitics minimized (vias, stubs, coupled components).

6.3 Application Board (PCB) Stack up / impedance

Key factors to remember and observe when designing an application board with regards to layer stack up include the following:

- Characteristic Impedance – System impedance for most clock sources and DSPs is 50 Ω . This impedance is critical to the performance of the DSP system and should always be maintained. An increased PCB impedance (e.g., 65 Ω) reduces propagation delays (speeds the signal up) whereas a decreased PCB impedance (e.g., 30 Ω) increases propagation delays (slows the signal down) in the system. In both cases the impedance mismatch generates added reflections and timing anomalies that can be detrimental to the design.
- Symmetrical Stack up – A symmetrical stack up is important when designing and laying out the application board. Proper symmetry (stack up) assures minimal warpage, proper impedance, and reduces radiation. Proper stack up should be symmetrical, that is mirrored midpoint to top layer and midpoint to bottom layer. Signal routing layers (except for the top and bottom layers) should be routed between alternating ground layers, and each routing layer (signal layer) should be adjacent to a power or ground plane. A typical 14-layer (6 routing layers) stack up would be:
 - S – Signal / Routing (top layer)
 - G – Ground plane
 - S – Signal / Routing (internal layer)
 - S – Signal / Routing (internal layer)
 - G – Ground plane
 - S – Signal / Routing (internal layer)
 - P – Power plane
 - P – Power plane
 - S – Signal / Routing (internal layer)
 - G – Ground plane
 - S – Signal / Routing (internal layer)
 - S – Signal / Routing (internal layer)
 - G – Ground plane
 - S – Signal / Routing (bottom layer)

- **Thickness** – Proper PCB thickness is important. Many application boards range from 0.0625 (1.6mm) to 0.125 (3.175mm) depending on applicable standards and end use. Verify your end use application requirements.
- **Power Planes** – As indicated above, the stack up must contain separate power planes (as opposed to split power/signal planes) and these planes should be closely coupled together. The greater number of adjacent ground planes (ground layers) the lower the ground impedance will be which will lower the common-mode radiation.

6.4 Application Board (PCB) Vias (number and size)

With today's DSP and clocking technologies and the added complexity and density of application hardware it is almost impossible to design, layout, and route clock signals on multilayered boards without the addition of multiple vias.

Unless the clock source and DSP are on opposite sides of the PCB, a minimum of two vias is required. Vias can be of two types (more exist but are less common): blind and through-hole. Blind vias are typically reserved for internal signal layer connections whereas through-hole vias are typically larger and used for mating components on opposite sides of the board to one another.

Vias, regardless of size act as an additional load on the clock signal and depending on size can add between 50 fF (0.05 pF) to 3 pF additional loading to the clock source. An additional load of this magnitude can render the clock (source) waveform useless (refer to simulations).

In order to understand the impact a via will have on the signal path (as a load) the following formula is provided to calculate the effective capacitance:

$$C = 1.41 * \epsilon_r * d1 * t / (d2 - d1) \text{ (pF)}$$

Where

ϵ_r = relative dielectric constant
 d1 = via pad diameter (in.)
 d2 = via antipad diameter (in.)
 t = board thickness (in.)

example #1: $\epsilon_r = 4.3$; $d1 = 0.020''$; $t = 0.0625''$ $d2 = 0.028''$

$$C = 1.41 * \epsilon_r * d1 * t / (d2 - d1)$$

$$C = 1.41 * 4.3 * 0.020 * 0.0625 / (0.028 - 0.020)$$

$$C = 1.41 * 4.3 * 0.020 * 0.0625 / (0.028 - 0.020)$$

$$C = 7.57875e-3 / (0.008)$$

$$C = 0.94734 \text{ pF (947 fF)}$$

example #2: $\epsilon_r = 4.3$; $d1 = 0.036''$; $t = 0.0625''$ $d2 = 0.044''$

$$C = 1.41 * \epsilon_r * d1 * t / (d2 - d1)$$

$$C = 1.41 * 4.3 * 0.036 * 0.0625 / (0.044 - 0.036)$$

$$C = 1.41 * 4.3 * 0.036 * 0.0625 / 0.008$$

$$C = 13.64175e-3 / 0.008$$

$$C = 1.705 \text{ pF (1705 fF)}$$

6.5 Component selection

The most important factors to remember when selecting active and passive components for the clocking system include jitter, duty cycle distortion, clock output level, thermal limitations and response, and form factor. Regarding discrete components, it is advisable that each be as small a form factor as possible (typically 0402 size or smaller). Larger components tend to have significantly different parasitics that will have a greater impact the higher the frequency.

7 Simulation

Simulation and modeling, along with good engineering practices are the keys to a successful design. Several tools exist that are currently available and well suited for this type of exercise. The most current form of circuit simulation is performed using IBIS. IBIS traditionally works well for most high speed signals (up to 200 – 300 MHz), beyond this IBIS v5 models or hspice models would be required. The following subsections illustrate the simulation results for various DC and AC coupling methods identified in [Section 4](#) and [Section 5](#).

7.1 DC-Coupling

The following section provides a comprehensive analysis of various DC-Coupling schemes when simulated to illustrate the functionality of each. Each of the following figures contain both individual input and output (clock source and DSP destination) wave forms.

7.1.1 LVPECL Clock Source → DSP

[Figure 39](#) illustrates the simulation of the recommended LVPECL → LVDS DSP input. In the following figure the purple waveform represents the output from the LVPECL oscillator whereas the red waveform represents the input to the DSP.

Single best method of validating a design prior to fabrication and assembly of physical hardware.

Figure 39 Simulation 1: [DC Simulation] - LVPECL (Clock) → LVDS (DSP)

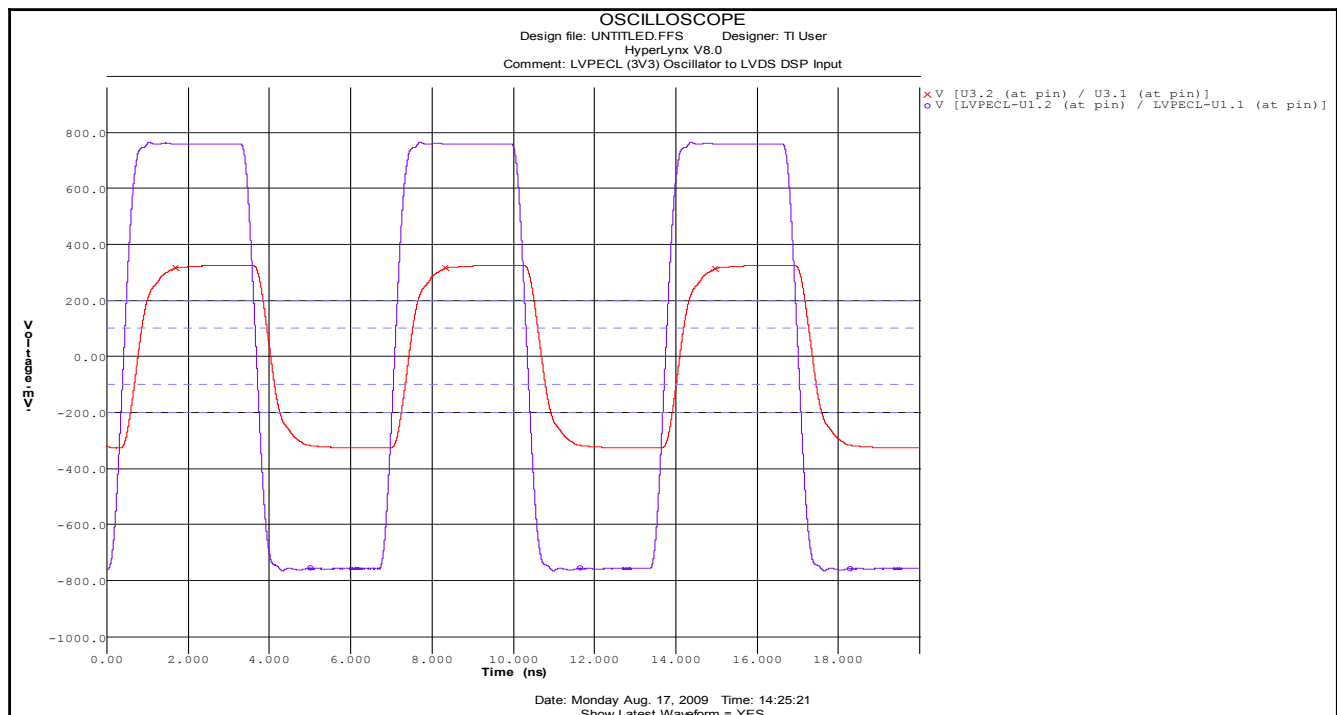


Figure 40 (Simulation 2) denotes the simulation results for the recommended LVPECL → LVDS Clock buffer → multiple DSPs attached.

Figure 40 Simulation 2: [DC Simulation] - LVPECL (Clock) → LVDS Buffer → Multiple DSP

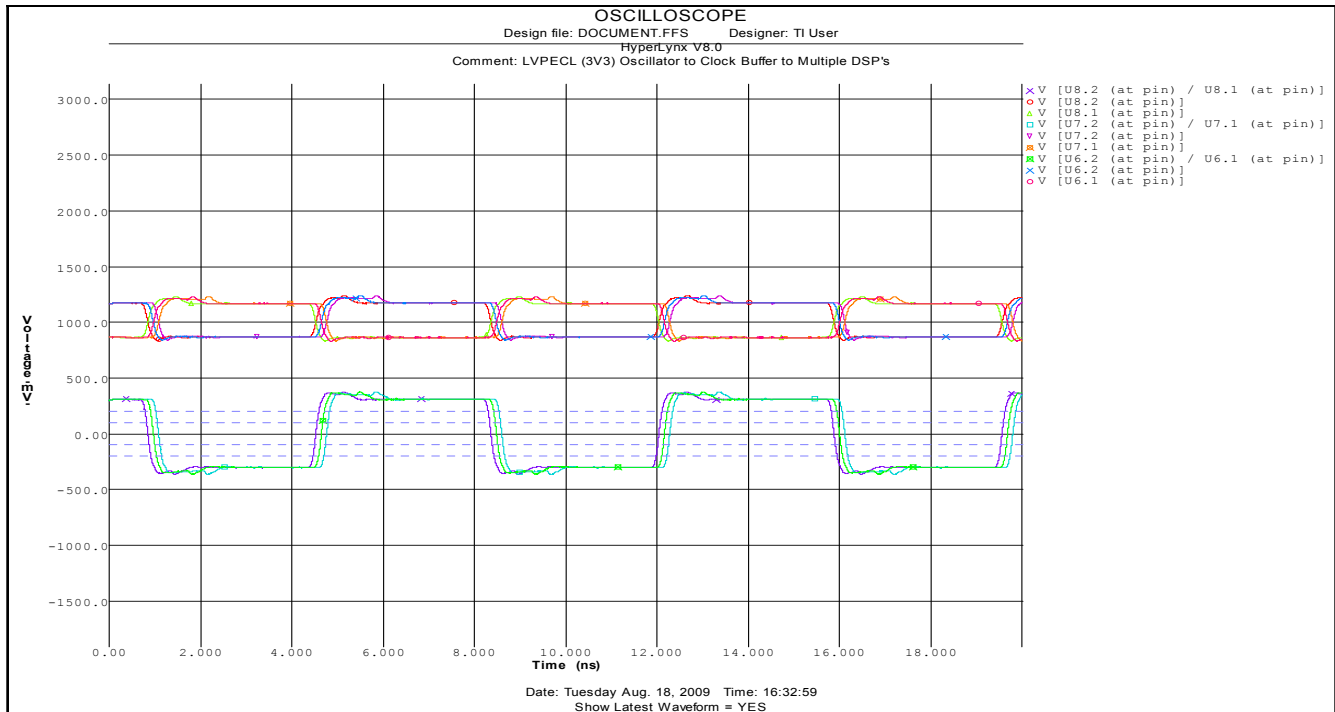


Figure 41 (Simulation 3) denotes the simulation results for the recommended LVPECL → CML DSP configuration.

Figure 41 Simulation 3: [DC Simulation] - LVPECL (Clock) → CML (DSP)

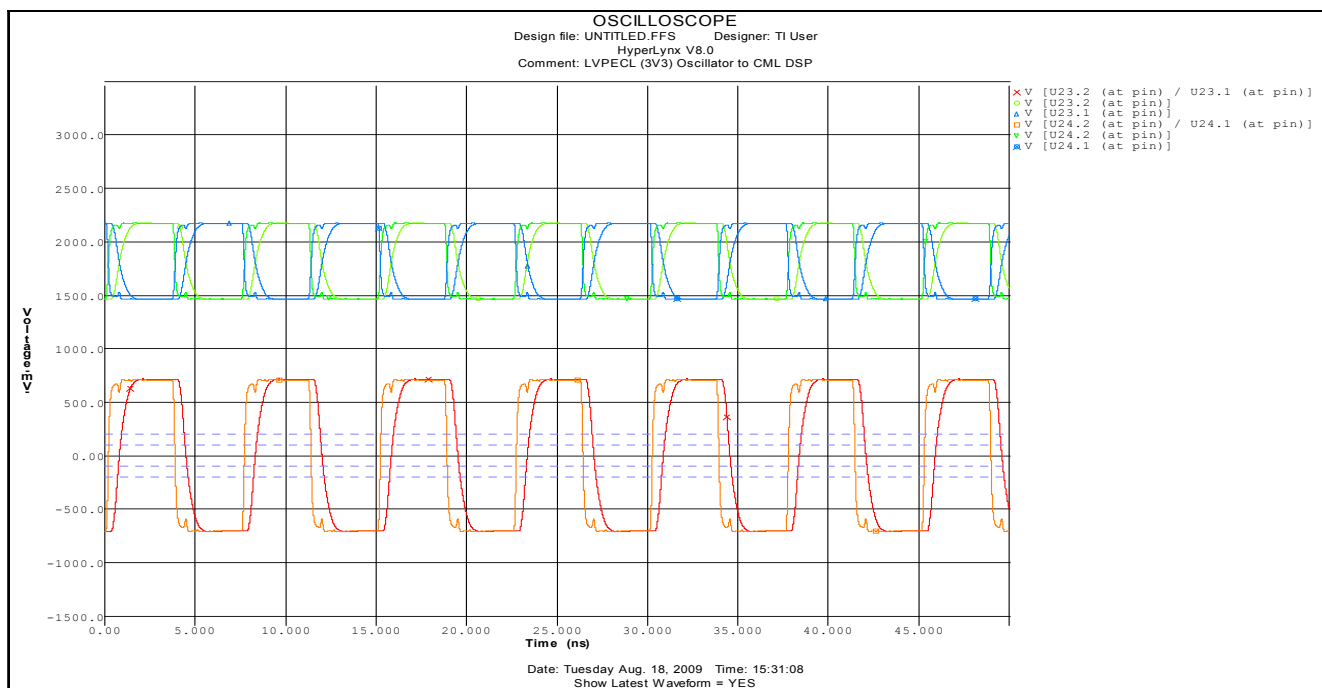
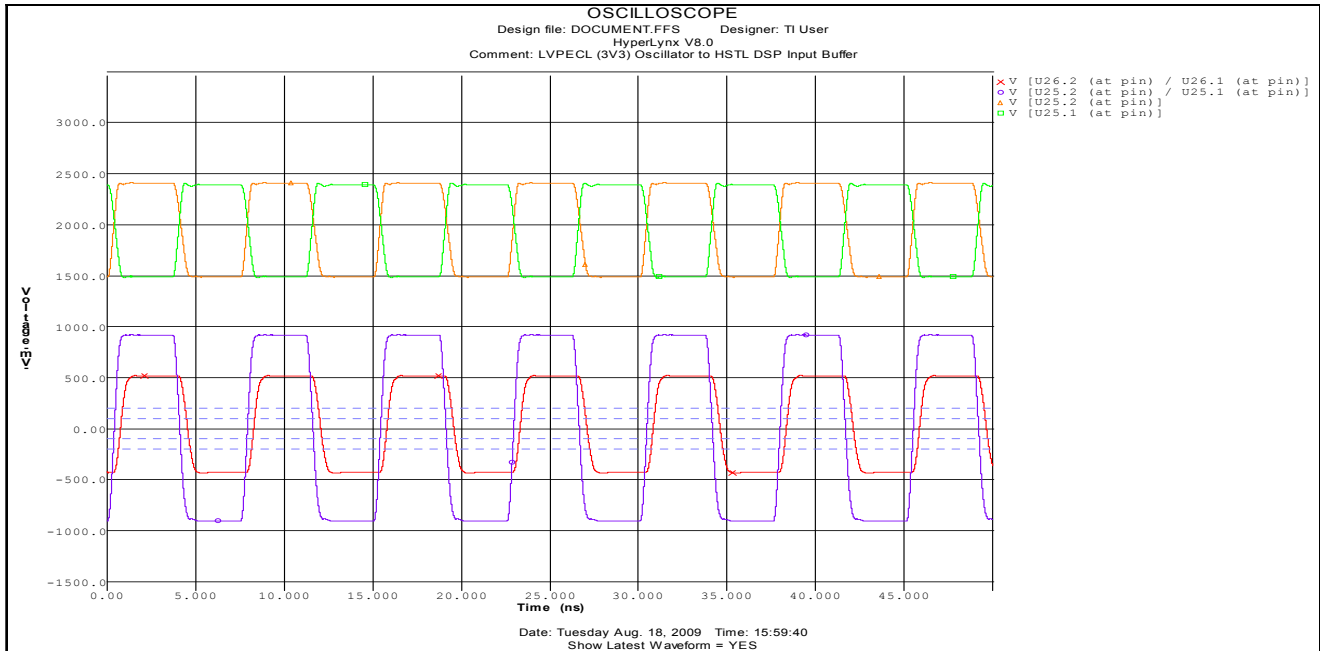


Figure 42 (Simulation 4) denotes the simulation results for the recommended LVPECL → HSTL DSP configuration.

Figure 42 Simulation 4: [DC Simulation] - LVPECL (Clock) → HSTL (DSP)



7.1.2 LVDS Clock Source → DSP

Figure 43 (Simulation 5) denotes the simulation results for the recommended LVDS → LVDS DSP configuration.

Figure 43 Simulation 5: [DC Simulation] - LVDS (Clock) → LVDS (DSP)

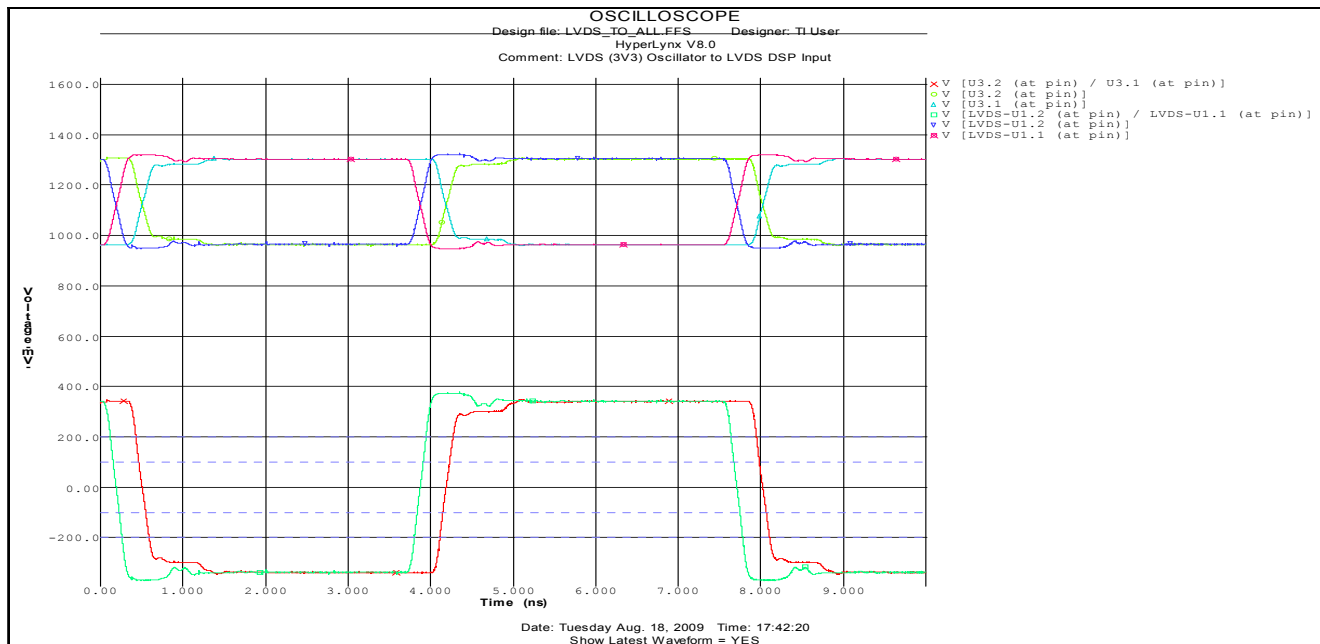


Figure 44 (Simulation 6) denotes the simulation results for the recommended LVPECL → CML DSP configuration.

Figure 44 Simulation 6: [DC Simulation] - LVDS (Clock) → CML (DSP)

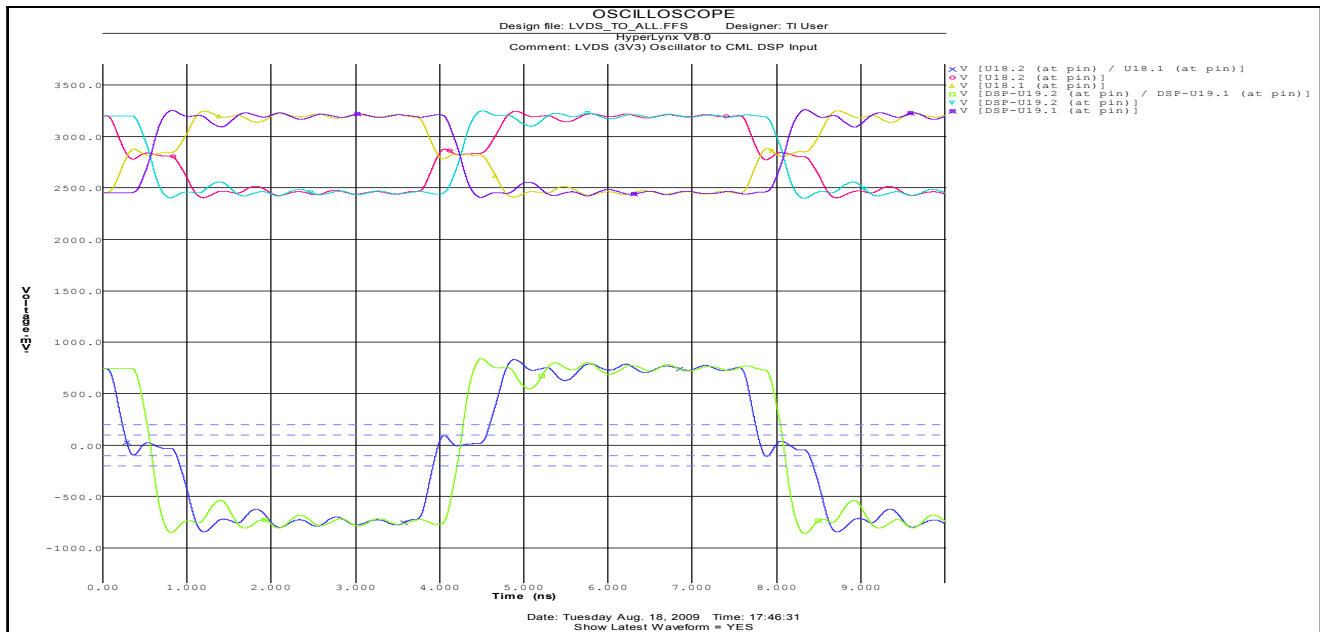
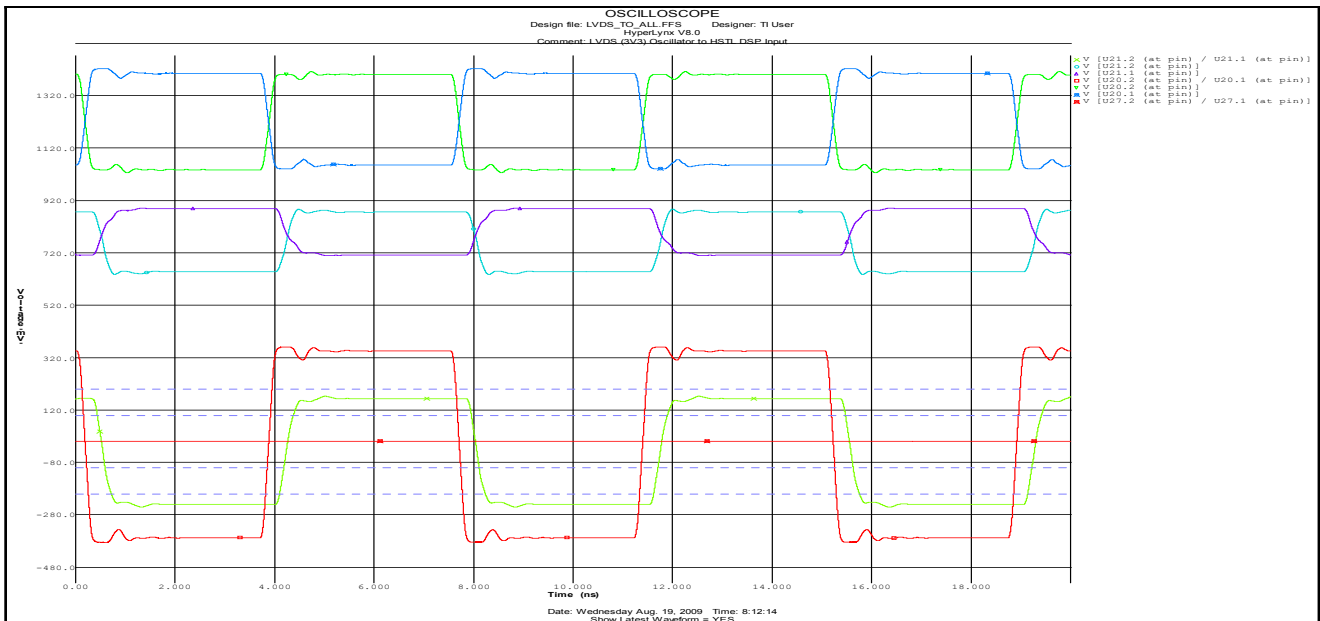


Figure 45 (Simulation 7) denotes the simulation results for the recommended LVDS → HSTL DSP configuration.

Figure 45 Simulation 7: [DC Simulation] - LVDS (Clock) → HSTL (DSP)



7.1.3 CML Clock Source → DSP

Figure 46 (Simulation 8) denotes the simulation results for the recommended CML → LVDS DSP configuration.

Figure 46 Simulation 8: [DC Simulation] - CML (Clock) → LVDS (DSP)

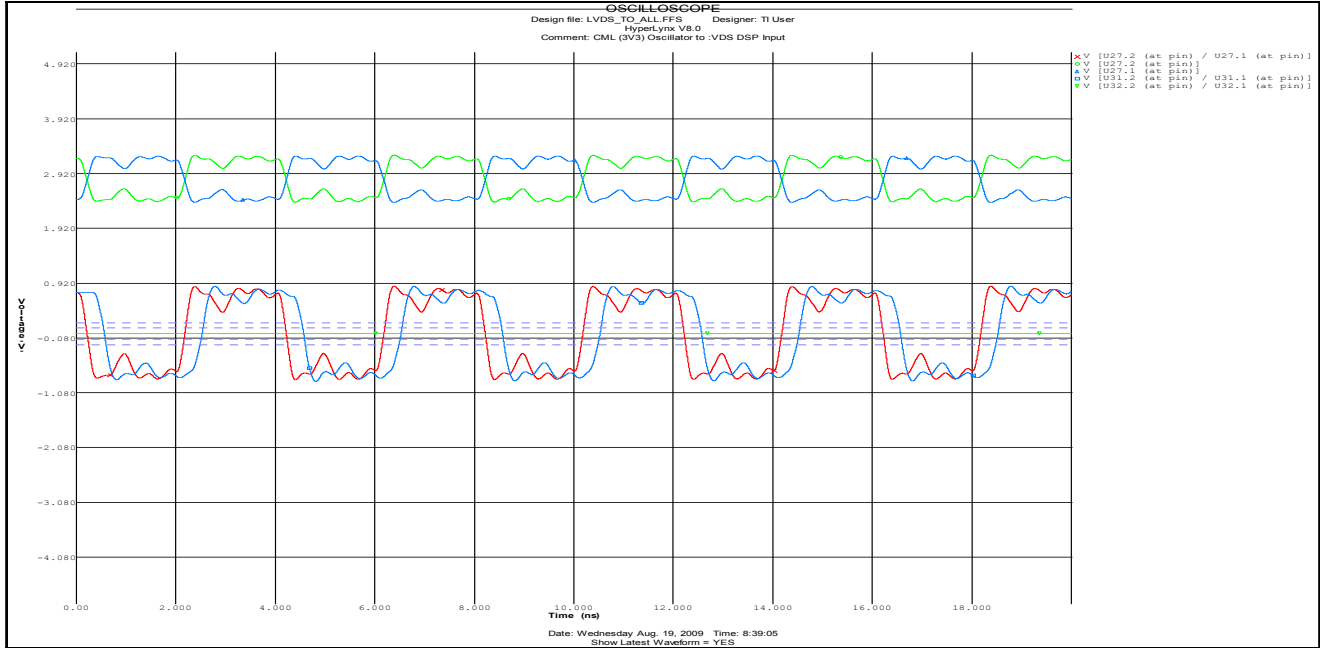


Figure 47 (Simulation 9) denotes the simulation results for the recommended CML → CML DSP configuration.

Figure 47 Simulation 9: [DC Simulation] - CML (Clock) → CML (DSP)

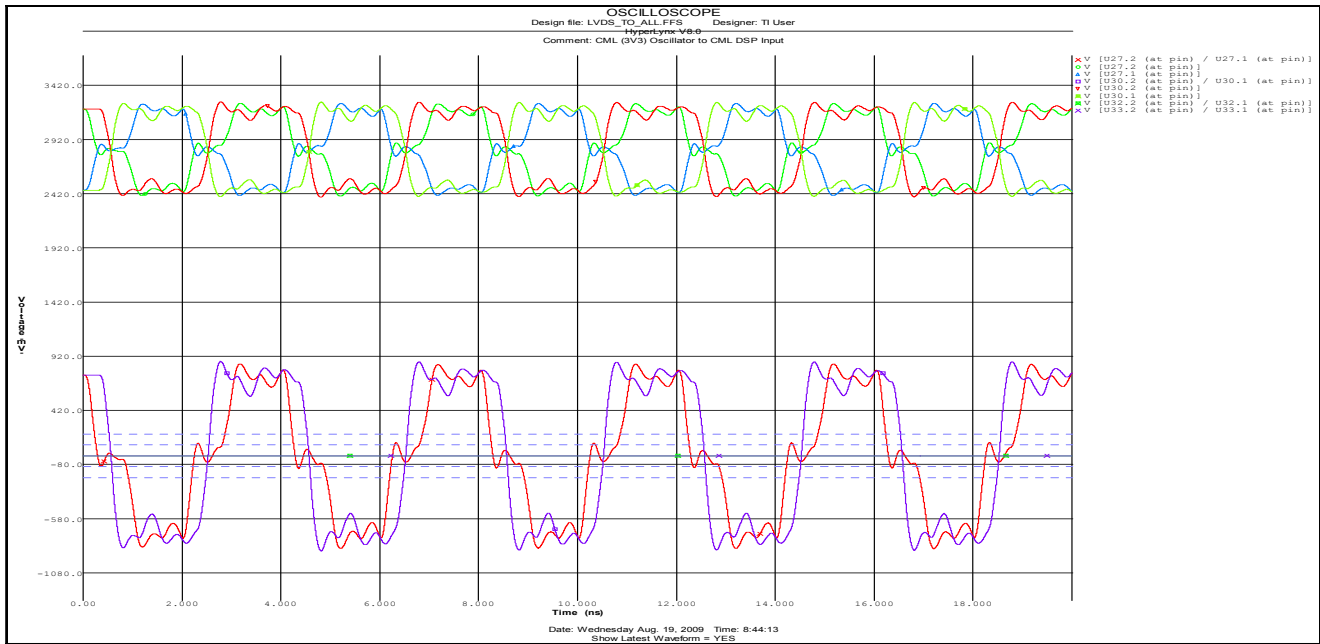
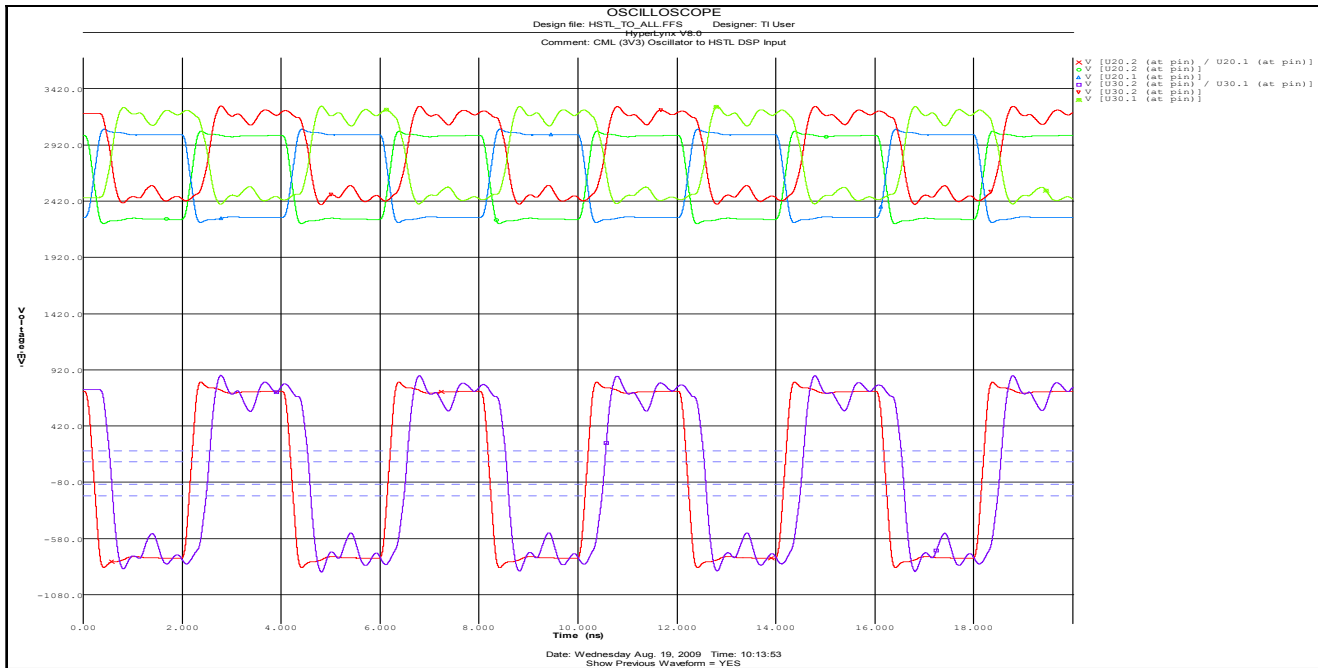


Figure 48 (Simulation 10) denotes the simulation results for the recommended CML → HSTL DSP configuration.

Figure 48 Simulation 10: [DC Simulation] - CML (Clock) → HSTL (DSP)



7.1.4 HSTL Clock Source → DSP

Figure 49 (Simulation 11) denotes the simulation results for the recommended HSTL → HSTL DSP configuration.

Figure 49 Simulation 11: [DC Simulation] - HSTL (Clock) → HSTL (DSP)

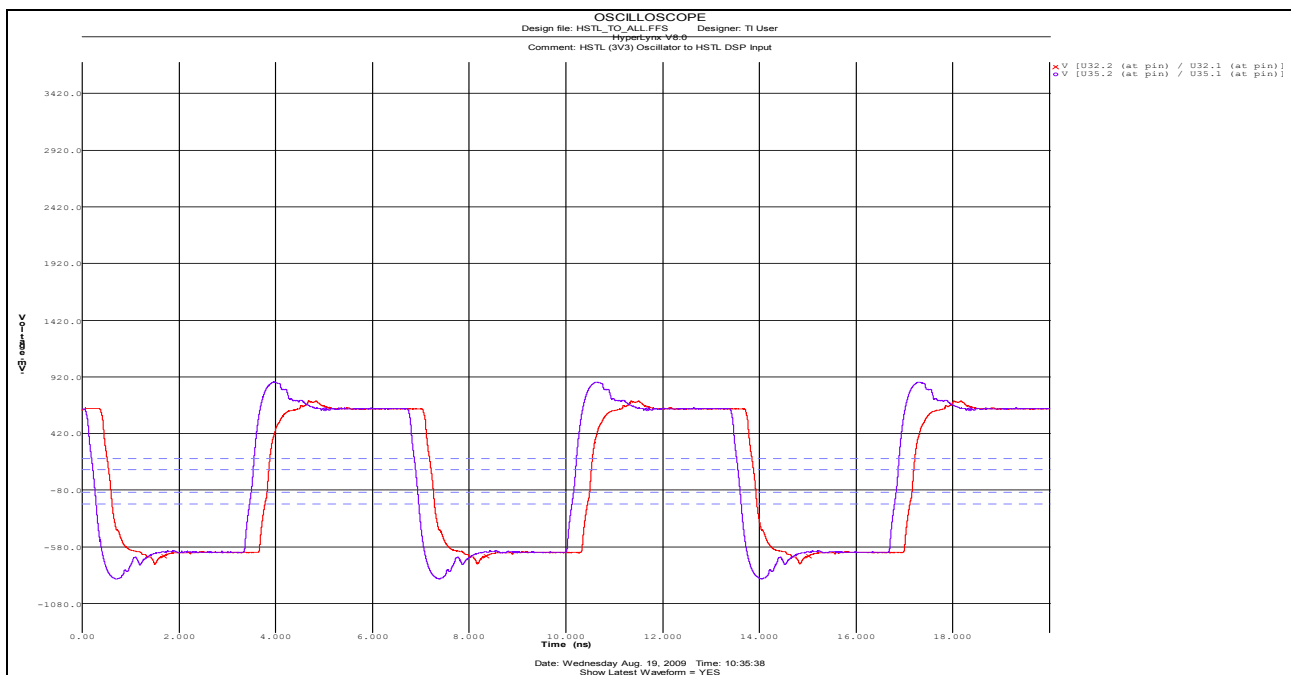
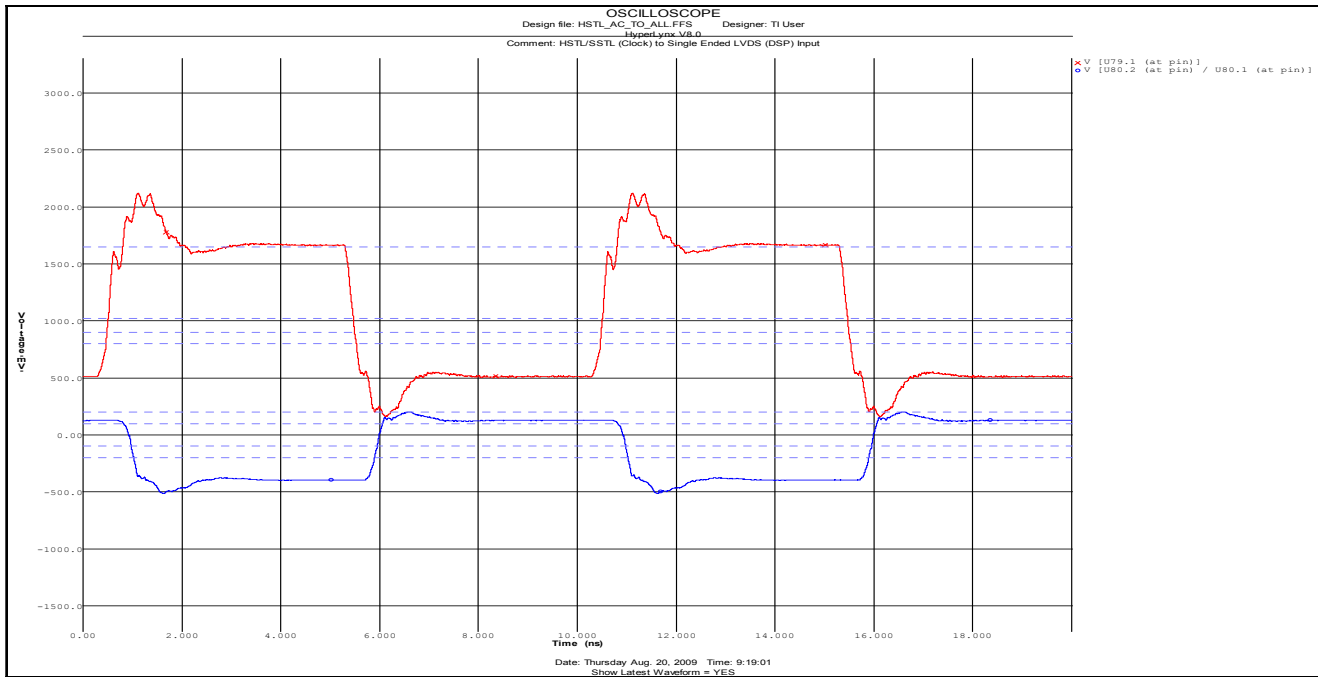


Figure 50 (Simulation 12) denotes the simulation results for the recommended HSTL → LVDS DSP configuration.

Figure 50 Simulation 12: [DC Simulation] - HSTL (Clock) → Single Ended LVDS (DSP)



7.1.5 LVTTTL Single Ended Clock Source → DSP

Figures 51, 52, and 53 (Simulation 13-15) denote a single ended LVTTTL / LVCMOS clock source connected to a single-ended DSP input buffer. The difference between the following three waveforms is the termination placement – termination placement has been varied to illustrate the impact of incorrect placement during initial application layout.

Figure 51 Simulation 13: [DC Simulation] - LVTTTL (Clock) → LVTTTL (DSP) [Term. at DSP] #1

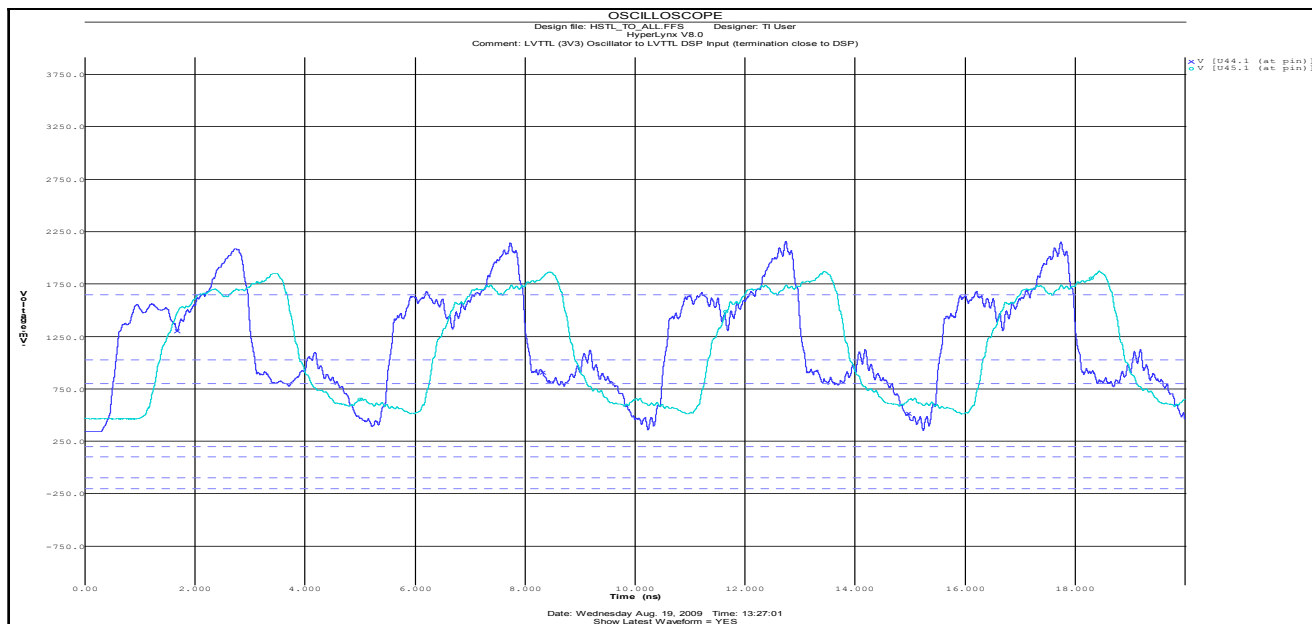


Figure 52 Simulation 14: [DC Simulation] - LVTTTL (Clock) → LVTTTL (DSP) [Term. at Clock] #2

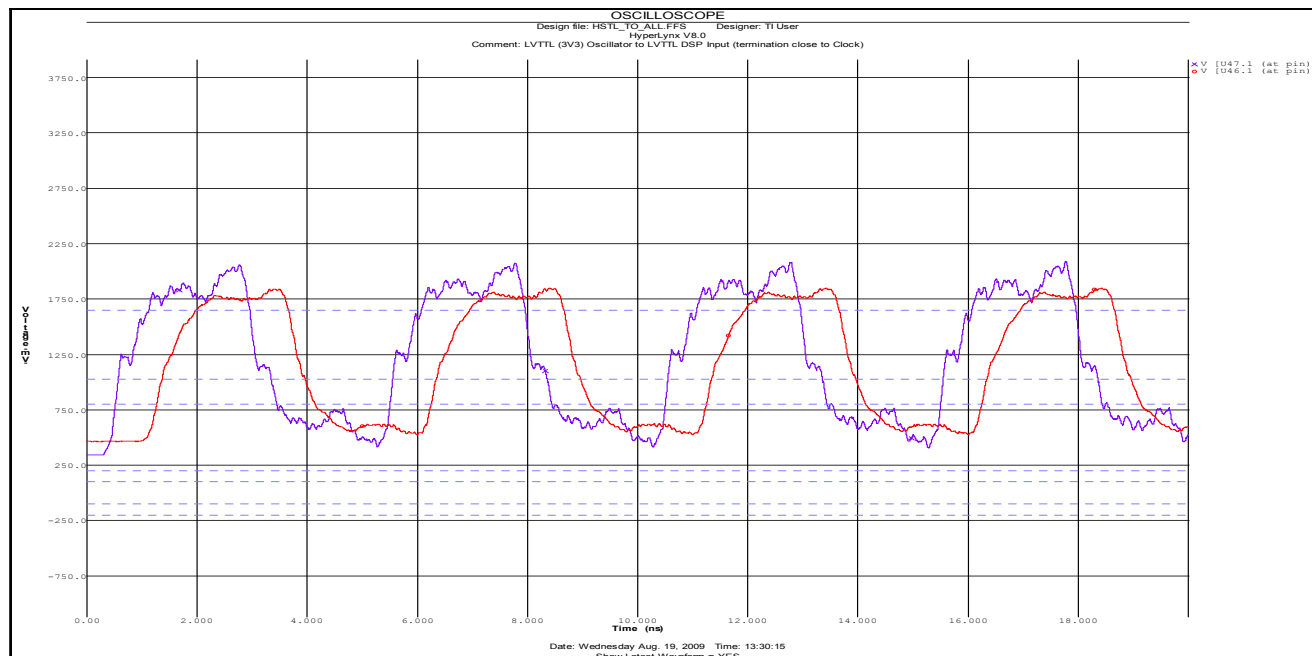


Figure 53 Simulation 15: [DC Simulation] - LVTTTL (Clock) → LVTTTL (DSP) [Midpoint Term] #3

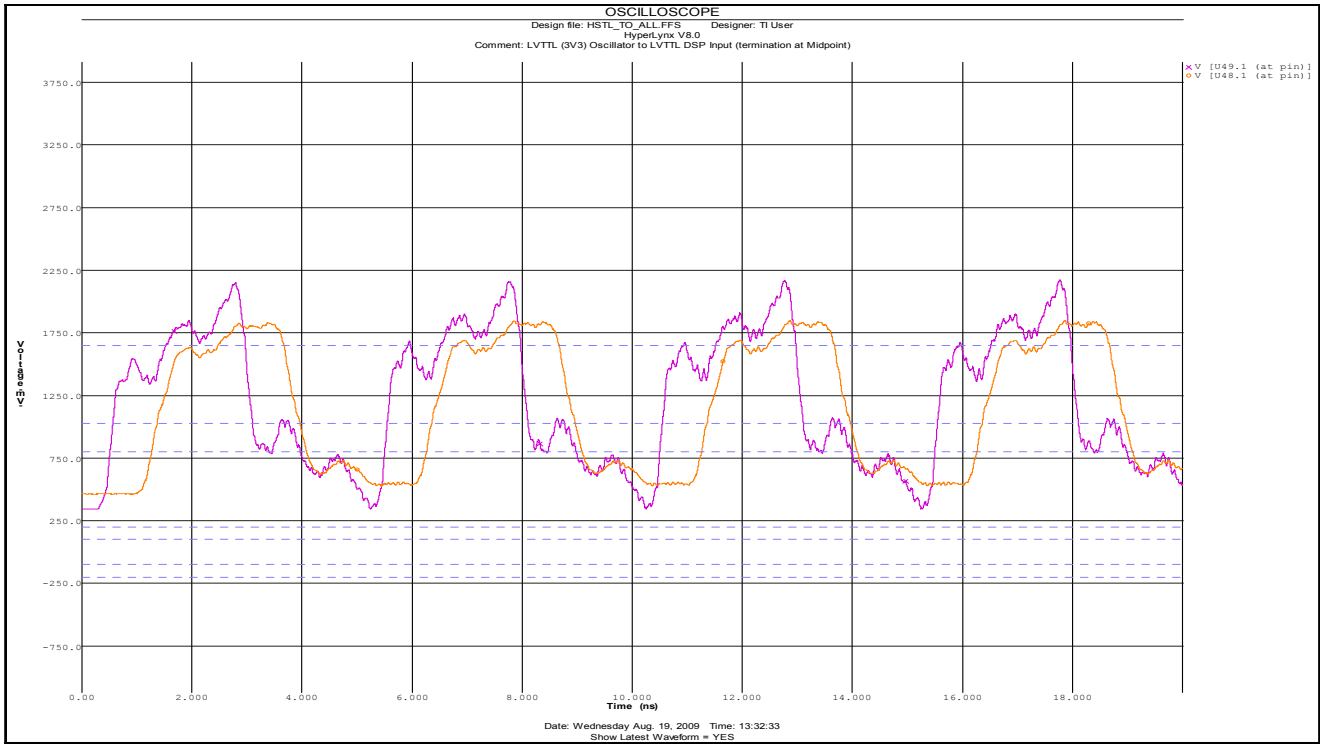


Figure 54 (Simulation 16) denotes the simulation results for the recommended CMOS → LVDS DSP configuration.

Figure 54 Simulation 16: [DC Simulation] - CMOS [3.3 V] (Clock) → Single Ended LVDS (DSP)

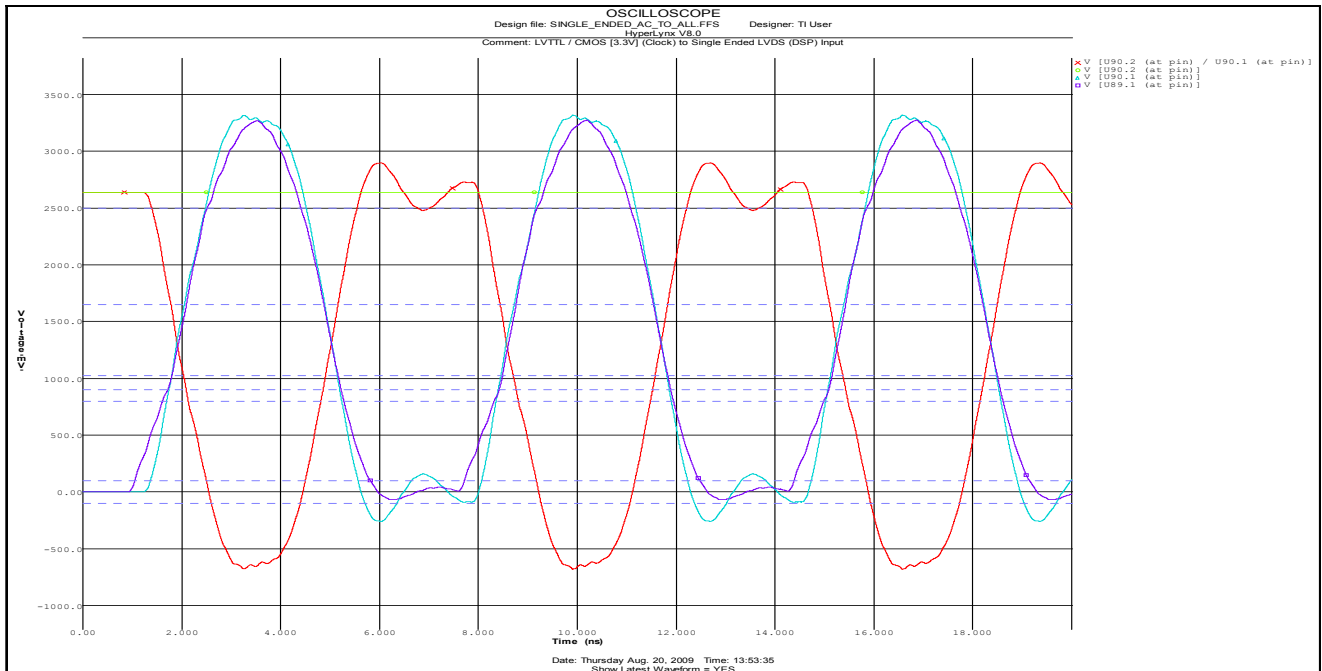
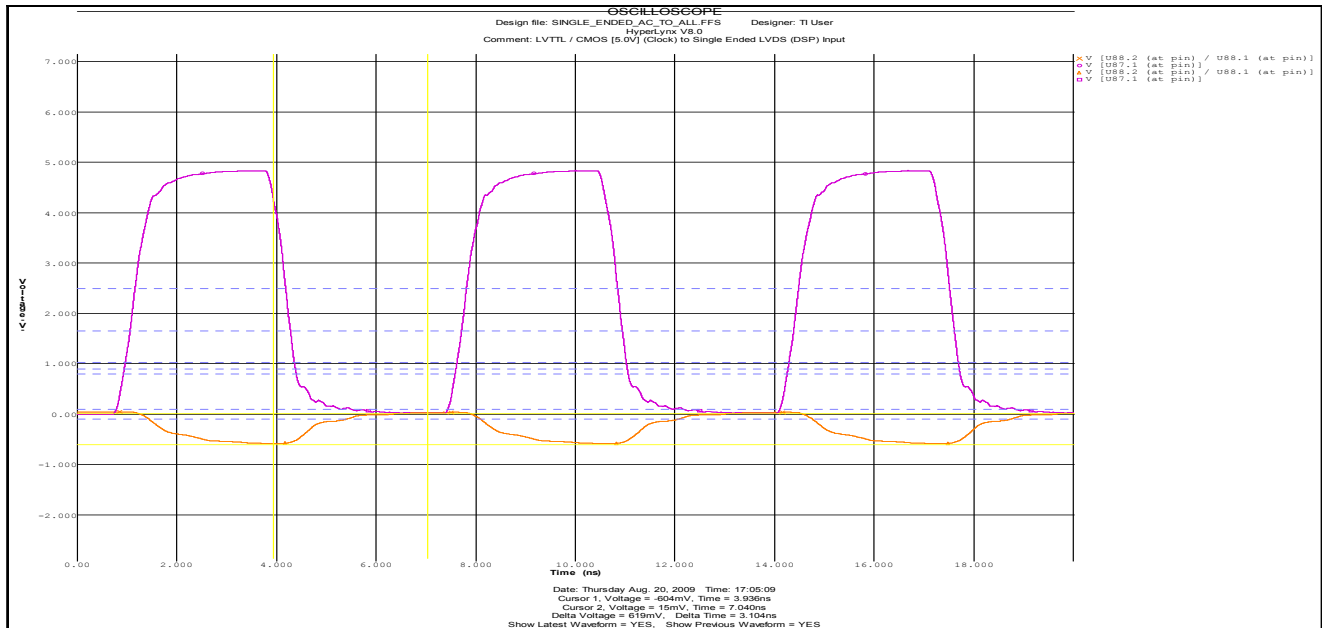


Figure 55 (Simulation 17) denotes the simulation results for the recommended CMOS → LVDS (5 V) DSP configuration.

Figure 55 Simulation 17: [DC Simulation] –CMOS [5.0 V] (Clock) → Single Ended LVDS (DSP)



7.2 AC-Coupling

The following section provides a comprehensive analysis of various AC-Coupling schemes.

7.2.1 LVPECL Clock Source → DSP

Figure 56 (Simulation 18) denotes the simulation results for the recommended LVPECL → LVDS DSP configuration.

Figure 56 Simulation 18: [AC Simulation] - LVPECL (Clock) → LVDS (DSP) - bias

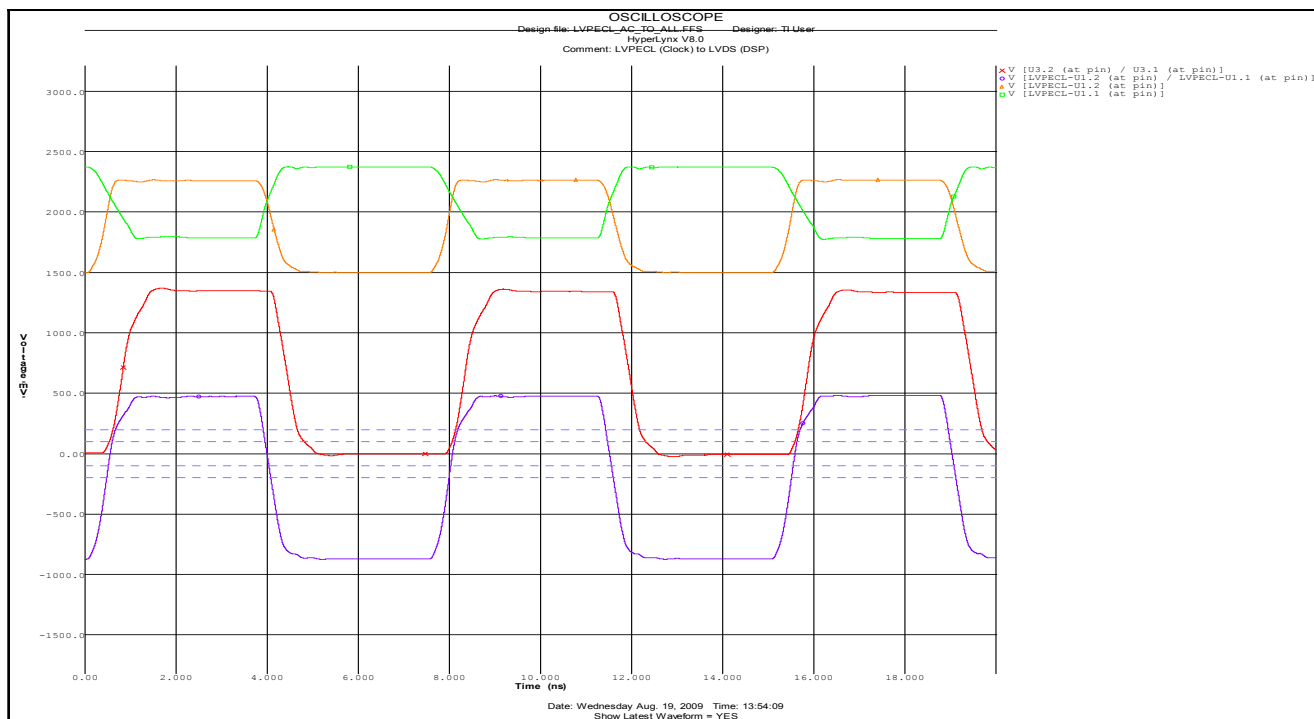
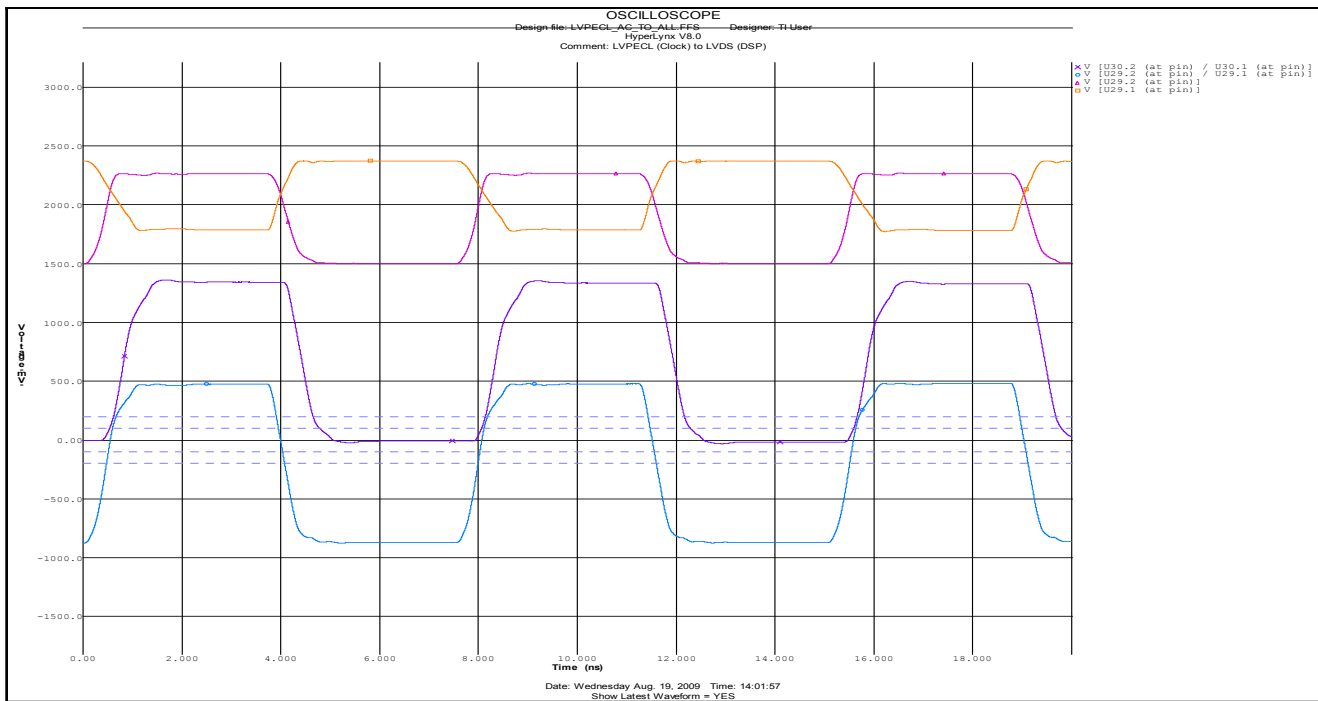


Figure 57 (Simulation 19) denotes the simulation results for the recommended LVPECL → LVDS DSP configuration.

Figure 57 Simulation 19: [AC Simulation] - LVPECL (Clock) → LVDS (DSP)



7.2.2 CML Clock Source → DSP

Figure 58 (Simulation 20) denotes the simulation results for the recommended LVPECL → CML DSP configuration.

Figure 58 Simulation 20: [AC Simulation] - LVPECL (Clock) → CML (DSP)

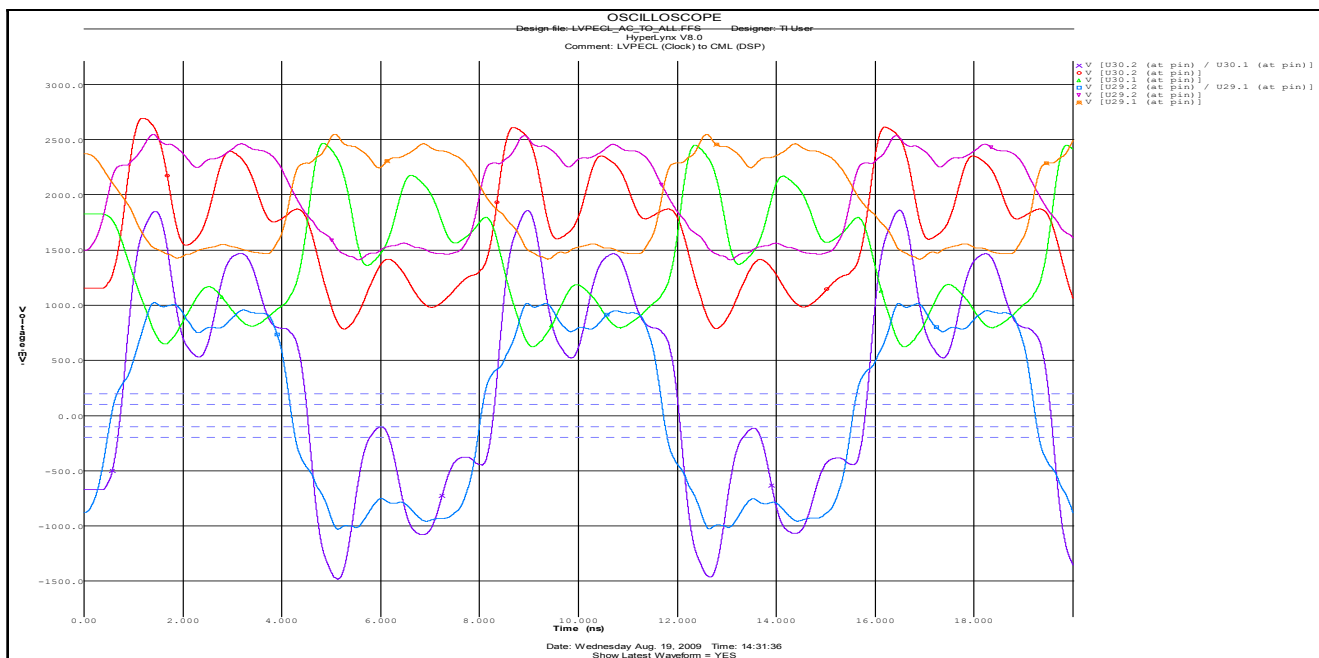


Figure 59 (Simulation 21) denotes the simulation results for the recommended LVPECL → CML (attenuated) DSP configuration.

Figure 59 Simulation 21: [AC Simulation] - LVPECL (Clock) → CML (DSP) - attenuated

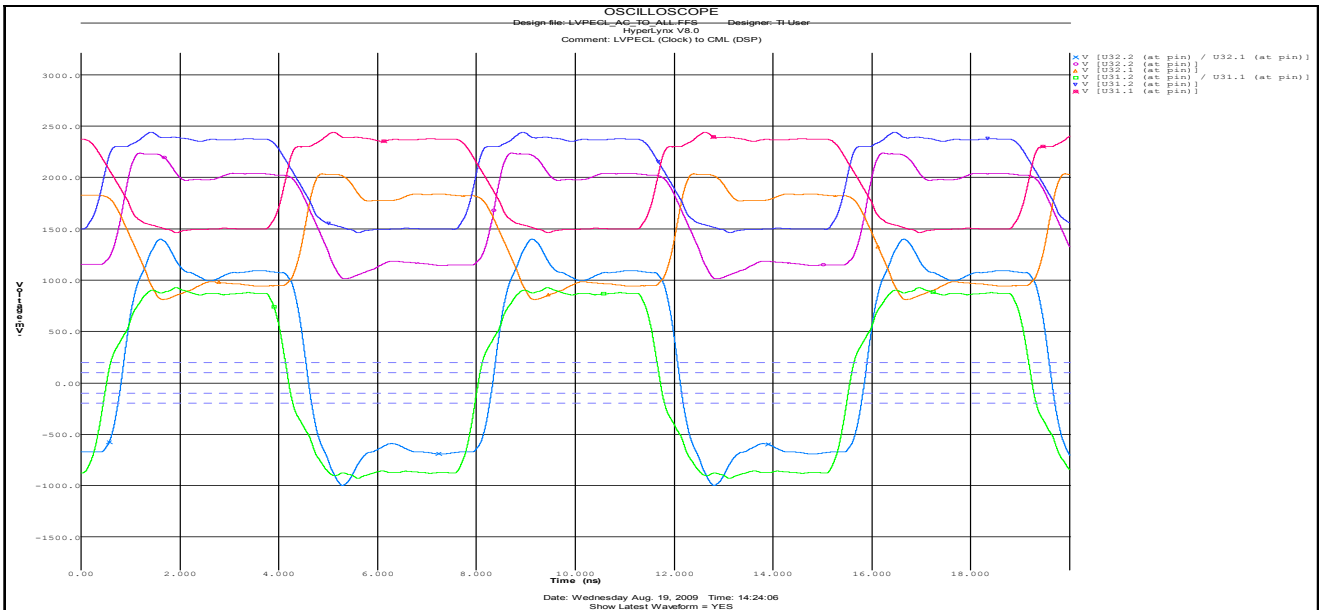


Figure 60 (Simulation 22) denotes the simulation results for the recommended LVPECL → HSTL DSP configuration.

Figure 60 Simulation 22: [AC Simulation] - LVPECL (Clock) → HSTL (DSP)

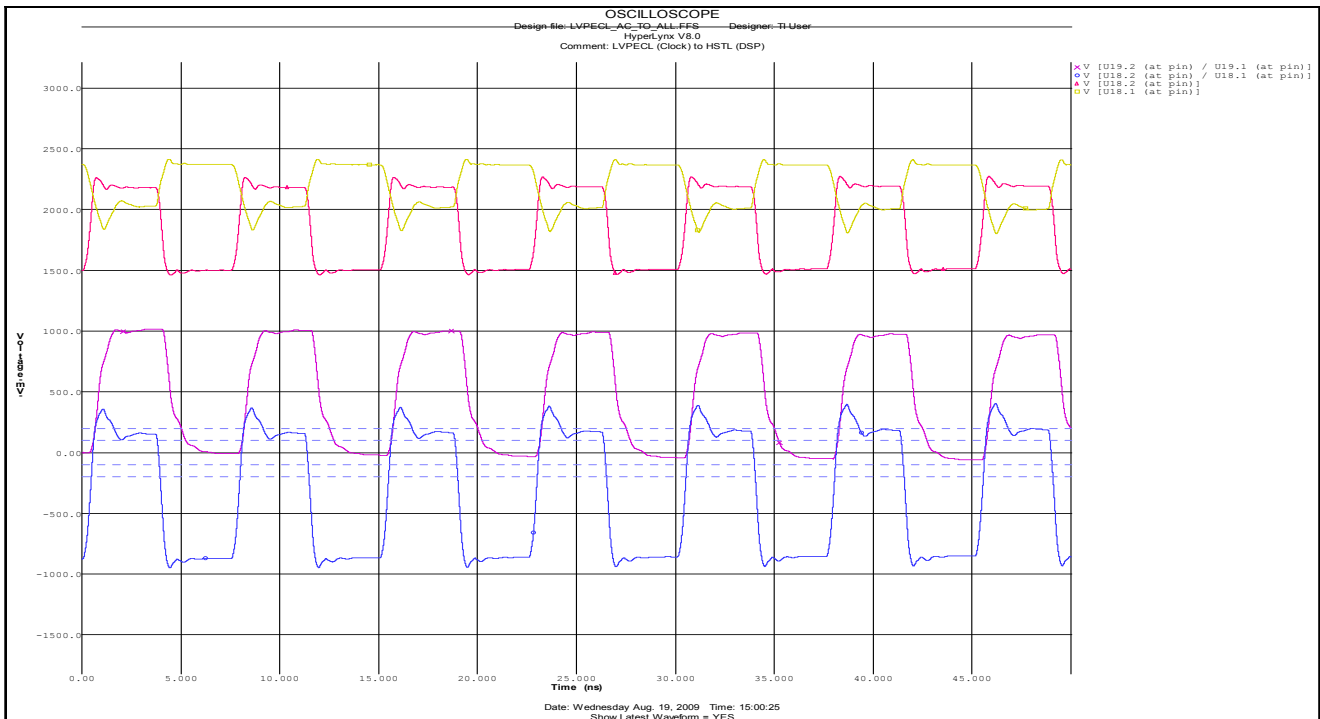
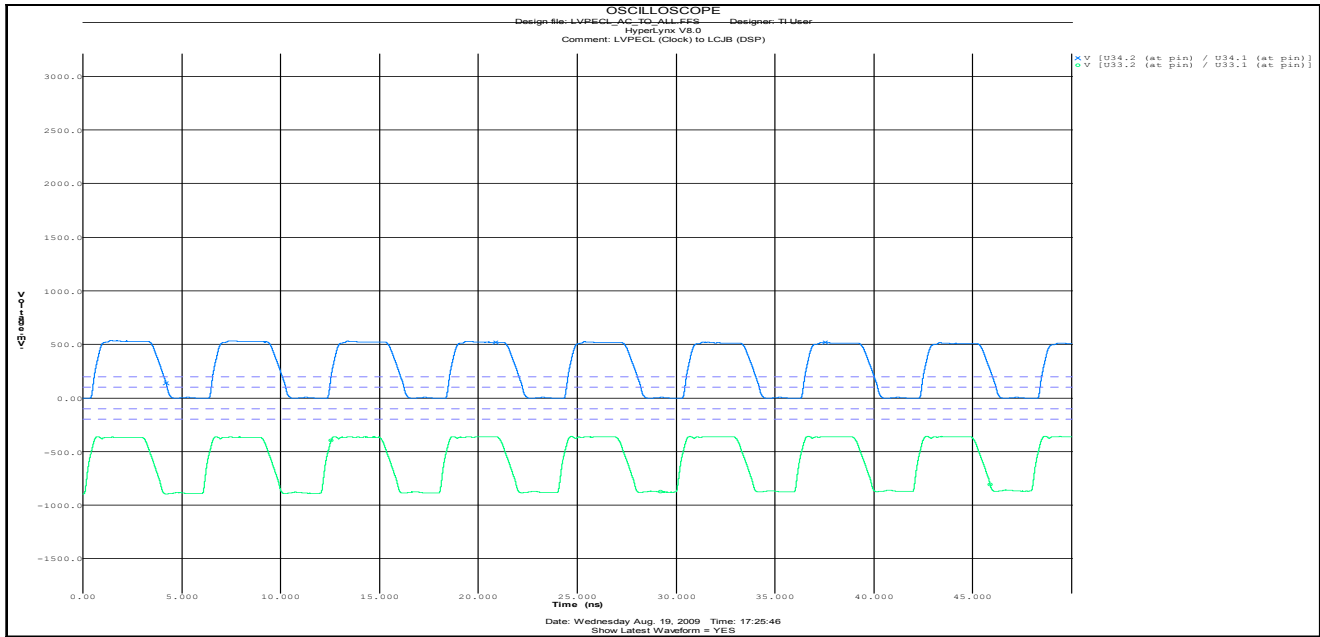


Figure 61 (Simulation 23) denotes the simulation results for the recommended LVPECL → LJCB DSP configuration.

Figure 61 Simulation 23: [AC Simulation] - LVPECL (Clock) → LCJB (DSP)



7.2.3 LVDS Clock Source → DSP

Figure 62 (Simulation 24) denotes the simulation results for the recommended LVDS → LVDS DSP configuration.

Figure 62 Simulation 24: [AC Simulation] - LVDS (Clock) → LVDS (DSP)

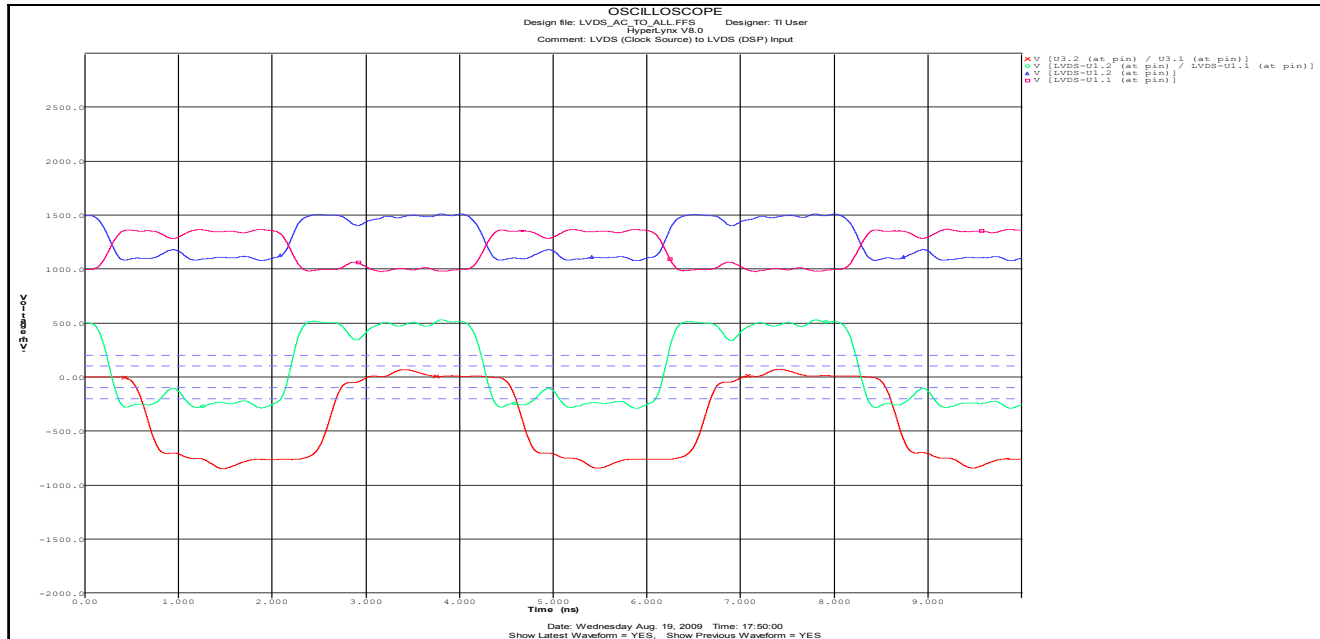


Figure 63 (Simulation 25) denotes the simulation results for the recommended LVDS → CML DSP configuration.

Figure 63 Simulation 25: [AC Simulation] - LVDS (Clock) → CML (DSP)

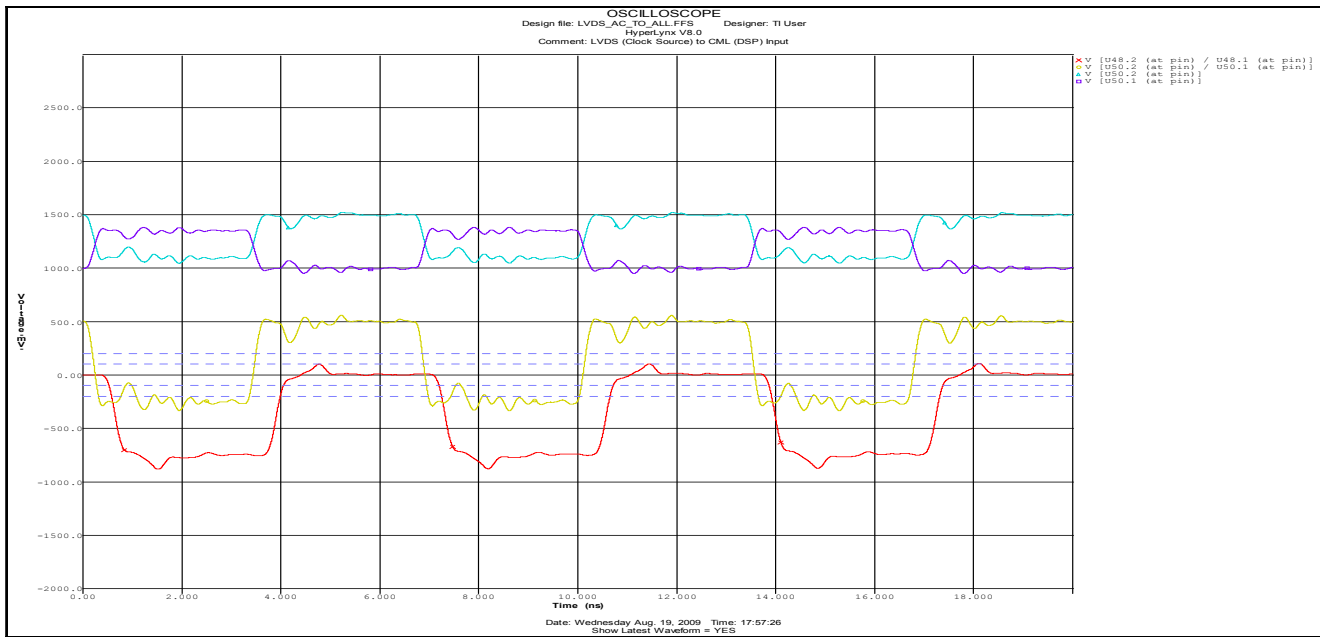
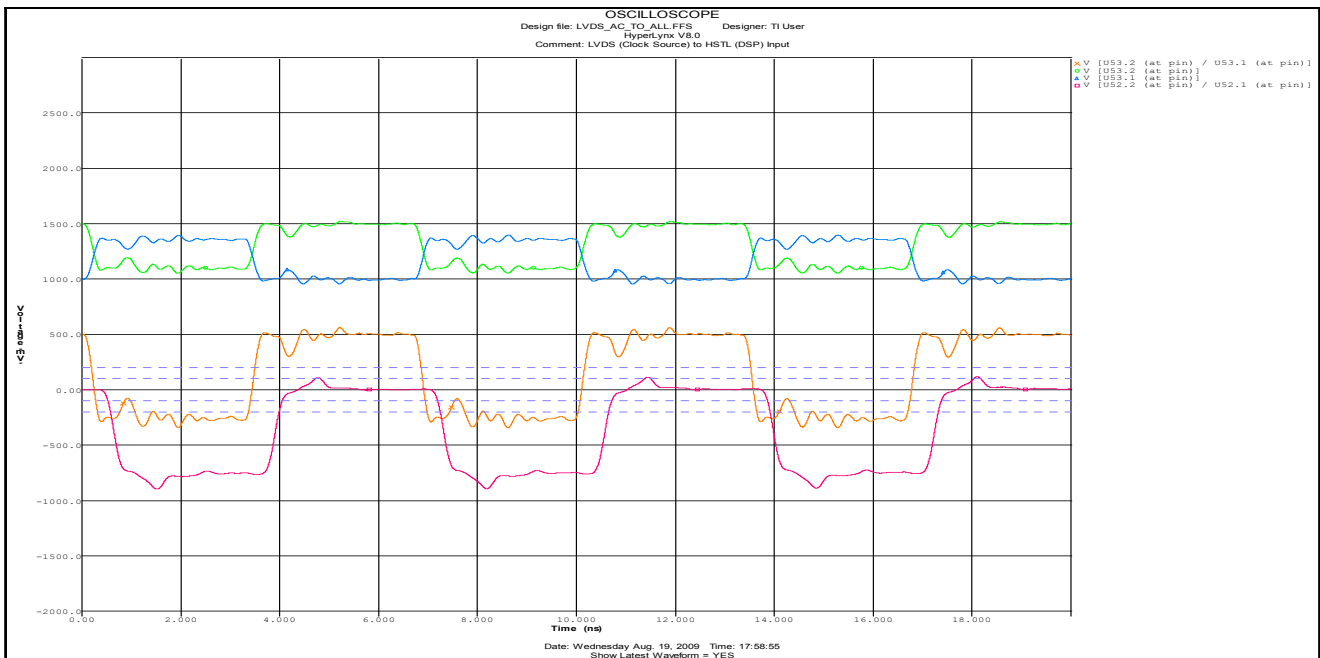


Figure 64 (Simulation 26) denotes the simulation results for the recommended LVDS → HSTL DSP configuration.

Figure 64 Simulation 26: [AC Simulation] - LVDS (Clock) → HSTL (DSP)



7.2.4 CML Clock Source → DSP

Figure 65 (Simulation 27) denotes the simulation results for the recommended CML → LVDS DSP configuration.

Figure 65 Simulation 27: [AC Simulation] - CML (Clock) → LVDS (DSP)

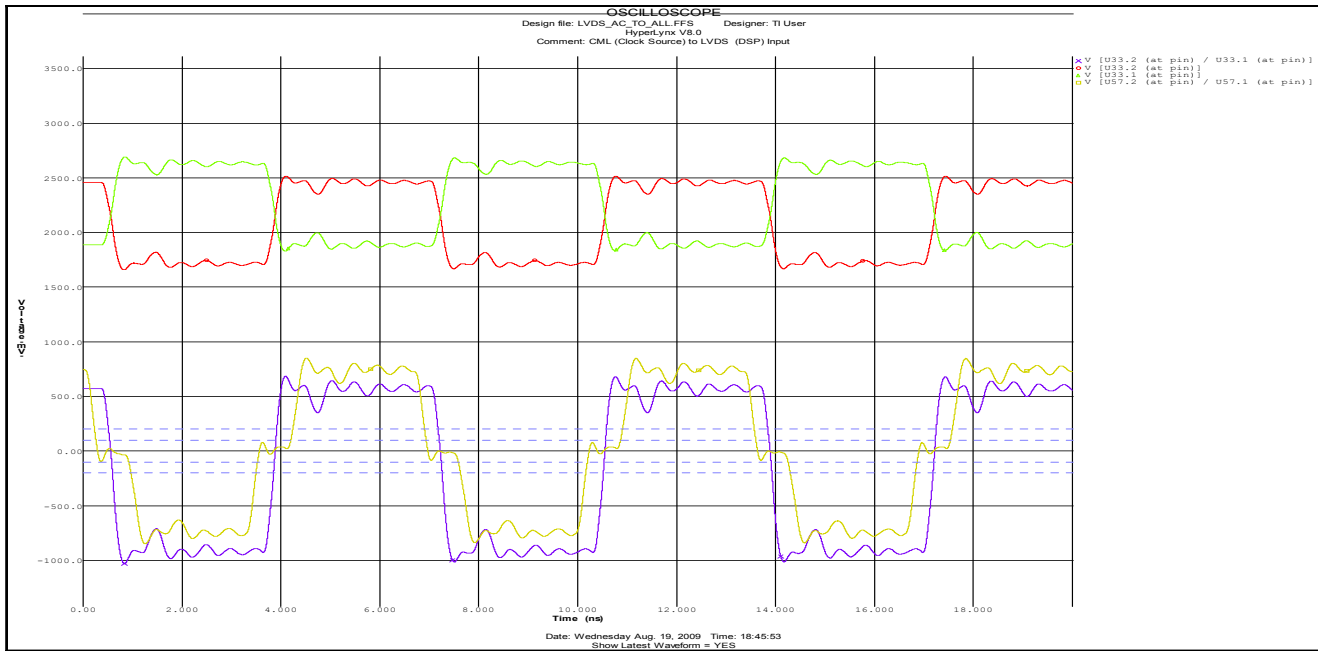


Figure 66 (Simulation 28) denotes the simulation results for the recommended CML → CML DSP configuration.

Figure 66 Simulation 28: [AC Simulation] - CML (Clock) → CML (DSP)

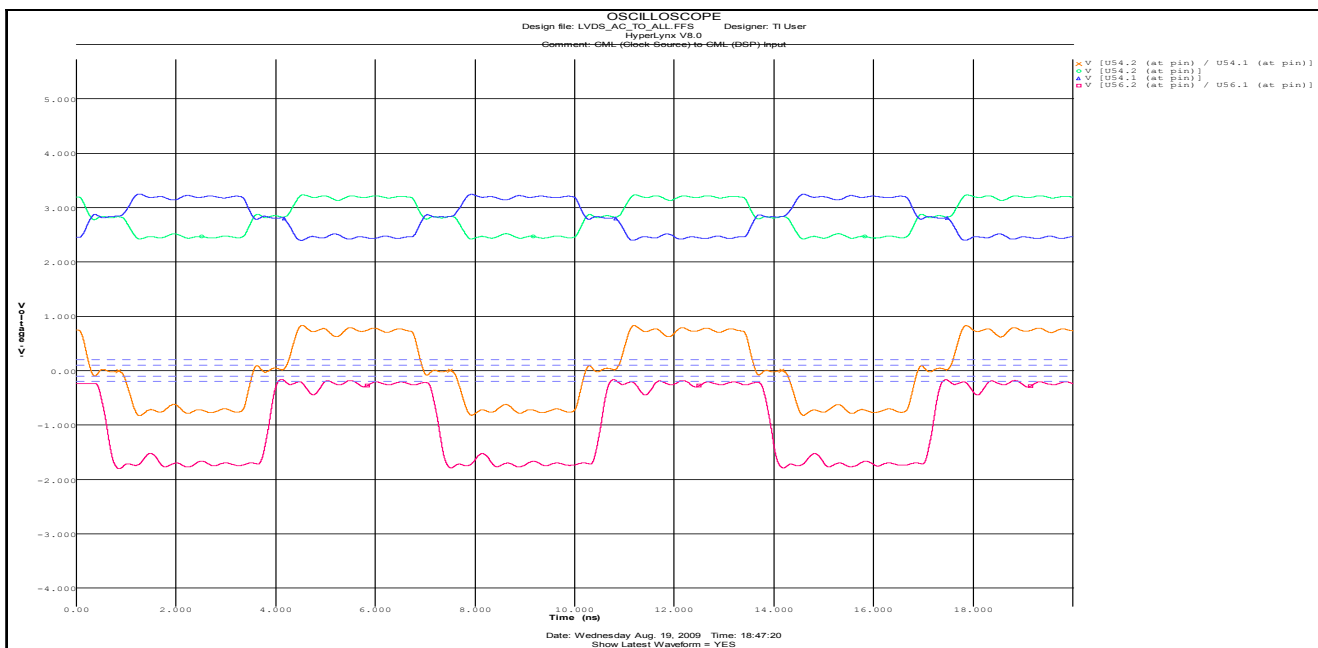


Figure 67 (Simulation 29) denotes the simulation results for the recommended CML → LVDS DSP configuration.

Figure 67 Simulation 29: [AC Simulation] - CML (Clock) → LVDS (DSP) 3.3 V

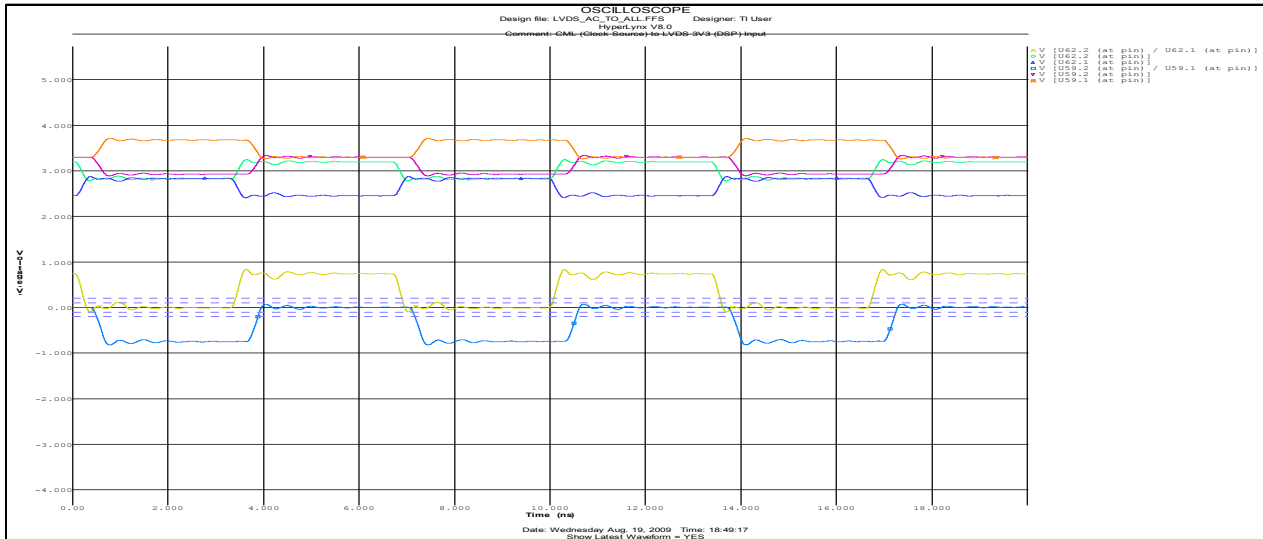


Figure 68 (Simulation 30) denotes the simulation results for the recommended CML → LVDS DSP configuration.

Figure 68 Simulation 30: [AC Simulation] - CML (Clock) → LVDS (DSP) 1.8 V

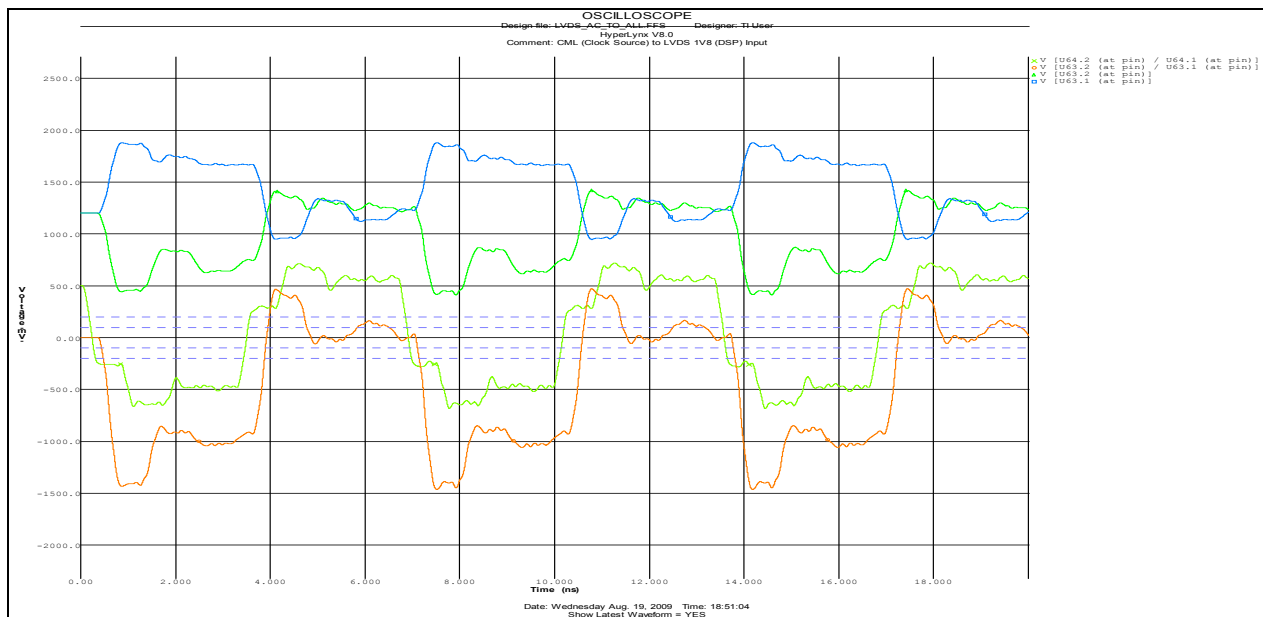
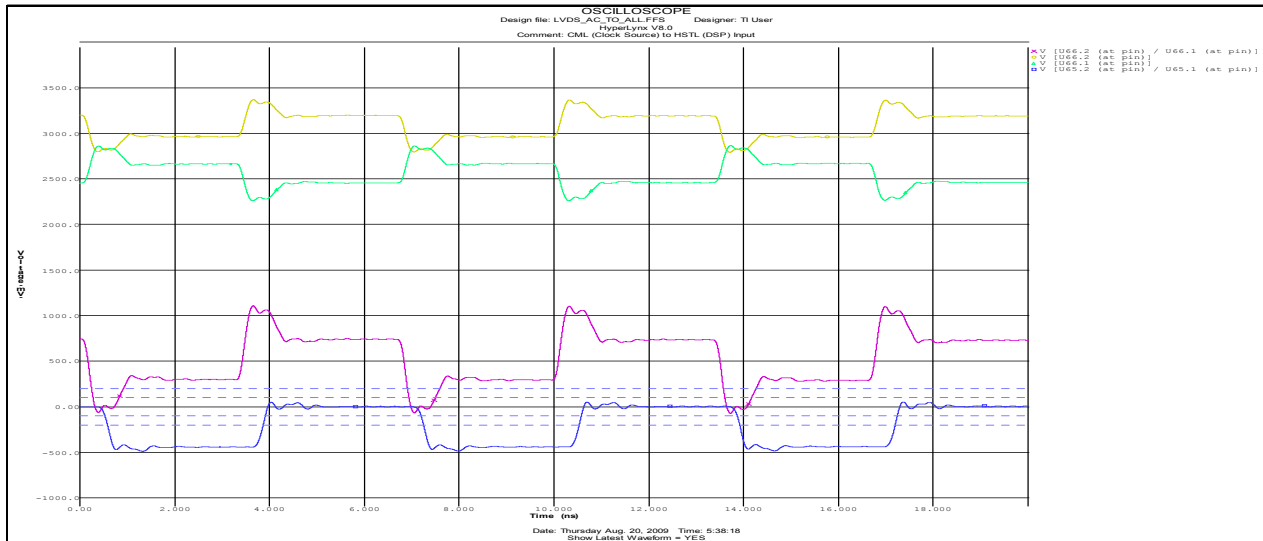


Figure 69 (Simulation 31) denotes the simulation results for the recommended CML → HSTL DSP configuration.

Figure 69 Simulation 31: [AC Simulation] - CML (Clock) → HSTL (DSP)



7.2.5 HSTL Clock Source → DSP

Figure 70 (Simulation 32) denotes the simulation results for the recommended HSTL → LVDS DSP configuration.

Figure 70 Simulation 32: [AC Simulation] - HSTL (Clock) → LVDS (DSP)

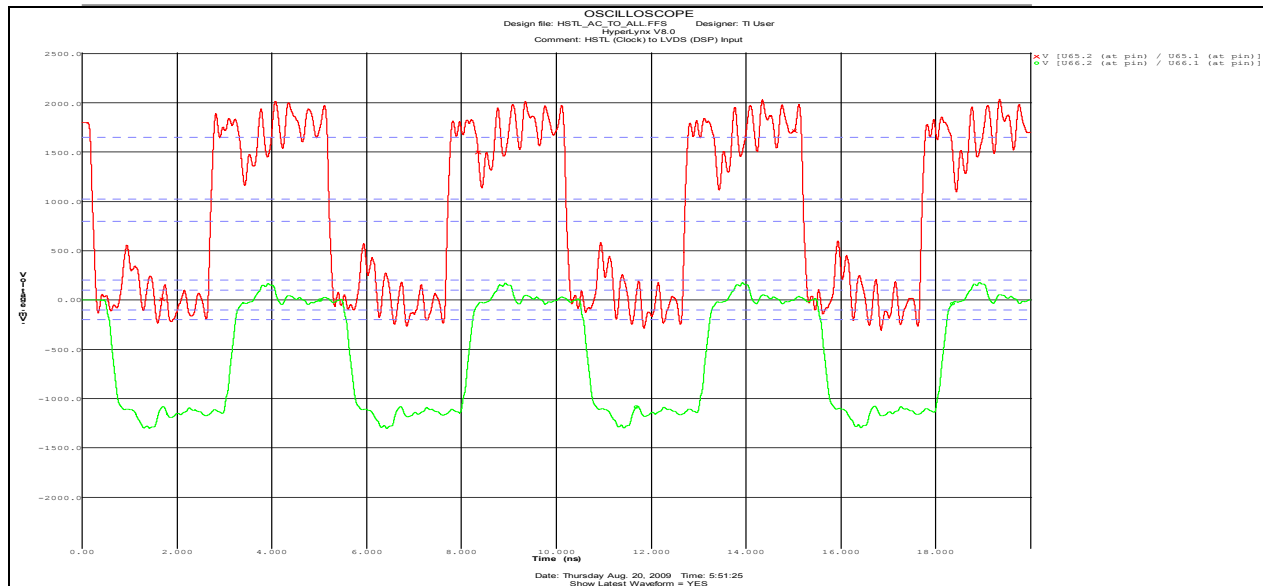
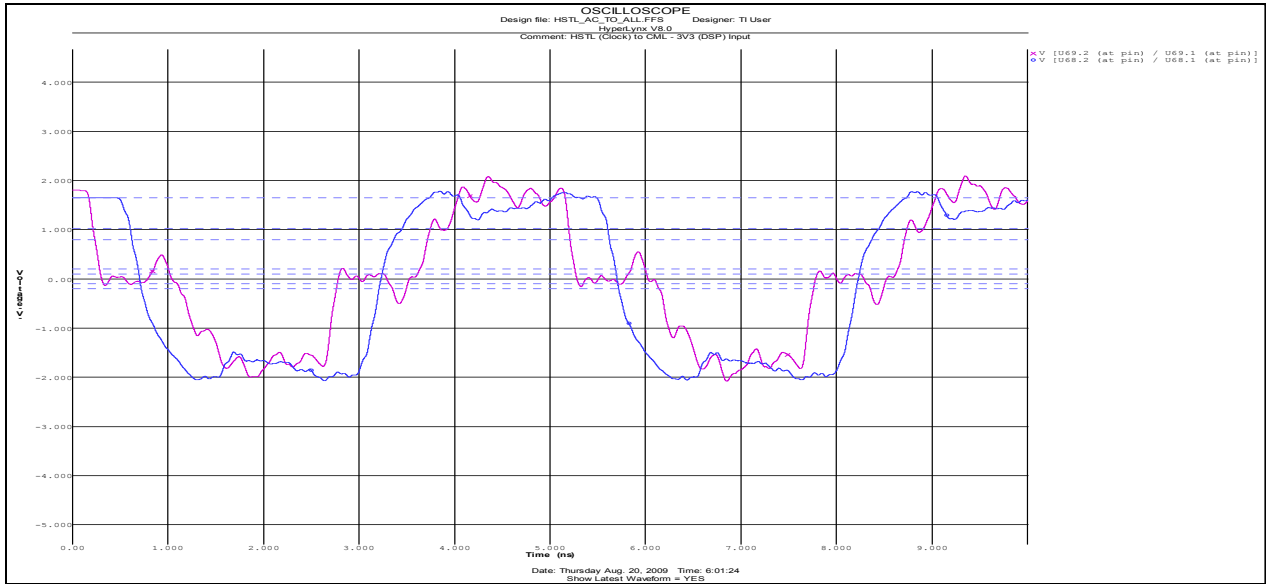


Figure 71 (Simulation 33) denotes the simulation results for the recommended HSTL → CML DSP configuration.

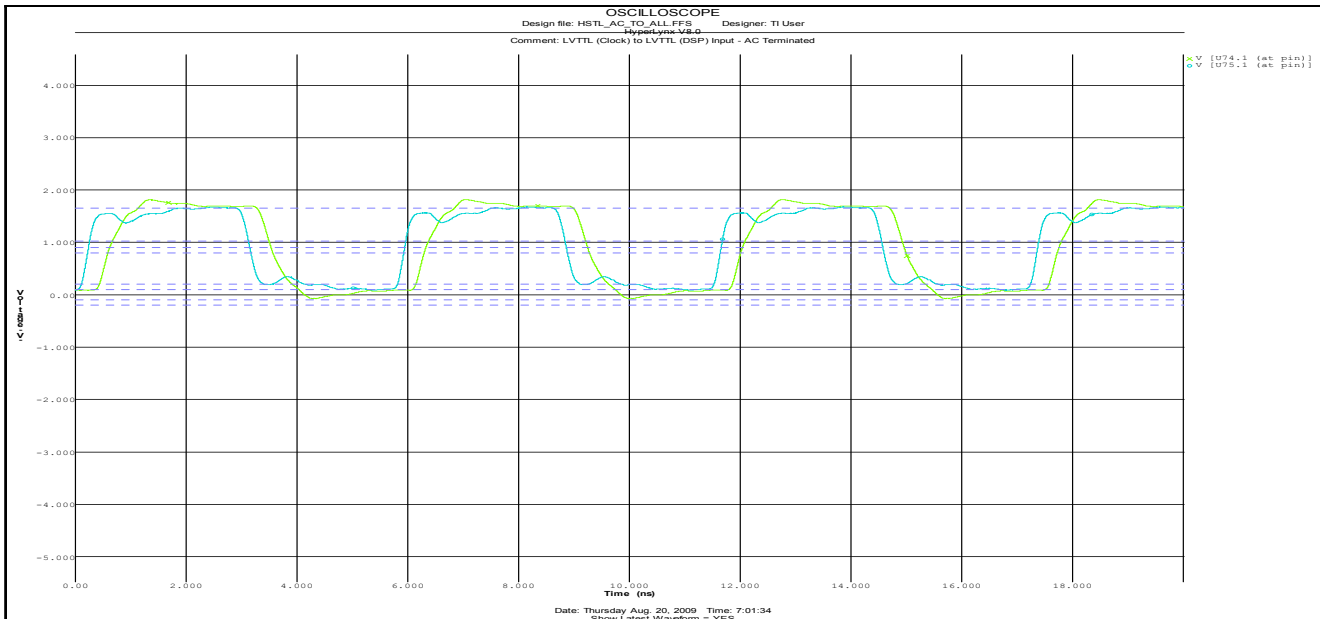
Figure 71 Simulation 33: [AC Simulation] - HSTL (Clock) → CML 3V3 (DSP)



7.2.6 LVTTTL Clock Source → DSP

Figure 72 (Simulation 34) denotes the simulation results for the recommended LVTTTL → LVTTTL DSP configuration.

Figure 72 Simulation 34: [AC Simulation] - LVTTTL (Clock) → LVTTTL AC-Termination (DSP)



8 Warnings & Disclaimers

Comments and proposals identified within this document are presented as guidelines. Texas Instruments cannot fully comprehend every possible application or design variation and therefore requires each end user to perform proper due diligence using good engineering practices including proper component selection, simulation, and modeling to verify these recommendations will work properly in the end use application. This application guide is not intended to be the sole source or reference design guide. Many factors not encompassed within this document can force a change in component values, selection, placement, or termination type.

The possible permutations available do to component, layout, and assembly can also induce variations not encompassed in the recommendations provided. Voltage rails, manufacturer parts selection, and switching levels should all be verified before committing the design to production. Not all manufacturer's device input and output levels match equally and thus slight modifications to each design may occur.

It is the end use's responsibility to always verify the design, and connectivity between any active or passive component and the targeted DSP. This includes verifying against individual data sheets and application notes.

Simulation and modeling play an important role in system verification and validation. This effort and the need to conduct this level of analysis should not be overlooked in any design – regardless of simplicity or complexity.

This is not a primer for high-speed design. Use of the information provided assumes a strong understanding of electrical and mechanical design requirements in a high-performance application design.

To avoid common design mistakes, it is always recommended that the clock source and clock destination be of like types.

9 References

The following documents were used or referenced during the creation of this design guide:

1. DC-Coupling Between Differential LVPECL, LVDS, HSTL, and CM (SCAA062)
2. AC-Coupling between LVPECL, LVDS, CML, and HSTL (SCAA059)
3. Interfacing Between LVPECL, LVDS, and CML (SCAA056)
4. Interfacing Differential Logic With LVDS Receivers (SLLA101)
5. Interfacing Between LVPECL, VML, CML, and LVDS Levels (SLLA120)
6. GTL Low-Level, High Speed Interface Standard for Digital Integrated Circuits (JESD8-3A)
7. 2.5 & 1.8 V – 2.7 V Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits (JESD8-5A)
8. High Speed Transceiver Logic Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits (JESD8-6)
9. 1.8 & 1.2 V – 1.95 V Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits (JESD8-7A)
10. Stub Series Terminated Logic for 2.5V -- SSTL_2 (JESD8-9)
11. TIA/EIA-644-A Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
12. Interfacing Between LVPECL, LVDS, and CML (SCAA056)

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