Application Report
SPRACL8–March 2019

KeyStone™ I DDR3 interface bring-up

Catalog Processor

ABSTRACT

Obtaining robust KeyStone I DDR3 interface operation requires careful PCB design and layout as well as proper DDR Controller and PHY configuration through software. This application report highlights the documents and tools available to support this design and configuration.

Project collateral discussed in this document can be downloaded from the following URL: http://www.ti.com/lit/zip/spracl8.

Contents

Trademarks

1 Introduction

KeyStone I DDR3 commissioning is in two parts: proper board design and proper software configuration. The *DDR3 design requirements for KeyStone devices* must be followed to obtain a properly routed board. The steps in *KeyStone I DDR3 initialization* must be followed to get the DDR3 Controller and PHY properly configured to communicate robustly with the DDR3 SDRAM.

2 Spreadsheet Tools

There are two spreadsheets that can be downloaded from the link in *KeyStone I DDR3 initialization* that assist with register configuration: PHY_CALC and REG_CALC. These spreadsheets are contained in [3]. Additional details are in the *Keystone architecture DDR3 memory controller user's guide*. All are available from the C6678 web page at: TMS320C6678.

3 DDR3 Routed Length Matching

The most overlooked step in designing a robust DDR3 layout is length-matching the fly-by nets properly. The fly-by nets are the address, clock, control and command nets. These must be length matched individually from the DDR3 controller (KeyStone I device) to each of the SDRAM devices.

The PHY_CALC spreadsheet calculates initial values that are needed by the leveling logic in the DDR3 PHY. You need to populate the lengths of the clock pair and the DQS pair to each SDRAM into this spreadsheet. This information is taken from the length matching report. The results then need to be copied into the CCS GEL file and then later into your application software.

Table 1 is an example of a length matching report generated by CAD software showing that the ADDR, CMD and CTL (fly-by group) length matching rules have been met.

Table 1. Example Fly-by Length Matching Report

	Rule	Length (mils)	Skew (mils)	Check
R_DDR_ADD_U4 (27)				
DSP1.A12:U4.J7 [DSP0_DDR3_ECKP_0]	**Target**	2315.91		**Target**
DSP1.B12:U4.K7 [DSP0_DDR3_ECKN_0]	0.00 MIL:20.00 MIL	2315.16	0.75	Pass
DSP1.A14:U4.N3 [DSP0_DDR3_EA0]	0.00 MIL:20.00 MIL	2329.05	-13.14	Pass
DSP1.B14:U4.P7 [DSP0_DDR3_EA1]	0.00 MIL:20.00 MIL	2315.69	0.22	Pass
DSP1.F14:U4.P3 [DSP0_DDR3_EA2]	0.00 MIL:20.00 MIL	2318.68	-2.77	Pass
DSP1.F13:U4.N2 [DSP0_DDR3_EA3]	0.00 MIL:20.00 MIL	2321.20	-5.29	Pass
DSP1.A15:U4.P8 [DSP0_DDR3_EA4]	0.00 MIL:20.00 MIL	2312.56	3.35	Pass
DSP1.C15:U4.P2 [DSP0_DDR3_EA5]	0.00 MIL:20.00 MIL	2303.57	12.34	Pass
DSP1.B15:U4.R8 [DSP0_DDR3_EA6]	0.00 MIL:20.00 MIL	2332.99	-17.08	Pass
DSP1.D15:U4.R2 [DSP0_DDR3_EA7]	0.00 MIL:20.00 MIL	2333.28	-17.37	Pass
DSP1.F15:U4.T8 [DSP0_DDR3_EA8]	0.00 MIL:20.00 MIL	2335.84	-19.93	Pass
DSP1.E15:U4.R3 [DSP0_DDR3_EA9]	0.00 MIL:20.00 MIL	2312.01	3.90	Pass
DSP1.E16:U4.L7 [DSP0_DDR3_EA10]	0.00 MIL:20.00 MIL	2313.78	2.13	Pass
DSP1.D16:U4.R7 [DSP0_DDR3_EA11]	0.00 MIL:20.00 MIL	2316.78	-0.87	Pass
DSP1.E17:U4.N7 [DSP0_DDR3_EA12]	0.00 MIL:20.00 MIL	2315.76	0.15	Pass
DSP1.C16:U4.T3 [DSP0_DDR3_EA13]	0.00 MIL:20.00 MIL	2310.17	5.74	Pass
DSP1.D17:U4.T7 [DSP0_DDR3_EA14]	0.00 MIL:20.00 MIL	2317.66	-1.75	Pass
DSP1.C17:U4.M7 [DSP0_DDR3_EA15]	0.00 MIL:20.00 MIL	2316.65	-0.74	Pass
DSP1.A13:U4.M2 [DSP0_DDR3_EBA_0]	0.00 MIL:20.00 MIL	2317.78	-1.87	Pass
DSP1.B13:U4.N8 [DSP0_DDR3_EBA_1]	0.00 MIL:20.00 MIL	2312.46	3.45	Pass
DSP1.C13:U4.M3 [DSP0_DDR3_EBA_2]	0.00 MIL:20.00 MIL	2315.10	0.81	Pass
DSP1.C10:U4.J3 [DSP0_DDR3_ERAS#]	0.00 MIL:20.00 MIL	2328.06	-12.15	Pass
DSP1.D12:U4.K3 [DSP0_DDR3_ECAS#]	0.00 MIL:20.00 MIL	2310.86	5.05	Pass
DSP1.E12:U4.L3 [DSP0_DDR3_EWE#]	0.00 MIL:20.00 MIL	2312.28	3.63	Pass

Table 1. Example Fly-by Length Matching Report (continued)

	Rule	Length (mils)	Skew (mils)	Check
DSP1.C11:U4.L2 [DSP0_DDR3_ECS_0#]	0.00 MIL:20.00 MIL	2317.55	-1.64	Pass
DSP1.D11:U4.K9 [DSP0_DDR3_ECKE_0]	0.00 MIL:20.00 MIL	2317.76	-1.85	Pass
DSP1.D13:U4.K1 [DSP0_DDR3_EODT_0]	0.00 MIL:20.00 MIL	2313.44	2.47	Pass
R_DDR_ADD_U5 (27)				
DSP1.A12:U5.J7 [DSP0_DDR3_ECKP_0]	**Target**	2826.47		**Target**
DSP1.B12:U5.K7 [DSP0_DDR3_ECKN_0]	0.00 MIL:20.00 MIL	2826.89	-0.42	Pass
DSP1.A14:U5.N3 [DSP0_DDR3_EA0]	0.00 MIL:20.00 MIL	2841.36	-14.89	Pass
DSP1.B14:U5.P7 [DSP0_DDR3_EA1]	0.00 MIL:20.00 MIL	2828.82	-2.35	Pass
DSP1.F14:U5.P3 [DSP0_DDR3_EA2]	0.00 MIL:20.00 MIL	2831.01	-4.54	Pass
DSP1.F13:U5.N2 [DSP0_DDR3_EA3]	0.00 MIL:20.00 MIL	2833.89	-7.42	Pass
DSP1.A15:U5.P8 [DSP0_DDR3_EA4]	0.00 MIL:20.00 MIL	2830.24	-3.77	Pass
DSP1.C15:U5.P2 [DSP0_DDR3_EA5]	0.00 MIL:20.00 MIL	2815.89	10.58	Pass
DSP1.B15:U5.R8 [DSP0_DDR3_EA6]	0.00 MIL:20.00 MIL	2845.02	-18.55	Pass
DSP1.D15:U5.R2 [DSP0_DDR3_EA7]	0.00 MIL:20.00 MIL	2845.71	-19.24	Pass
DSP1.F15:U5.T8 [DSP0_DDR3_EA8]	0.00 MIL:20.00 MIL	2842.97	-16.50	Pass
DSP1.E15:U5.R3 [DSP0_DDR3_EA9]	0.00 MIL:20.00 MIL	2824.00	2.47	Pass
DSP1.E16:U5.L7 [DSP0_DDR3_EA10]	0.00 MIL:20.00 MIL	2827.37	-0.90	Pass
DSP1.D16:U5.R7 [DSP0_DDR3_EA11]	0.00 MIL:20.00 MIL	2828.61	-2.14	Pass
DSP1.E17:U5.N7 [DSP0_DDR3_EA12]	0.00 MIL:20.00 MIL	2828.82	-2.35	Pass
DSP1.C16:U5.T3 [DSP0_DDR3_EA13]	0.00 MIL:20.00 MIL	2823.51	2.96	Pass
DSP1.D17:U5.T7 [DSP0_DDR3_EA14]	0.00 MIL:20.00 MIL	2826.85	-0.38	Pass
DSP1.C17:U5.M7 [DSP0_DDR3_EA15]	0.00 MIL:20.00 MIL	2830.27	-3.80	Pass
DSP1.A13:U5.M2 [DSP0_DDR3_EBA_0]	0.00 MIL:20.00 MIL	2830.67	-4.20	Pass
DSP1.B13:U5.N8 [DSP0_DDR3_EBA_1]	0.00 MIL:20.00 MIL	2826.16	0.31	Pass
DSP1.C13:U5.M3 [DSP0_DDR3_EBA_2]	0.00 MIL:20.00 MIL	2827.41	-0.94	Pass
DSP1.C10:U5.J3 [DSP0_DDR3_ERAS#]	0.00 MIL:20.00 MIL	2839.48	-13.01	Pass
DSP1.D12:U5.K3 [DSP0_DDR3_ECAS#]	0.00 MIL:20.00 MIL	2826.69	-0.22	Pass
DSP1.E12:U5.L3 [DSP0_DDR3_EWE#]	0.00 MIL:20.00 MIL	2825.73	0.74	Pass
DSP1.C11:U5.L2 [DSP0_DDR3_ECS_0#]	0.00 MIL:20.00 MIL	2829.87	-3.40	Pass
DSP1.D11:U5.K9 [DSP0_DDR3_ECKE_0]	0.00 MIL:20.00 MIL	2831.51	-5.04	Pass
DSP1.D13:U5.K1 [DSP0_DDR3_EODT_0]	0.00 MIL:20.00 MIL	2831.00	-4.53	Pass
R_DDR_ADD_U8 (27)				
DSP1.A12:U8.J7 [DSP0_DDR3_ECKP_0]	**Target**	3300.49		**Target**
DSP1.B12:U8.K7 [DSP0_DDR3_ECKN_0]	0.00 MIL:20.00 MIL	3301.00	-0.51	Pass
DSP1.A14:U8.N3 [DSP0_DDR3_EA0]	0.00 MIL:20.00 MIL	3317.84	-17.35	Pass
DSP1.B14:U8.P7 [DSP0_DDR3_EA1]	0.00 MIL:20.00 MIL	3295.07	5.42	Pass
DSP1.F14:U8.P3 [DSP0_DDR3_EA2]	0.00 MIL:20.00 MIL	3314.00	-13.51	Pass
DSP1.F13:U8.N2 [DSP0_DDR3_EA3]	0.00 MIL:20.00 MIL	3316.82	-16.33	Pass
DSP1.A15:U8.P8 [DSP0_DDR3_EA4]	0.00 MIL:20.00 MIL	3298.66	1.83	Pass
DSP1.C15:U8.P2 [DSP0_DDR3_EA5]	0.00 MIL:20.00 MIL	3300.12	0.37	Pass
DSP1.B15:U8.R8 [DSP0_DDR3_EA6]	0.00 MIL:20.00 MIL	3317.54	-17.05	Pass
DSP1.D15:U8.R2 [DSP0_DDR3_EA7]	0.00 MIL:20.00 MIL	3315.90	-15.41	Pass
DSP1.F15:U8.T8 [DSP0_DDR3_EA8]	0.00 MIL:20.00 MIL	3314.38	-13.89	Pass
DSP1.E15:U8.R3 [DSP0_DDR3_EA9]	0.00 MIL:20.00 MIL	3307.20	-6.71	Pass
DSP1.E16:U8.L7 [DSP0_DDR3_EA10]	0.00 MIL:20.00 MIL	3300.01	0.48	Pass
DSP1.D16:U8.R7 [DSP0_DDR3_EA11]	0.00 MIL:20.00 MIL	3300.69	-0.20	Pass
DSP1.E17:U8.N7 [DSP0_DDR3_EA12]	0.00 MIL:20.00 MIL	3297.71	2.78	Pass

Table 1. Example Fly-by Length Matching Report (continued)

	Rule	Length (mils)	Skew (mils)	Check
DSP1.C16:U8.T3 [DSP0_DDR3_EA13]	0.00 MIL:20.00 MIL	3310.23	-9.74	Pass
DSP1.D17:U8.T7 [DSP0_DDR3_EA14]	0.00 MIL:20.00 MIL	3298.45	2.04	Pass
DSP1.C17:U8.M7 [DSP0_DDR3_EA15]	0.00 MIL:20.00 MIL	3303.47	-2.98	Pass
DSP1.A13:U8.M2 [DSP0_DDR3_EBA_0]	0.00 MIL:20.00 MIL	3312.80	-12.31	Pass
DSP1.B13:U8.N8 [DSP0_DDR3_EBA_1]	0.00 MIL:20.00 MIL	3298.80	1.69	Pass
DSP1.C13:U8.M3 [DSP0_DDR3_EBA_2]	0.00 MIL:20.00 MIL	3311.27	-10.78	Pass
DSP1.C10:U8.J3 [DSP0_DDR3_ERAS#]	0.00 MIL:20.00 MIL	3311.96	-11.47	Pass
DSP1.D12:U8.K3 [DSP0_DDR3_ECAS#]	0.00 MIL:20.00 MIL	3298.97	1.52	Pass
DSP1.E12:U8.L3 [DSP0_DDR3_EWE#]	0.00 MIL:20.00 MIL	3297.74	2.75	Pass
DSP1.C11:U8.L2 [DSP0_DDR3_ECS_0#]	0.00 MIL:20.00 MIL	3302.09	-1.60	Pass
DSP1.D11:U8.K9 [DSP0_DDR3_ECKE_0]	0.00 MIL:20.00 MIL	3300.06	0.43	Pass
DSP1.D13:U8.K1 [DSP0_DDR3_EODT_0]	0.00 MIL:20.00 MIL	3301.15	-0.66	Pass
R_DDR_ADD_U16 (27)				
DSP1.A12:U16.J7 [DSP0_DDR3_ECKP_0]	**Target**	3785.07		**Target**
DSP1.B12:U16.K7 [DSP0_DDR3_ECKN_0]	0.00 MIL:20.00 MIL	3784.91	0.16	Pass
DSP1.A14:U16.N3 [DSP0_DDR3_EA0]	0.00 MIL:20.00 MIL	3789.82	-4.75	Pass
DSP1.B14:U16.P7 [DSP0_DDR3_EA1]	0.00 MIL:20.00 MIL	3773.36	11.71	Pass
DSP1.F14:U16.P3 [DSP0_DDR3_EA2]	0.00 MIL:20.00 MIL	3785.92	-0.85	Pass
DSP1.F13:U16.N2 [DSP0_DDR3_EA3]	0.00 MIL:20.00 MIL	3788.38	-3.31	Pass
DSP1.A15:U16.P8 [DSP0_DDR3_EA4]	0.00 MIL:20.00 MIL	3769.68	15.39	Pass
DSP1.C15:U16.P2 [DSP0_DDR3_EA5]	0.00 MIL:20.00 MIL	3783.00	2.07	Pass
DSP1.B15:U16.R8 [DSP0_DDR3_EA6]	0.00 MIL:20.00 MIL	3789.52	-4.45	Pass
DSP1.D15:U16.R2 [DSP0_DDR3_EA7]	0.00 MIL:20.00 MIL	3791.81	-6.74	Pass
DSP1.F15:U16.T8 [DSP0_DDR3_EA8]	0.00 MIL:20.00 MIL	3786.50	-1.43	Pass
DSP1.E15:U16.R3 [DSP0_DDR3_EA9]	0.00 MIL:20.00 MIL	3779.32	5.75	Pass
DSP1.E16:U16.L7 [DSP0_DDR3_EA10]	0.00 MIL:20.00 MIL	3771.81	13.26	Pass
DSP1.D16:U16.R7 [DSP0_DDR3_EA11]	0.00 MIL:20.00 MIL	3772.30	12.77	Pass
DSP1.E17:U16.N7 [DSP0_DDR3_EA12]	0.00 MIL:20.00 MIL	3773.14	11.93	Pass
DSP1.C16:U16.T3 [DSP0_DDR3_EA13]	0.00 MIL:20.00 MIL	3779.23	5.84	Pass
DSP1.C17:U16.M7 [DSP0_DDR3_EA15]	0.00 MIL:20.00 MIL	3774.53	10.54	Pass
DSP1.D17:U16.T7 [DSP0_DDR3_EA14]	0.00 MIL:20.00 MIL	3771.04	14.03	Pass
DSP1.A13:U16.M2 [DSP0_DDR3_EBA_0]	0.00 MIL:20.00 MIL	3783.88	1.19	Pass
DSP1.B13:U16.N8 [DSP0_DDR3_EBA_1]	0.00 MIL:20.00 MIL	3770.19	14.88	Pass
DSP1.C13:U16.M3 [DSP0_DDR3_EBA_2]	0.00 MIL:20.00 MIL	3782.44	2.63	Pass
DSP1.C10:U16.J3 [DSP0_DDR3_ERAS#]	0.00 MIL:20.00 MIL	3788.54	-3.47	Pass
DSP1.D12:U16.K3 [DSP0_DDR3_ECAS#]	0.00 MIL:20.00 MIL	3772.55	12.52	Pass
DSP1.E12:U16.L3 [DSP0_DDR3_EWE#]	0.00 MIL:20.00 MIL	3771.67	13.40	Pass
DSP1.C11:U16.L2 [DSP0_DDR3_ECS_0#]	0.00 MIL:20.00 MIL	3774.56	10.51	Pass
DSP1.D11:U16.K9 [DSP0_DDR3_ECKE_0]	0.00 MIL:20.00 MIL	3771.19	13.88	Pass
DSP1.D13:U16.K1 [DSP0_DDR3_EODT_0]	0.00 MIL:20.00 MIL	3772.96	12.11	Pass
R_DDR_ADD_U17 (27)				
DSP1.A12:U17.J7 [DSP0_DDR3_ECKP_0]	**Target**	4296.31		**Target**
DSP1.B12:U17.K7 [DSP0_DDR3_ECKN_0]	0.00 MIL:20.00 MIL	4297.94	-1.63	Pass
DSP1.A14:U17.N3 [DSP0_DDR3_EA0]	0.00 MIL:20.00 MIL	4314.63	-18.32	Pass
DSP1.B14:U17.P7 [DSP0_DDR3_EA1]	0.00 MIL:20.00 MIL	4297.84	-1.53	Pass
DSP1.F14:U17.P3 [DSP0_DDR3_EA2]	0.00 MIL:20.00 MIL	4311.64	-15.33	Pass
DSP1.F13:U17.N2 [DSP0_DDR3_EA3]	0.00 MIL:20.00 MIL	4313.36	-17.05	Pass

Table 1. Example Fly-by Length Matching Report (continued)

	Rule	Length (mils)	Skew (mils)	Check
DSP1.A15:U17.P8 [DSP0_DDR3_EA4]	0.00 MIL:20.00 MIL	4294.07	2.24	Pass
DSP1.C15:U17.P2 [DSP0_DDR3_EA5]	0.00 MIL:20.00 MIL	4296.38	-0.07	Pass
DSP1.B15:U17.R8 [DSP0_DDR3_EA6]	0.00 MIL:20.00 MIL	4313.41	-17.10	Pass
DSP1.F15:U17.T8 [DSP0_DDR3_EA8]	0.00 MIL:20.00 MIL	4312.51	-16.20	Pass
DSP1.D15:U17.R2 [DSP0_DDR3_EA7]	0.00 MIL:20.00 MIL	4310.46	-14.15	Pass
DSP1.E15:U17.R3 [DSP0_DDR3_EA9]	0.00 MIL:20.00 MIL	4303.39	-7.08	Pass
DSP1.E16:U17.L7 [DSP0_DDR3_EA10]	0.00 MIL:20.00 MIL	4295.65	0.66	Pass
DSP1.D16:U17.R7 [DSP0_DDR3_EA11]	0.00 MIL:20.00 MIL	4296.40	-0.09	Pass
DSP1.E17:U17.N7 [DSP0_DDR3_EA12]	0.00 MIL:20.00 MIL	4298.13	-1.82	Pass
DSP1.C16:U17.T3 [DSP0_DDR3_EA13]	0.00 MIL:20.00 MIL	4305.57	-9.26	Pass
DSP1.D17:U17.T7 [DSP0_DDR3_EA14]	0.00 MIL:20.00 MIL	4295.72	0.59	Pass
DSP1.C17:U17.M7 [DSP0_DDR3_EA15]	0.00 MIL:20.00 MIL	4298.90	-2.59	Pass
DSP1.C10:U17.J3 [DSP0_DDR3_ERAS#]	0.00 MIL:20.00 MIL	4310.07	-13.76	Pass
DSP1.D12:U17.K3 [DSP0_DDR3_ECAS#]	0.00 MIL:20.00 MIL	4298.02	-1.71	Pass
DSP1.E12:U17.L3 [DSP0_DDR3_EWE#]	0.00 MIL:20.00 MIL	4296.51	-0.20	Pass
DSP1.A13:U17.M2 [DSP0_DDR3_EBA_0]	0.00 MIL:20.00 MIL	4307.56	-11.25	Pass
DSP1.B13:U17.N8 [DSP0_DDR3_EBA_1]	0.00 MIL:20.00 MIL	4294.55	1.76	Pass
DSP1.C13:U17.M3 [DSP0_DDR3_EBA_2]	0.00 MIL:20.00 MIL	4306.94	-10.63	Pass
DSP1.C11:U17.L2 [DSP0_DDR3_ECS_0#]	0.00 MIL:20.00 MIL	4298.91	-2.60	Pass
DSP1.D11:U17.K9 [DSP0_DDR3_ECKE_0]	0.00 MIL:20.00 MIL	4295.83	0.48	Pass
DSP1.D13:U17.K1 [DSP0_DDR3_EODT_0]	0.00 MIL:20.00 MIL	4297.31	-1.00	Pass

1. U4 is the first DDR3 SDRAM and the other SDRAMs are in the following fly-by order: U5, U8, U16, and U17.
2. The rule on DSP0_DDR3_ECK[p/n] is matching within ± 1 mil from the PHY to each SDRAM chip sequentially (CLKN <= CLKP ± 1 mil)
3. The rule on ADDR, CMD and CTL is matching within ± 20 mils of the DSP0_DDR3_ECK[p/n] from the PHY to each SDRAM chip sequentially (ADDR/CMD/CTL ≦ CLK ± 20 mils).

Table 2 is an example of a length matching report generated by CAD software showing that the DATA group length matching rules have been met.

Table 2. Example Data Group Length Matching Report

	Rule	Length (mils)	Skew (mils)	Check
R_DDR_DATA0 (11)				
U4.G3:DSP1.C29 [DSP0_DDR3_EDQSN_0]	0.00 MIL:2.00 MIL	1261.48	0.34	Pass
U4.F3:DSP1.C28 [DSP0_DDR3_EDQSP_0]	**TARGET**	1261.82	0.00	
U4.E3:DSP1.E28 [DSP0_DDR3_EDQ0]	0.00 MIL:15.00 MIL	1260.29	1.53	Pass
U4.F7:DSP1.D29 [DSP0_DDR3_EDQ1]	0.00 MIL:15.00 MIL	1253.80	8.02	Pass
U4.F2:DSP1.E27 [DSP0_DDR3_EDQ2]	0.00 MIL:15.00 MIL	1257.77	4.05	Pass
U4.F8:DSP1.D28 [DSP0_DDR3_EDQ3]	0.00 MIL:15.00 MIL	1253.72	8.10	Pass
U4.H3:DSP1.D27 [DSP0_DDR3_EDQ4]	0.00 MIL:15.00 MIL	1258.21	3.61	Pass
U4.H8:DSP1.B28 [DSP0_DDR3_EDQ5]	0.00 MIL:15.00 MIL	1251.47	10.35	Pass
U4.G2:DSP1.E26 [DSP0_DDR3_EDQ6]	0.00 MIL:15.00 MIL	1259.64	2.18	Pass
U4.H7:DSP1.F25 [DSP0_DDR3_EDQ7]	0.00 MIL:15.00 MIL	1255.74	6.08	Pass
U4.E7:DSP1.E29 [DSP0_DDR3_EDM_0]	0.00 MIL:15.00 MIL	1259.68	2.14	Pass
R_DDR_DATA1 (11)				
U4.B7:DSP1.B27 [DSP0_DDR3_EDQSN_1]	0.00 MIL:2.00 MIL	1141.75	-1.95	Pass
U4.C7:DSP1.A27 [DSP0_DDR3_EDQSP_1]	**TARGET**	1139.80	0.00	

Table 2. Example Data Group Length Matching Report (continued)

	Rule	Length (mils)	Skew (mils)	Check
U4.D7:DSP1.F24 [DSP0_DDR3_EDQ8]	0.00 MIL:15.00 MIL	1143.58	-3.78	Pass
U4.C3:DSP1.E24 [DSP0_DDR3_EDQ9]	0.00 MIL:15.00 MIL	1154.06	-14.26	Pass
U4.C8:DSP1.E25 [DSP0_DDR3_EDQ10]	0.00 MIL:15.00 MIL	1131.86	7.94	Pass
U4.C2:DSP1.D25 [DSP0_DDR3_EDQ11]	0.00 MIL:15.00 MIL	1141.53	-1.73	Pass
U4.A7:DSP1.D26 [DSP0_DDR3_EDQ12]	0.00 MIL:15.00 MIL	1135.58	4.22	Pass
U4.A2:DSP1.C26 [DSP0_DDR3_EDQ13]	0.00 MIL:15.00 MIL	1141.94	-2.14	Pass
U4.B8:DSP1.B26 [DSP0_DDR3_EDQ14]	0.00 MIL:15.00 MIL	1134.42	5.38	Pass
U4.A3:DSP1.A26 [DSP0_DDR3_EDQ15]	0.00 MIL:15.00 MIL	1136.15	3.65	Pass
U4.D3:DSP1.C27 [DSP0_DDR3_EDM_1]	0.00 MIL:15.00 MIL	1129.70	10.10	Pass
R_DDR_DATA2 (11)				
U5.G3:DSP1.B24 [DSP0_DDR3_EDQSN_2]	0.00 MIL:2.00 MIL	929.27	-0.77	Pass
U5.F3:DSP1.A24 [DSP0_DDR3_EDQSP_2]	**TARGET**	928.50	0.00	
U5.E3:DSP1.F23 [DSP0_DDR3_EDQ16]	0.00 MIL:15.00 MIL	923.13	5.37	Pass
U5.F7:DSP1.F22 [DSP0_DDR3_EDQ17]	0.00 MIL:15.00 MIL	929.31	-0.81	Pass
U5.F2:DSP1.D24 [DSP0_DDR3_EDQ18]	0.00 MIL:15.00 MIL	927.55	0.95	Pass
U5.F8:DSP1.E23 [DSP0_DDR3_EDQ19]	0.00 MIL:15.00 MIL	934.22	-5.72	Pass
U5.H3:DSP1.A23 [DSP0_DDR3_EDQ20]	0.00 MIL:15.00 MIL	930.06	-1.56	Pass
U5.H8:DSP1.B23 [DSP0_DDR3_EDQ21]	0.00 MIL:15.00 MIL	924.84	3.66	Pass
U5.G2:DSP1.C24 [DSP0_DDR3_EDQ22]	0.00 MIL:15.00 MIL	925.89	2.61	Pass
U5.H7:DSP1.E22 [DSP0_DDR3_EDQ23]	0.00 MIL:15.00 MIL	921.16	7.34	Pass
U5.E7:DSP1.A25 [DSP0_DDR3_EDM_2]	0.00 MIL:15.00 MIL	918.44	10.06	Pass
R_DDR_DATA3 (11)				
U5.B7:DSP1.B21 [DSP0_DDR3_EDQSN_3]	0.00 MIL:2.00 MIL	997.01	-1.71	Pass
U5.C7:DSP1.A21 [DSP0_DDR3_EDQSP_3]	**TARGET**	995.30	0.00	
U5.D7:DSP1.D21 [DSP0_DDR3_EDQ24]	0.00 MIL:15.00 MIL	990.95	4.35	Pass
U5.C3:DSP1.F20 [DSP0_DDR3_EDQ25]	0.00 MIL:15.00 MIL	998.91	-3.61	Pass
U5.C8:DSP1.E21 [DSP0_DDR3_EDQ26]	0.00 MIL:15.00 MIL	983.85	11.45	Pass
U5.C2:DSP1.F21 [DSP0_DDR3_EDQ27]	0.00 MIL:15.00 MIL	1008.48	-13.18	Pass
U5.A7:DSP1.D22 [DSP0_DDR3_EDQ28]	0.00 MIL:15.00 MIL	989.54	5.76	Pass
U5.A2:DSP1.C21 [DSP0_DDR3_EDQ29]	0.00 MIL:15.00 MIL	985.31	9.99	Pass
U5.B8:DSP1.B22 [DSP0_DDR3_EDQ30]	0.00 MIL:15.00 MIL	986.63	8.67	Pass
U5.A3:DSP1.C22 [DSP0_DDR3_EDQ31]	0.00 MIL:15.00 MIL	987.65	7.65	Pass
U5.D3:DSP1.A22 [DSP0_DDR3_EDM_3]	0.00 MIL:15.00 MIL	992.76	2.54	Pass
R_DDR_DATA4 (11)				
U16.F3:DSP1.A9 [DSP0_DDR3_EDQSP_4]	**TARGET**	1121.70	0.00	
U16.G3:DSP1.B9 [DSP0_DDR3_EDQSN_4]	0.00 MIL:2.00 MIL	1120.57	1.13	Pass
U16.E3:DSP1.E10 [DSP0_DDR3_EDQ32]	0.00 MIL:15.00 MIL	1116.86	4.84	Pass
U16.F7:DSP1.D10 [DSP0_DDR3_EDQ33]	0.00 MIL:15.00 MIL	1124.47	-2.77	Pass
U16.F2:DSP1.B10 [DSP0_DDR3_EDQ34]	0.00 MIL:15.00 MIL	1111.58	10.12	Pass
U16.F8:DSP1.D9 [DSP0_DDR3_EDQ35]	0.00 MIL:15.00 MIL	1114.76	6.94	Pass
U16.H3:DSP1.E9 [DSP0_DDR3_EDQ36]	0.00 MIL:15.00 MIL	1130.02	-8.32	Pass
U16.H8:DSP1.C9 [DSP0_DDR3_EDQ37]	0.00 MIL:15.00 MIL	1128.94	-7.24	Pass
U16.G2:DSP1.B8 [DSP0_DDR3_EDQ38]	0.00 MIL:15.00 MIL	1111.45	10.25	Pass
U16.H7:DSP1.E8 [DSP0_DDR3_EDQ39]	0.00 MIL:15.00 MIL	1116.94	4.76	Pass
U16.E7:DSP1.A10 [DSP0_DDR3_EDM_4]	0.00 MIL:15.00 MIL	1128.11	-6.41	Pass
R_DDR_DATA5 (11)				
U16.B7:DSP1.A6 [DSP0_DDR3_EDQSN_5]	0.00 MIL:2.00 MIL	710.27	0.31	Pass

Table 2. Example Data Group Length Matching Report (continued)

	Rule	Length (mils)	Skew (mils)	Check
U16.C7:DSP1.B6 [DSP0_DDR3_EDQSP_5]	**TARGET**	710.58	0.00	
U16.D7:DSP1.A7 [DSP0_DDR3_EDQ40]	0.00 MIL:15.00 MIL	720.25	-9.67	Pass
U16.C3:DSP1.D7 [DSP0_DDR3_EDQ41]	0.00 MIL:15.00 MIL	699.25	11.33	Pass
U16.C8:DSP1.E7 [DSP0_DDR3_EDQ42]	0.00 MIL:15.00 MIL	718.70	-8.12	Pass
U16.C2:DSP1.C7 [DSP0_DDR3_EDQ43]	0.00 MIL:15.00 MIL	700.82	9.76	Pass
U16.A7:DSP1.B7 [DSP0_DDR3_EDQ44]	0.00 MIL:15.00 MIL	699.23	11.35	Pass
U16.A2:DSP1.E6 [DSP0_DDR3_EDQ45]	0.00 MIL:15.00 MIL	703.39	7.19	Pass
U16.B8:DSP1.D6 [DSP0_DDR3_EDQ46]	0.00 MIL:15.00 MIL	709.46	1.12	Pass
U16.A3:DSP1.C6 [DSP0_DDR3_EDQ47]	0.00 MIL:15.00 MIL	699.88	10.70	Pass
U16.D3:DSP1.A8 [DSP0_DDR3_EDM_5]	0.00 MIL:15.00 MIL	697.94	12.64	Pass
R_DDR_DATA6 (11)				
U17.F3:DSP1.B3 [DSP0_DDR3_EDQSP_6]	**TARGET**	1206.95	0.00	
U17.G3:DSP1.A3 [DSP0_DDR3_EDQSN_6]	0.00 MIL:2.00 MIL	1206.79	0.16	Pass
U17.E3:DSP1.C5 [DSP0_DDR3_EDQ48]	0.00 MIL:15.00 MIL	1202.33	4.62	Pass
U17.F7:DSP1.A5 [DSP0_DDR3_EDQ49]	0.00 MIL:15.00 MIL	1201.11	5.84	Pass
U17.F2:DSP1.B4 [DSP0_DDR3_EDQ50]	0.00 MIL:15.00 MIL	1209.54	-2.59	Pass
U17.F8:DSP1.A4 [DSP0_DDR3_EDQ51]	0.00 MIL:15.00 MIL	1203.31	3.64	Pass
U17.H3:DSP1.D4 [DSP0_DDR3_EDQ52]	0.00 MIL:15.00 MIL	1205.54	1.41	Pass
U17.H8:DSP1.E4 [DSP0_DDR3_EDQ53]	0.00 MIL:15.00 MIL	1212.18	-5.23	Pass
U17.G2:DSP1.C4 [DSP0_DDR3_EDQ54]	0.00 MIL:15.00 MIL	1210.11	-3.16	Pass
U17.H7:DSP1.C3 [DSP0_DDR3_EDQ55]	0.00 MIL:15.00 MIL	1203.16	3.79	Pass
U17.E7:DSP1.B5 [DSP0_DDR3_EDM_6]	0.00 MIL:15.00 MIL	1201.02	5.93	Pass
R_DDR_DATA7 (11)				
U17.B7:DSP1.C1 [DSP0_DDR3_EDQSN_7]	0.00 MIL:2.00 MIL	1209.00	-0.12	Pass
U17.C7:DSP1.D1 [DSP0_DDR3_EDQSP_7]	**TARGET**	1208.88	0.00	
U17.D7:DSP1.F4 [DSP0_DDR3_EDQ56]	0.00 MIL:15.00 MIL	1223.84	-14.96	Pass
U17.C3:DSP1.D2 [DSP0_DDR3_EDQ57]	0.00 MIL:15.00 MIL	1203.94	4.94	Pass
U17.C8:DSP1.E2 [DSP0_DDR3_EDQ58]	0.00 MIL:15.00 MIL	1216.92	-8.04	Pass
U17.C2:DSP1.C2 [DSP0_DDR3_EDQ59]	0.00 MIL:15.00 MIL	1203.40	5.48	Pass
U17.A7:DSP1.F2 [DSP0_DDR3_EDQ60]	0.00 MIL:15.00 MIL	1202.33	6.55	Pass
U17.A2:DSP1.F3 [DSP0_DDR3_EDQ61]	0.00 MIL:15.00 MIL	1205.89	2.99	Pass
U17.B8:DSP1.E1 [DSP0_DDR3_EDQ62]	0.00 MIL:15.00 MIL	1206.01	2.87	Pass
U17.A3:DSP1.F1 [DSP0_DDR3_EDQ63]	0.00 MIL:15.00 MIL	1200.11	8.77	Pass
U17.D3:DSP1.B2 [DSP0_DDR3_EDM_7]	0.00 MIL:15.00 MIL	1195.64	13.24	Pass
R_DDR_DATA8 (11)				
U8.G3:DSP1.B19 [DSP0_DDR3_EDQSN_8]	0.00 MIL:2.00 MIL	1074.21	-1.11	Pass
U8.F3:DSP1.A19 [DSP0_DDR3_EDQSP_8]	**TARGET**	1073.10	0.00	
U8.E3:DSP1.E19 [DSP0_DDR3_ECC0]	0.00 MIL:15.00 MIL	1069.54	3.56	Pass
U8.F7:DSP1.C20 [DSP0_DDR3_ECC1]	0.00 MIL:15.00 MIL	1068.21	4.89	Pass
U8.F2:DSP1.D19 [DSP0_DDR3_ECC2]	0.00 MIL:15.00 MIL	1072.31	0.79	Pass
U8.F8:DSP1.B20 [DSP0_DDR3_ECC3]	0.00 MIL:15.00 MIL	1072.71	0.39	Pass
U8.H3:DSP1.C19 [DSP0_DDR3_ECC4]	0.00 MIL:15.00 MIL	1071.71	1.39	Pass
U8.H8:DSP1.C18 [DSP0_DDR3_ECC5]	0.00 MIL:15.00 MIL	1073.60	-0.50	Pass
U8.G2:DSP1.B18 [DSP0_DDR3_ECC6]	0.00 MIL:15.00 MIL	1071.21	1.89	Pass
U8.H7:DSP1.A18 [DSP0_DDR3_ECC7]	0.00 MIL:15.00 MIL	1077.41	-4.31	Pass
U8.E7:DSP1.A20 [DSP0_DDR3_EDM_8]	0.00 MIL:15.00 MIL	1072.71	0.39	Pass

(1) The rule on DSP0_DDR3_EDQS[p/n]_# is matching within ± 1 mil to each SDRAM chip (DQSN_# <= DQSP_# ± 1 mil)

(2) The rule on Data lanes is matching within ±15 mils of their respective DSP0_DDR3_EDQS[p/n]_# from the PHY to each SDRAM chip (DQ/DM ≦ DQS ± 15 mils).

There is an alternative tool in draft form that provides a DDR3 routing rules checklist and a tool for validating length matching requirements are met for KeyStone I devices. This spreadsheet template can be used to validate that the length matching rules have been met. It also summarizes the routing rules listed in the *DDR3 design requirements for KeyStone devices*.

4 References

1. Texas Instruments: *DDR3 design requirements for KeyStone devices*
2. Texas Instruments: *KeyStone I DDR3 initialization*
3. http://www.ti.com/lit/zip/sprabl2
4. Texas Instruments: *Keystone architecture DDR3 memory controller user's guide*

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