Application Report
SLVA343B–June 2009–Revised August 2011

Medium Integrated Power Solution Using a Dual DC/DC Converter and an LDO

Ambreesh Tripathi *PMP - DC/DC Low-Power Converters*

ABSTRACT

This reference design is intended for users designing with the TMS320C6742, TMS320C6746, TMS320C6748, or OMAP-L132/L138 processor. Using sequenced power supplies, this reference design describes a system having a 3.3-V input voltage and a high-efficiency dc/dc converter with integrated FETs for a small, simple design.

Sequenced power supply architectures are becoming commonplace in high-performance microprocessor and digital signal processor (DSP) systems. To save power and increase processing speeds, processor cores have smaller geometry cells and require lower supply voltages than the system bus voltages. Power management in these systems requires special attention. This application report addresses these topics and suggests solutions for output voltage sequencing.

Contents

List of Figures

List of Tables

1 Introduction

In dual voltage architectures, coordinated management of power supplies is necessary to avoid potential problems and ensure reliable performance. Power supply designers must consider the timing and voltage differences between core and input/output (I/O) voltage supplies during power-up and power-down operations.

Sequencing refers to the order, timing, and differential in which the two voltage rails are powered up and down. A system designed without proper sequencing may be at risk for two types of failures. The first of these represents a threat to the long-term reliability of the dual voltage device, whereas the second is more immediate, with the possibility of damaging interface circuits in the processor or system devices such as memory, logic or data converter integrated circuits (IC).

Another potential problem with improper supply sequencing is bus contention. Bus contention is a condition when the processor and another device both attempt to control a bidirectional bus during power up. Bus contention may also affect I/O reliability. Power supply designers must check the requirements regarding bus contention for individual devices.

The power-on sequencing for the OMAP-L132/L138, TMS320C6742, TMS320C6746, and TMS320C6748 are shown in Table 1. No specific voltage ramp rate is required for any of the supplies as long as the 3.3-V rail never exceeds the 1.8-V rail by more than 2 V.

2 Power Requirements

The power requirements are as specified in Table 1.

Table 1. Power Requirements

	PIN NAME	VOLTAGE [1] [2] (V)	Imax (mA)	TOLERANCE	SEQUENCING ORDER	TIMING DELAY
I/O	RTC_CVDD	1.2	1	–25%, +10%	1[3]	
Core	CVDD[4]	1 / 1.1 / 1.2	600	–9.75%, +10%	2	
I/O	RVDD, PLL0_VDDA, PLL1_VDDA, SATA_VDD, USB_CVDD, USB0_VDDA12	1.2	200	–5%, +10%	3	
I/O	USB0_VDDA18, USB1_VDDA18, DDR_DVDD18, SATA_VDDR, DVDD18	1.8	180	±5%	4	
I/O	USB0_VDDA33, USB1_VDDA33	3.3	24	±5%	5	
I/O	DVDD3318_A, DVDD3318_B, DVDD3318_C	1.8 / 3.3	50 / 90[5]	±5%	4 / 5	

(1) If 1.8-V LVCMOS is used, power rails up with the 1.8-V rails. If 3.3-V LVCMOS is used, power it up with the ANALOG33 rails (VDDA33_USB0/1).

(2) No specific voltage ramp rate is required for any of the supplies LVCMOS33 (USB0_VDDA33, USB1_VDDA33) if STATIC18 (USB0_VDDA18, USB1_VDDA18, DDR_DVDD18, SATA_VDDR, DVDD18) never exceeds more than 2 volts.

(3) If RTC is not used/maintained on a separate supply, it can be included in the STATIC12 (fixed 1.2 V) group.

(4) If using CVDD at fixed 1.2 V, all 1.2-V rails may be combined.

(5) If DVDD3318_A, B, and C are powered independently, maximum power for each rail is 1/3 the above maximum power.

3 Features

The design uses the following high-efficiency dc/dc converter with integrated FETs.

INPUT VOLTAGE	**~3.3 V**
	INTEGRATION AND HIGH EFFICIENCY (Without DVFS)
COMBINE RTC AND STATIC 1.2	
Core 1.2 V at 600 mA	TPS62420 (DCDC1)
Static 1.2 V + VRTC at 251 mA	
Static 1.8 V at 230 mA	TPS62420 (DCDC2)
Static 3.3 V at 115 mA	TPS71733 (DRV)

In the preceding table, VRTC is included in the STATIC12 (fixed 1.2 V) group.

TPS62420

- High efficiency – up to 95%
- VIN range From 2.5 V to 6 V
- Output current 600 mA and 1000 mA
- EasyScale™ optional 1-pin serial interface for dynamic output voltage adjustment
- Power-Save mode at light-load currents
- Available in a 10-pin QFN (3×3mm)

TPS71733

- 150-mA low-dropout (LDO) regulator with enable
- Low noise: 30 µV typical (100 Hz to 100 kHz)
- Excellent load/line transient response
- Small SC70-5, 2 mm × 2 mm SON-6, and 1,5 mm × 1,5 mm SON-6 packages

More information on the devices can be found in the data sheets.

- TPS62420; literature number SLVS676
- TPS71733; literature number SBVS068

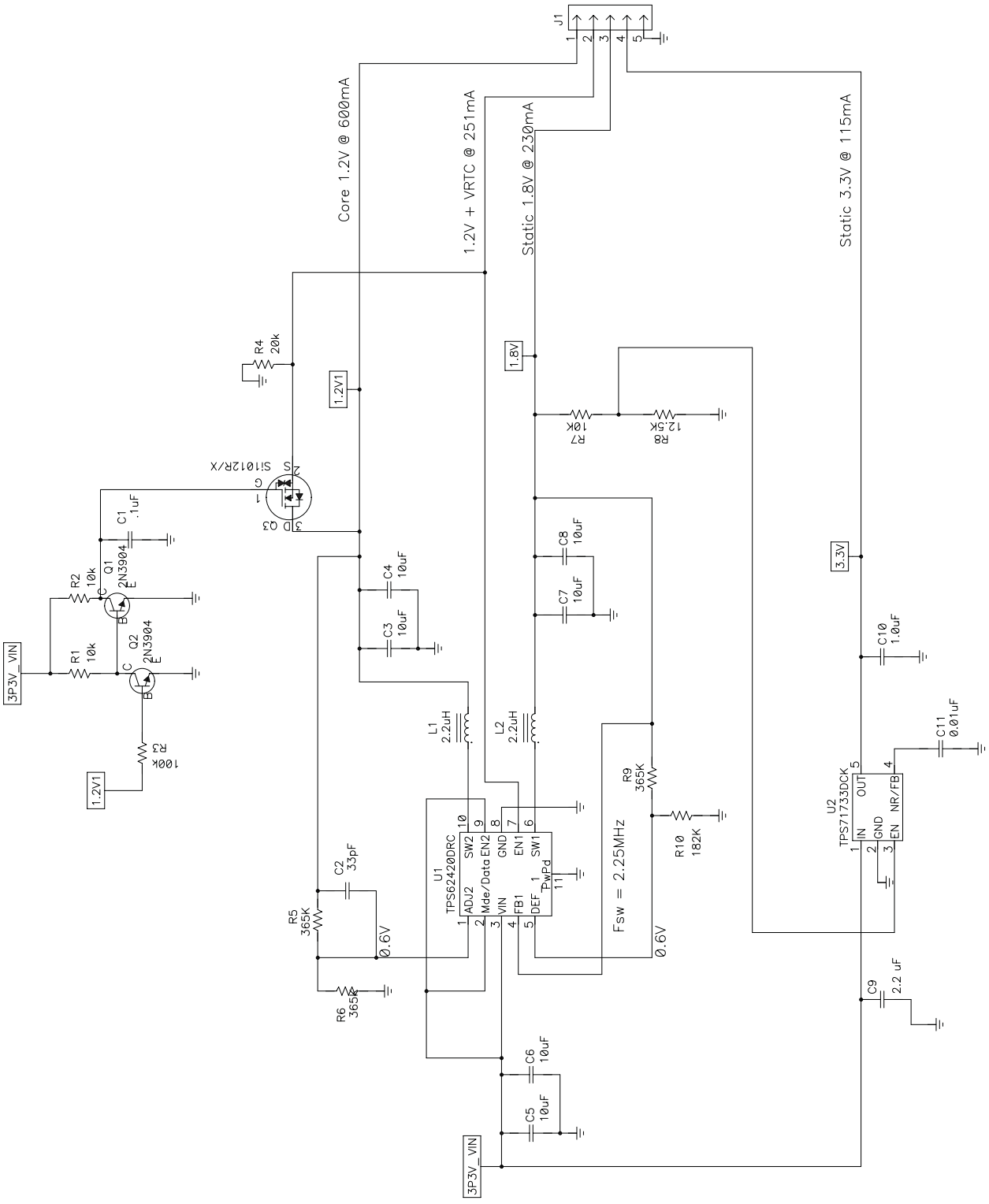
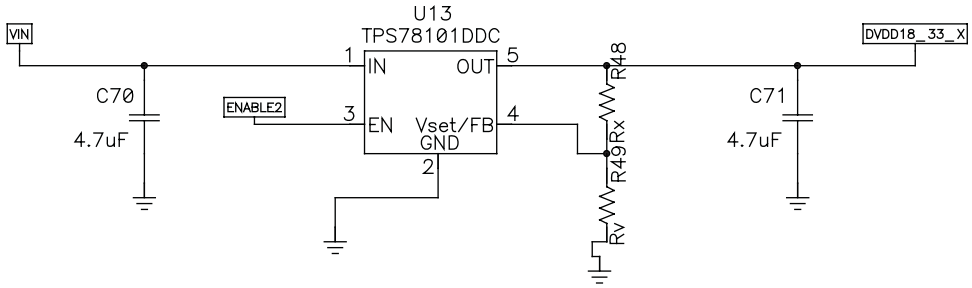


Figure 1. PMP4978 Reference Design Schematic

Proper sequencing is ensured in the design with the use of a NPN transistor and a N-channel MOSFET. As required, Core 1.2 V at 600 mA comes first , which in turn pulls up the gate of a N-channel MOSFET to 3.3 V with the use of a NPN transistor. Then 1.2 V + VRTC at 251 mA comes up. This 1.2 V further enables the DCDC1 and sequentially 1.8 V comes up, which again enables an LDO to give 3.3 V at 115 mA.



(1) Use three such LDOs to power up DVDDA, DVDDB, and DVDDC. (It can be either 1.8 V or 3.3 V.)

(2) Rx = 0.499 MΩ, Ry = 1 MΩ for Vout = 1.8 V

(3) Rx = 1.8 MΩ, Ry = 1 MΩ for Vout = 3.3 V

(4) For proper sequencing of output, enable of the LDOs are fed either from a 1.2-V output from TPS62420 DCDC2 if DVDDX is 1.8 V or from a 1.8-V output from TPS62420 DCDC1 if DVDDX is 3.3 V.

Figure 2. Optional Circuit for DVDD_A, DVDD_B and DVDD_C

4 Bill of Materials

Table 2. PMP4978 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR	Area
1	C1	0.1 µF	Capacitor, Ceramic, 50V, C0G, 5%	0603	Std	Std	5650
1	C2	33pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	Std	Std	5650
6	C3	10 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	C2012X5R0J106M	TDK	10560
	C4	10 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	C2012X5R0J106M	TDK	10560
	C5	10 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	C2012X5R0J106M	TDK	10560
	C6	10 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	C2012X5R0J106M	TDK	10560
	C7	10 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	C2012X5R0J106M	TDK	10560
	C8	10 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	C2012X5R0J106M	TDK	10560
1	C9	2.2 µF	Capacitor, Ceramic, 16V, X5R, 10%	0603	C1608X5R1C225K	TDK	5650
1	C10	1.0 µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	C1608X5R1E105K	TDK	5650
1	C11	0.01 µF	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H103K	TDK	5650
1	J1	PEC36SAAN	Header, Male 5-pin, 100mil spacing, (36-pin strip)	0.100 inch × 5	PEC36SAAN	Sullins	60000
2	L1	2.2 µH	Inductor, SMT, 1.2A, 100mΩ	0.102 × 0.110 inch	VLF3014AT-2R2M1R2	TDK	24,7
	L2	2.2 µH	Inductor, SMT, 1.2A, 100mΩ	0.102 × 0.110 inch	VLF3014AT-2R2M1R2	TDK	24,7
2	Q1	2N3904	Transistor, NPN, 40V, 200mA, 625mW	TO-92	2N3904	Fairchild	37800
	Q2	2N3904	Transistor, NPN, 40V, 200mA, 625mW	TO-92	2N3904	Fairchild	37800
1	Q3	Si1012R/X	MOSFET, N-ch, 20V, 600mA, 0.7ohms	SC89-3	Si1012R/X	Vishay	12125
2	R1	10k	Resistor, Chip, 1/16W, 1%	0603	CRCW0603-xxxx-F	Vishay	9100
	R2	10k	Resistor, Chip, 1/16W, 1%	0603	CRCW0603-xxxx-F	Vishay	9100
1	R3	100k	Resistor, Chip, 1/16W, 1%	0603	CRCW0603-xxxx-F	Vishay	9100
1	R4	20k	Resistor, Chip, 1/16W, 1%	0603	CRCW0603-xxxx-F	Vishay	9100
3	R5	365K	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
	R6	365K	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
1	R7	10K	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
1	R8	12.5K	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
	R9	365K	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
1	R10	182K	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
1	U1	TPS62420DRC	IC, 2.25 MHz Dual Step Down Converter	QFN10	TPS62420DRC	TI	40500
1	U2	TPS71733DCK	IC, 150mA, Low Iq, Wide Bandwidth, LDO Linear Regulators	SC70	TPS71728DCK	TI	18.6

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.

2. These assemblies must be clean and free from flux and all contaminants. Failure to use clean flux is unacceptable.

3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.

4. Reference designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

4.1 Test Results

The start-up waveform (Figure 3) specifies the sequencing order that is required.

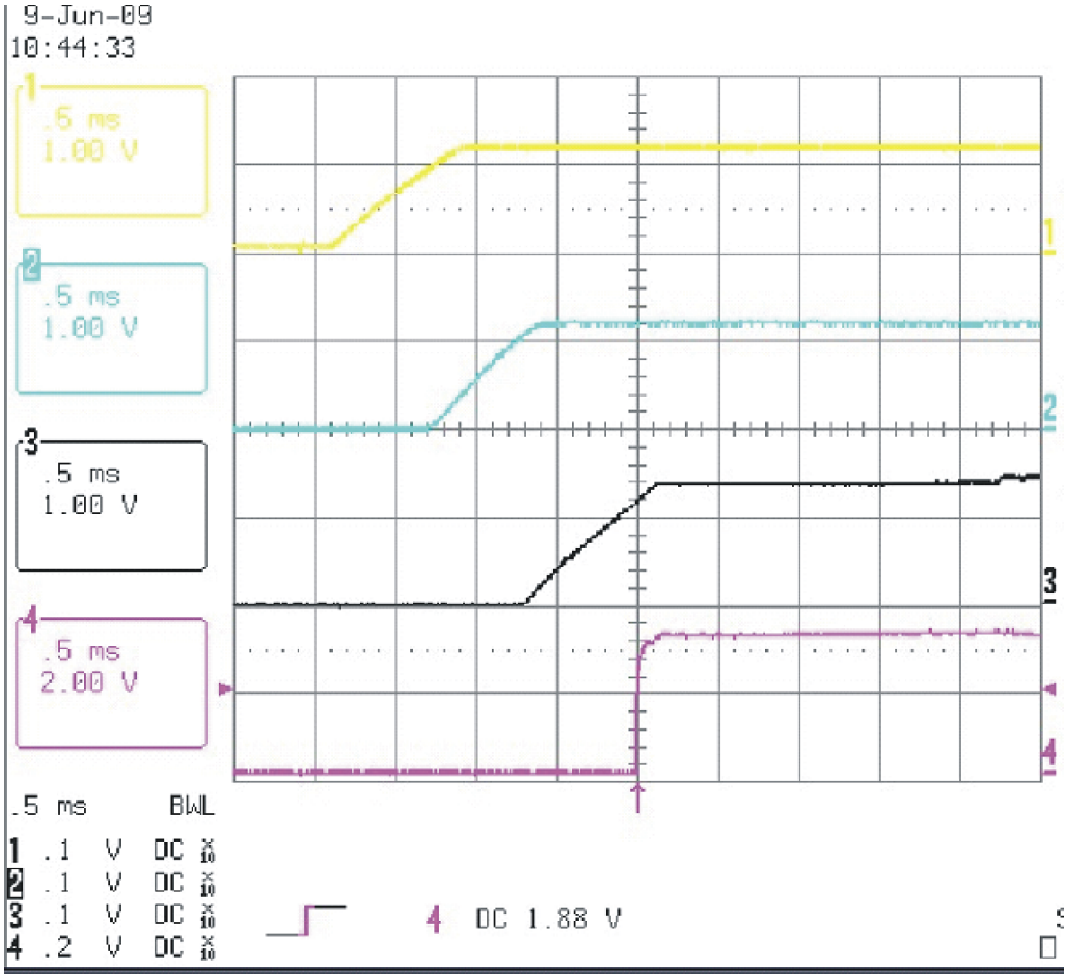


Figure 3. Sequencing in Start-up Waveform

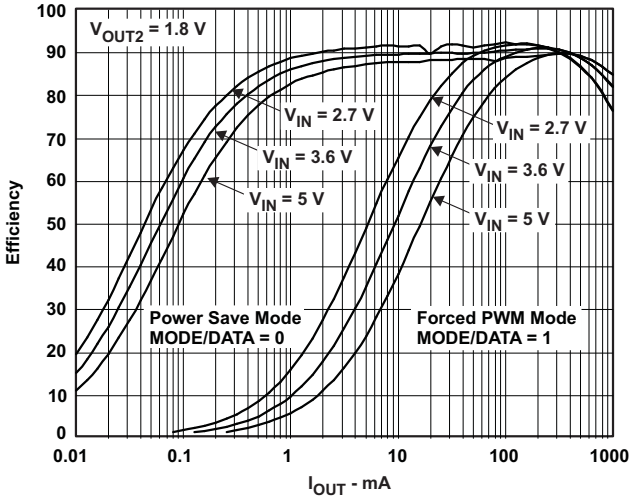


Figure 4. Efficiency V_{OUT2} = 1.8 V

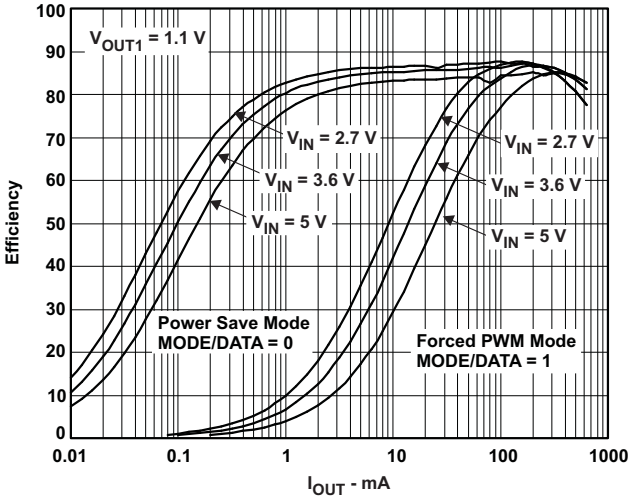


Figure 5. Efficiency V_{OUT1} = 1.1 V

Revision History

Changes from A Revision (May, 2010) to B Revision	Page
• Updated references to *OMAP-L138* to include *OMAP-L132* devices	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connctivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265