Application Report
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Migrating From TMS320DM644x v.2.1 ROM Bootloader to 2.3 Version

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ABSTRACT

This application report describes device considerations to migrate a design based on a TI OMAP3530 application processor to one based on a TI AM37x System-on-Chip (SoC) application processor. These two devices are based on similar ARM CPU cores, feature Neon and SGX graphics processors, and a mixture of memory and other peripherals useful in a system environment. The details for performing migration from an OMAP3530 device to a AM37x device are discussed in this document; therefore, familiarity with the OMAP3530 device and its documentation is assumed. Note that all of the documentation referenced in this migration guide can be found on the TI website located in the two device-specific product folders at:

- OMAP3530 - http://focus.ti.com/docs/prod/folders/print/omap3530.html
- AM37x -

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1 Basic Feature Comparison

Table 1 shows a comparison of the basic features of the OMAP35xx and the AM/DM37xx. The remainder of this document presents a comparison of these features in greater detail, and also provides references to the appropriate documentation for further information.

Table 1. Basic Feature Comparison

RTM (Data sheet Available)	1Q10	Samples Now
Device Family		
Device Family	AM3703 - CortexA8 AM3715 - CortexA8 + SGX 530 DM3725 - CortexA8 + IVA2.2 DM3730 - CortexA8 + IVA2.2 + SGX 530	OMAP3703 - CortexA8 OMAP3715 - CortexA8 + SGX 530 OMAP3725 - CortexA8 + IVA2.2 OMAP3730 - CortexA8 + IVA2.2 + SGX 530
Package Options		
Packages	CBP - 0.4 mm bottom, 0.5 mm top CBC - 0.5 mm bottom, 0.65 mm top CUS - .65 mm bottom. [layout using .8 mm rules]	CBB - 0.4 mm bottom, 0.5 mm top CBC - 0.5 mm bottom, 0.65 mm top CUS - .65 mm bottom. [layout using .8 mmrules]
Co-Processors and Subsystems	r3p2; 32k L1 I$ & 32k D$. Cortex-A8 720 MHz	r1p7; 16k L1 I$ & 16k D$. Cortex-A8
CortexA8 Processor	Increase to 192 MHz	110 MHz
2D/3D Graphics Accelerator	Increase to 620 MHz	520 MHz
IVA2.2 Subsystem	Y	Y
Neon Co-Processor	Updated linked list	Y
System DMA		
Memory Interfaces:		
SDRC		
SDRAM Controller	Increase to 200 MHz	166 MHz
SDRAM Memory Scheduler (SMS)	Y	Y
Rotation Engine	Y	Y
Mobile DDR SDRAM (mDDR)	Y	Y
Width (bits)	16,32	16,32
GPMC	Increased addressing space 2 GB (A11 is available on CBP PoP side & CBC bottom side only)	128 MB per CS, 1 GB total address space
Chips Selects	Y	Y
Wait Pins	Y	Y
Width (bits)	8,16	8,16
POP	(CBP & CBC Package)	(CBB & CBC Package)
Discrete Memory Interface	(CUS Package only)	(CBB & CUS Package)
Video Interfaces:		
Camera ISP		
Additional Dual Camera Schemes	Y	Y
Parallel Interface	Y	Y
Previewer	Y	Y
Resizer	Y	Y
H3A	Y	Y
Histogram	Y	Y
CCDC	Y	
Display Subsystem	Additional dual display schemes	Y
Display Controller (LCD and TV Output)	Y	NDA

Table 1. Basic Feature Comparison (continued)

RTM (Data sheet Available)	1Q10	Samples Now
Remote Frame Buffer Interface (RFBI)	Mutually exclusive with parallel I/F	NDA
MIPI DSI	NDA	NDA
Video Encoder (VENC)	Y	Y

Table 1. Basic Feature Comparison (continued)

RTM (Data sheet Available)	1Q10	Samples Now
Macrovision	NDA	NDA
Serial Communication:		
McBSP		
McBSP1	Y	Y
McBSP2	Y	Y
McBSP3	Y	Y
McBSP4	Y	Y
McBSP5	Y	Y
Multichannel SPI		
McSPI1	Y	Y
McSPI2	Y	Y
McSPI3	Y	Y
McSPI4	Y	Y
USB OTG	New mentor core 1,8 Rev	Y
USB Host		
USB1 (all features)	Y	Y
USB2 (all features)	Y	Y
USB3 (all features)	Y	Y
HDQ/1-Wire	Y	Y
UART/IrDA/CIR		
UART1	Y	Y
UART2	Y	Y
UART3 / IrDA	Y	Y
UART4	Y	N
I2C		
I2C1	Y	Y
I2C2	Y	Y
I2C3	Y	Y
I2C4	Y	Y
Removable Media:		
MMC/SD/SDIO		
MMC1/SDIO1	Only 4 bit interface supported	Y
MMC2/SDIO2	Y	Y
MMC3/SDIO3	Y	Y
Memory Stick Pro	NDA-only	NDA-only
Univeral Subscriber Identity Module (USIM)	Not available on CUS package	NDA-only
Power, Reset, and Clock Management		
All Features	Various PM features updated	Y
Test Interfaces		
JTAG	Y	Y
ETK (trace)	Y	Y
Misc		
GP Timer (x12)	Y	Y
Watchdog Timer (x3)	Y	Y
32-kHz Sync Timer	Y	Y
GPIO	Y	Y

2 General Migration Careabouts

37xx is a drop-in replacement for the OMAP35x on the same printed circuit board (PCB) if:

- Camera and displays are used in the same configuration, as is the case for OMAP35x
- If using CBB, OMAP35x is used with the memory PoP-ed
  - SDRC signals are not available at the bottom of CBP [0.4 mm pacakage] in AM/DM37xx.
- MultiMedia Card (MMC1) 8 bit are not used with OMAP35x
- Two discrete components need to change compared to OMAP34xx
  - One discrete component (capacitor) needs to be changed, but the PCB does not change
  - If AVDAC is used, then a capacitor is changed to a resistor on the board and other resistor values need to be updated; but the PCB does not change.

37xx requires some software changes for:

- New pin multiplexing options that have been added based on customer feedback and for ease of use
- Register definitions are changed for some legacy features and new registers are added to enable new features such as new camera and display configurations, etc.
- To support new IPs and modules, e.g., ISP2P and ARM r3p2, etc.
- To configure PHYs, DPLLs, i.e., any change related to technology migration (see section **Error! Reference source not found**)

PCB changes may be needed to enable OMAP36x enhancements:

- To enable new technology features and configurations for 37xx, e.g., body bias, improved crystal mode jitter, AVDAC, etc.
- To enable new peripheral capabilities such as enhanced camera and display support
- To enable use of 720p display on parallel port
- Some interfaces are removed/updated such as MMC1 being 4 bits vs. 8 bits on OMAP35xx; if used the PCB may require a change.

2.1 Hardware Migration

This section discusses ... ***to be provided by engineer***.

2.1.1 Crystal Oscillator

AM37x crystal oscillator has a dedicated ground, SYS_XTALGND, that is used to improve jitter versus the OMAP35xx version. Implementation is done in such a way that it has no impact on the previously designed OMAP5xx PCB. A VSS ball has been updated to the SYS_XTALGND ball. When AM37xx is mounted on a 35xx board, then SYS_XTALGND is connected to the common ground. In that case, jitter performance is the same as OMAP35xx. When AM37xx is mounted on a 37xx optimized board, SYS_XTALGND is connected as shown in Figure 1 and jitter is improved versus on the OMAP35xx.

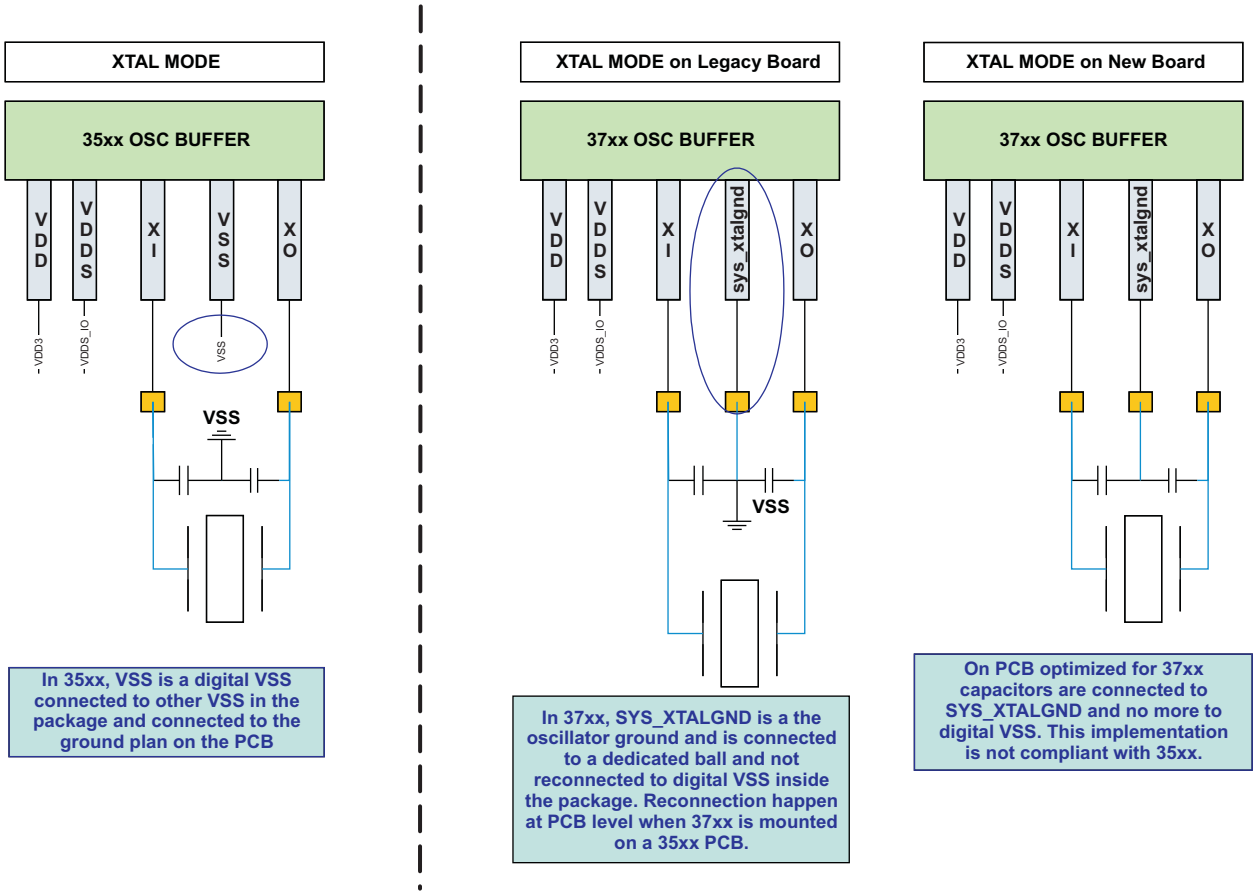

Figure 1. Crystal Oscillator Implementation

2.1.2 AVDAC Channels

Device supports composite and S-video through two GS70 channels: Channel1 and Channel2. Channel1 handles the composite or Luma signals and Channel2 handles the Chroma signals. Channel2 is used only in S-Video mode; TV load detection is only supported on Channel1. Both channels are supplied from the same VDDA/VSSA balls, only Channel1 RSET is balled out. The GS70 AVDAC does not require a reference voltage decoupling anymore, the OMAP35xx tv_vref ball is no longer used for that purpose. The ball is reused to externally set the operating reference current. OMAP35xx boards must be reworked to remove the capacitor and replace it with a resistor.

AM/DM37xx requires two balls for the filtering capacitors, logic and array outputs, where OMAP35xx only had one:

- OMAP35xx cap_vdd_wkup ball is reused for AM/DM37xx cap_vddu_wkup_logic (AA15) with the same capacitor value: 1uF
- OMAP35xx cap_vdd_dsi free ball (see section **Error! Reference source not found**) is used for AM/DM37xx cap_vddu_array (AH20) with the capacitor value: 1uF

OMAP35xx boards must be reworked to remove the 100 nF DSI capacitor and replace it with a 1 uF array capacitor.

2.1.3 BODY BIAS LDO

AM/DM37xx integrates a totally new GS70 BODY BIAS LDO designed to operate in three modes: forward body bias (FBB), reverse body bias (RBB), and bypass mode.

FBB boosts performance in weak processes, RBB reduces leakage in strong processes, and bypass mode (disabled, backward compatibility with 35xx). Body bias only operates on the IVA and MPU domains, not the CORE domains.

The body bias LDO is supplied by the same ball as the wakeup LDO and bandgap REF (vdda_wkup_bg_bb). A stability capacitor on the LDO output is required when the feature is enabled. A new ball was needed in AM/DM37xx for cap_vdd_bb_mpu_iva and the ball selected for physical reasons is U4. On OMAP35xx, U4 is the analog test output (bg_testout) ball: OMAP35xx boards have this ball NC on the PCB; as long as the feature is not activated on the 37xx die (bypass mode), board compatibility is insured. Customers wanting to enable this feature need a board rework to place a 1uF BB capacitor to ground.

2.2 Package Specific Migration Careabouts

This section discusses ... ***to be provided by engineer***.

2.2.1 CBB Package [0.4 mm] Processor

Table 2. Missing Table

Table 3. Missing Table

2.2.2 CBC Package [0.5 mm] Processor

Table 4. CBC Ballmap Bottom Side Differences

Pin Number	35xx Data Sheet Names	37xx Data Sheet Names
A2	SYS_OPMCSWS	VSENSE
A4		GPMC_A11
AD18	VDDS_CSI2	VDDS_CSIPHY2
AE19	CAP_VDD_DSI	CAP_VDDU_ARRAY
AF1	NC	ATESTV
AF23	VSS	SYS_XTALGND
B1	SYS_IPMCSWS	IFORCE
D6	BG_TESTOUT	CAP_VDD_BB_MPU_IVA
K13	VDDS_DPLL	VDDA_DPLLS_DLL
K14	CAP_VDD_WKUP	CAP_VDDU_WKUP_LOGIC
L19	VSS_CSIB	VSSA_CSIPHY1
L20	VDDS_CSIB	VDDA_CSIPHY1
M20	MMC1_DAT4	SIM_IO
P17	MMC1_DAT5	SIM_CLK
P18	MMC1_DAT6	SIM_PWRCTRL
P19	MMC1_DAT7	SIM_RST
U24	TV_VFB2	CVIDEO2_VFB
V23	TV_VREF	CVIDEO1_RSET
V26	TV_OUT2	CVIDEO2_OUT
W14	VDDS_WKUP_BG	VDDS_WKUP_BG_BB
W25	TV_VFB1	CVIDEO1_VFB
W26	TV_OUT1	CVIDEO1_OUT

2.2.3 CUS Package [0.65 mm] Processor

Table 5. CUS Ballmap Differences

Pin Number	35xx Data Sheet Names	37xx Data Sheet Names
AA23	TV_OUT2	CVIDEO2_OUT
AB23	TV_VFB1	CVIDEO1_VFB
AB24	TV_OUT1	CVIDEO1_OUT
AD14	VSS	SYS_XTALOUT
H17	VDD_SRAM_CORE	CAP_VDD_SRAM_CORE
N20	MMC1_DAT6	CAP_VDDU_ARRAY
N21	MMC1_DAT5	CAP_VDD_BB_MPU_IVA
N22	MMC1_DAT4	gpio_126
P24	MMC1_DAT7	gpio_129
U8	VDD_SRAM_MPU_IVA	CAP_VDD_SRAM_MPU_IVA
W15	VSS	SYS_XTALGND
Y12	CAP_VDD_WKUP	cap_vddu_wkup_logic
Y23	TV_VFB2	CVIDEO2_VFB
Y24	TV_VREF	CVIDEO1_RSET

2.3 Operating Conditions Careabouts

This section discusses ... ***to be provided by engineer***.

2.3.1 VDD1 Recommended Operating Condition Comparison

	OMAP35xx									AM/DM37xx					
	OPP3			OPP2			OPP1			OPP3			OPP2		
	Freq	Max	Min	Freq	Max	Min	Freq	Max	Min	Freq	Max	Min	Freq	Max	Min
MPU	500	1.26	1.14	250	1.139	0.998	125	1.023	0.927	600	1.155	1.045	300	1.044	0.903
IVA	360	1.26	1.14	180	1.139	0.998	90	1.023	0.927	520	1.155	1.045	260	1.044	0.903

2.3.2 VDD2 Recommended Operating Condition Comparison

	OMAP35xx									AM/DM37xx					
	OPP3			OPP2			OPP1			OPP3			OPP2		
	Freq	Max	Min	Freq	Max	Min	Freq	Max	Min	Freq	Max	Min	Freq	Max	Min
Core	332	1.207	1.093	200	1.102	0.998	100	1.023	0.927	400	1.208	1.08	200	1.044	0.903
L3	166	1.207	1.093	100	1.102	0.998	50	1.023	0.927	200	1.208	1.08	100	1.044	0.903
SDRC	166	1.207	1.093	100	1.102	0.998	50	1.023	0.927	200	1.208	1.08	100	1.044	0.903
GPMC	83	1.207	1.093	50	1.102	0.998	25	1.023	0.927	100	1.208	1.08	50	1.044	0.903

2.3.3 Max Current Rating Comparison

Parameter		OMAP35xx	AM/DM37xx	
Signal	**Description**	**MAX**	**MAX**	**UNIT**
$C_{vdd\_mpu\_iva}$	Maximum current rating for MPU/IVA2 domain	1200	800	mA
C_{vdd_core}	Maximum current rating for OMAP core domain	490	300	mA
C_{vdds_io}	Maximum current rating for 1.8-V I/O macros	63	60	mA
C_{vdds_mem}	Maximum current rating for memory buffers	37	35	mA

Parameter		OMAP35xx	AM/DM37xx	
Signal	Description	MAX	MAX	UNIT
C_{vdds_sdmmc1}(2)	Maximum current rating for SDMMC1 dual voltage buffers	20	60	mA
C_{vdds_sim} (3)	Maximum current rating for SIM dual voltage buffers	2	2	mA
$C_{vdda\_wkup\_bg\_bb}$	Maximum current rating for wake-up, bandgap and VBB LDOs	6	5	mA
C_{vdda_dac}	Maximum current rating for video buffers and DAC	65	60	mA
$C_{vdda\_dplls\_dll}$	Maximum current rating for MPU, IVA, core DPLLs and DLL	30	30	mA
$C_{vdda\_dpll\_per}$	Maximum current rating for DPLLs (peripherals)	15	12	mA
C_{vdda_sram}	Maximum current rating for SRAM LDOs (common)	41	41	mA

2.3.4 Voltage Decoupling Comparison

Parameter	Ball Number	Max Frequency	OMAP35xx			AM/DM37xx			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
C_{vdds_io} (1)	2	-		100		50	100	150	nF
$C_{vdd\_mpu\_iva}$ (1) (3)	27	-	50	100	120	0.6	1.2	1.8	nF
C_{vdd_core} (1)(4)	34	-	50	100	120	0.6	1.2	1.8	nF
C_{vdds_mem} (1)	21	-		100		50	100	150	nF
C_{vdds_sdmmc1} (1)	1	140		100		50	100	150	nF
C_{vdds_sim} (1)	1	140		100		50	100	150	nF
C_{vdda_sram} (2)	1	40		100		110	220	330	nF
$C_{vdda\_dplls\_dll}$ (2)	1	140	100			50	100	150	nF
$C_{vdda\_dpll\_per}$ (2)	1	140	100			50	100	150	nF
C_{vdda_dac} (2)	1	100	100			50	100	150	nF
$C_{vdda\_csiphy1}$(2)	1	140	220			110	220	330	nF
$C_{vdda\_csiphy2}$ (2)	1	140	220			110	220	330	nF
C_{vdda_dsi} (2)	1	140	220			110	220	330	nF
C_{vdds_sdi} (2)	1	-		220		NA	NA	NA	nF
$C_{vdda\_wkup\_bg\_bb}$ (2)	1	TBD		100		240	470	700	nF
$C_{cap\_vdd\_sram\_mpu\_iva}$ (1)	1	-	0.7	1	1.3	0.7	1	1.3	ìF
$C_{cap\_vdd\_sram\_core}$ (1)	1	-	0.7	1	1.3	0.7	1	1.3	ìF
$C_{cap\_vddu\_wkup\_logic}$ (1)	1	-	0.7	1	1.3	0.7	1	1.3	ìF
$C_{cap\_vddu\_array}$ (1)	1	-	N/A	N/A	N/A	0.7	1	1.3	ìF
$C_{cap\_vdd\_bb\_mpu\_iva}$ (1)	1	-	N/A	N/A	N/A	0.7	1	1.3	ìF

3 Feature Enhancements

3.1 Increase SDRC/L3/ GPMC Clock Frequency

Supports LPDDR1 memories up to 200 MHz due to SDRC and L3 frequency increase from 166 MHz to 200 MHz. 37xx still supports the legacy frequency plan of OMAP35xx. GPMC frequency also would be increased from 100 to 83 MHz.

3.2 Increase With SGX Clock Frequency

SGX530 is now able to run up to 192 MHz. The PRCM.CM_CLKSEL_SGX register has been updated to support additional clocking schemes. The new definition of this register is backward compatible with 35xx definition, i.e., values defined for 35xx have the same meaning in 37xx.

3.3 Support Linked List on System DMA

Some existing registers have been updated and are backward compliant with 35xx. For instance DMA_CAPS_4 has been updated to reflect new DMA capabilities. If masking of reserved bits is not applied in 35xx software, value will be different when ported to 37xx. Additional registers have been added to support linked list features.

3.4 Support Pre-Multiplied Alpha Blending

Display supports pre-multiplied alpha RGB data coming from some HLOSes. When those data are sent to the display controller, hardware alpha multiplication in the display controller can be disabled.

3.5 Support 720p Input in ISP2P

ISP accepts a pixel clock up to 150 MHz with a 8-bits parallel interface instead of 130 MHz on the OMAP35xx.

3.6 DPLL

Bits that are controlled by the PRCM have been added to the DPLL programming model.

3.7 DLL

DLL in 45 nm does not support 72° phase shift mode. Only 90° phase shift is available.

4 Pinmultiplexing Updates

4.1 Additional DSS Multiplexing Schemes

Basically, backword compatibility is available if your pixel clock on DSS interface is ← 60 MHz. But if your pixel clock is higher, 60 < pclk ← 75 MHz, you would need to use pinmux as shown in Table 6.

Table 6. DSS Pinmux

	DPI Controller	OMAP35x Parallel Mode 24-Bit	Legacy Mode AM/DM37x Parallel Mode 24-Bit	AM/DM 37x Parallel Mode 24-Bit
			PClk < 60 MHz	60 MHz < Pclk < 75 MHz
dss_hsync/rfbi_cs0		DSS	DSS	DSS
dss_vsync/rfbi_wr				
dss_pclk/rfbi_rd				
dss_acbias/rfbi_a0				
dss_data0/rfbi_da0	dsi_dx1	DSS [0-5]	DSS [0-5]	NC
dss_data1/rfbi_da1	dsi_dy1			
dss_data2/rfbi_da2	dsi_dx0			
dss_data3/rfbi_da3	dsi_dy0			
dss_data4/rfbi_da4	dsi_dx2			
dss_data5/rfbi_da5	dsi_dy2			
vdda_dsi		pwr rail VIO	pwr rail VIO	pwr rail VIO
vssa_dsi		GND	GND	GND

Table 6. DSS Pinmux (continued)

	DPI Controller	OMAP35x Parallel Mode 24-Bit	Legacy Mode AM/DM37x Parallel Mode 24-Bit	AM/DM 37x Parallel Mode 24-Bit
dss_data6/rfbi_da6		DSS [6-17]	DSS [6-17]	DSS [6-17]
dss_data7/rfbi_da7				
dss_data8/rfbi_da8				
dss_data9//rfbi_da9				
dss_data10/rfbi_da10				
dss_data11/rfbi_da11				
dss_data12/rfbi_da12				
dss_data13/rfbi_da13				
dss_data14/rfbi_da14				
dss_data15/rfbi_da15				
dss_data16/rfbi_te_vsync0				
dss_data17/rfbi_hsync0				
dss_data18/rfbi_te_vsync1	dss_data0/rfbi_da0	DSS [18-23]	DSS [18-23]	DSS [0-5]
dss_data19/rfbi_hsync1	dss_data1/rfbi_da1			
dss_data20/rfbi_cs1	dss_data2/rfbi_da2			
dss_data21	dss_data3/rfbi_da3			
dss_data22	dss_data4/rfbi_da4			
dss_data23	dss_data5/rfbi_da5			
sys_boot0	dss_data18	NC	NC	DSS [18-23]
sys_boot1	dss_data19			
sys_boot3	dss_data20			
sys_boot4	dss_data21			
sys_boot5	dss_data22			
sys_boot6	dss_data23			

4.2 Additional UART3 Multiplexing Scheme

UART3 (TX/RX) has been multiplexed (muxmode 2) on pads DSS_DATA8/9, **refer to Error! Reference source not found**. This is a consequence of the removal of the SDI interface on the customer system; it impacts the customer PCB only.

Table 7. UART3 Pinmux

dss_data8		uart3_rx_irrx
dss_data9		uart3_tx_irtx

4.3 Additional DRM_MSECURE Multiplexing Scheme

DRM_MSECURE has been multiplexed (muxmode 1) on pads ETK D8 and D12, **refer to Error! Reference source not found**. This is a consequence of the new customer system configuration; it impacts the customer PCB only.

Table 8. DRM_MSECURE Pinmux

etk_d8	sys_drm_msecure
etk_d9	sys_secure_indicator
etk_d10	
etk_d11	
etk_d12	sys_drm_msecure

4.4 Additional UART2 Multiplexing Scheme

UART2 (full 4-wire interface) has been multiplexed (muxmode 5) on ULPI. This allows the customer to trace out on UART2 (in a carkit manner) while using UART3 for other functional reasons.

Table 9. UART2 Pinmux

hsusb0_clk				gpio_120	
hsusb0_stp				gpio_121	
hsusb0_dir				gpio_122	
hsusb0_nxt				gpio_124	
hsusb0_data0		uart3_tx_irtx		gpio_125	uart2_tx
hsusb0_data1		uart3_rx_irrx		gpio_130	uart2_rx
hsusb0_data2		uart3_rts_sd		gpio_131	uart2_rts
hsusb0_data3		uart3_cts_rctx		gpio_169	uart2_cts
hsusb0_data4				gpio_188	
hsusb0_data5				gpio_189	
hsusb0_data6				gpio_190	
hsusb0_data7				gpio_191	

5 ROM Code Updates

5.1 ASIC ID Descriptor Update

ASIC-ID descriptor has been updated to discriminate AM/DM37xx from OMAP35xx. AM/DM37xx ASIC-ID is 0x37xx. If this value is used by the software, then it has to be updated to take into account this new value.

5.2 ASIC ID Timeout Update

ASIC-ID time-out has been increased from 300 ms to 3s.

5.3 USB Descriptor Update

The USB descriptor has to discriminate 37xx from 35xx during the USB boot. The Id product field has been updated to 0xD00E. The string descriptor has been updated to *AM/DM37xx*. Those new values have to be taken into account by the software managing the USB boot on the HOST side.

5.4 Improved OneNAND Memory Support

OMAP35xx ROM code was able to support 1 bit correctable error. AM/DM37xx ROM code is able to support up to 4 bits correctable error. It makes AM/DM37xx ready for upcoming generations of oneNAND memories.

5.5 New Boot Modes Supported

A new boot configuration (configuration #28) has been added on 37xx. This configuration was marked as reserved on OMAP35xx. This configuration is as follows:

- sys.boot[5] = 0
  - 1st: MMC2 (with VRMMC1 enabled on PMU)
  - 2nd: USB
  - 3rd: UART3
  - 4th: None
- sys.boot[5] = 1
  - 1st: USB

- 2nd: UART3
- 3rd: MMC2 (with VRMMC1 enabled on PMU)
- 4th: None

5.6 L2 Cache Disabled After PoR/Warm Reset

Information to be provided by engineer.

6 Module Revision Update

6.1 CortexA8

ARM Cortex-A8 r3p2 implements bug fixes that have been found in Cortex-A8 r2p3 and intermediate releases to r3p2. A new revision used in AM/DM37xx comes with additional L1 cache memories. Data and instruction caches have been extended from 16KB each to 32KB each. This update has an impact on cache management software.

6.2 SGX530

37xx implements 1.2.5 V of the SGX530TM core. This includes bug fixes associated with cache management.

7 Removed Features

7.1 8 Data Bits on MMC1

MMC1 interface supports MMC cards with up to 4 data bits.

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