Application Report

Charge-Sharing Driving Circuits for C2000 ADCs

ABSTRACT

Microcontrollers from the TMS320F2837xD, TMS320F2837xS, TMS320F2838x, TMS320F2807x, TMS320F28004x, and TMS320F28002x families feature high-speed multiplexed analog-to-digital converters (ADCs). These multiplexed data converters provide a good match for real-time control applications that need to sense many control signals with low latency. Under conditions where the sample rate on a given ADC channel is much slower than the total maximum ADC sample rate it may be possible to use a "charge-sharing" input design to drive the ADC input channel. This input design methodology can result in potentially lower cost, simplified circuit designs, and lower acquisition latency when compared to high-speed op-amp based input designs. This application report discusses the conditions where a charge-sharing signal conditioning circuit design is appropriate as well as present methods to evaluate the circuit's performance.

Project collateral and source code discussed in this application report can be downloaded from the following URL: http://www.ti.com/lit/zip/spracv0.

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1 Introduction

When driving an ADC input, achieving good settling performance is critical. Failing to achieve the necessary settling performance in the ADC driving circuits can result in distortion and memory cross-talk in the ADC conversion results. For an in depth discussion of the importance of minimizing errors associated with ADC input settling, see Appendix A. The signal conditioning circuits used to drive an ADC channel can vary widely in their requirements and implementation depending on the application requirements for that particular channel as well as the ADC input and sampling characteristics.

When sampling a high bandwidth signal near the maximum sample rate in a high-speed ADC, a very high performance driving circuit is required. This typically is comprised of a high-speed and low-noise op-amp stage that has passive component values optimized for minimal settling time (low resistor and capacitor values). These high performance drive stage circuits are suitable for driving most input signals, but require a high bandwidth op-amp which can have high component cost and may consume substantial printed circuit board area. Furthermore, if significant low-pass filtering is desired (many times desirable to limit noise in the conversion results), an additional active op-amp based filter stage may be necessary, adding cost and area.

Under certain circumstances, signals with sufficiently low sample rate can be directly interfaced to an ADC input channel by using a large "charge-sharing" capacitor placed on the ADC input. This method has the advantage of being simple, low-cost, and provides low-pass filtering. Furthermore, this can sometimes reduce sampling latency associated with the ADC acquisition. In particular, real-time control applications tend to use the ADC to scan through multiple multiplexed channels in a burst of conversions. These periodic bursts result in a sample rate on each channel that can be much less than the maximum sample rate of the ADC, which can sometimes achieve the necessary conditions for a charge-sharing input design.

This application report explains the mechanism that charge-sharing inputs use to achieve fast settling and will provide methods for designing a charge-sharing ADC driving circuit. Simulation methods will also be provided for verifying proper circuit settling behavior.

1.1 Resources

The following tools and materials are useful for ADC driver circuit design and evaluation for input settling.

1.1.1 TINA-TI SPICE-Based Analog Simulation Program

TI provides the TINA-TI application to TI customers to allow easy SPICE-based simulation of circuits utilizing TI products. This application report will utilize this program to evaluate circuit settling performance. Ensure this application is downloaded and installed before proceeding.

Link to Tool Folder: TINA-TI™

1.1.2 Application Report: ADC Input Circuit Evaluation for C2000 MCUs

This application report describes how to design and evaluate high-speed op-amp based ADC input driving circuits for C2000 MCU ADCs. Please review this application report before proceeding to understand high-speed op-amp based ADC input circuit design methods.

Link to application report: ADC Input Circuit Evaluation for C2000 MCUs

1.1.3 TI Precision Labs - SAR ADC Input Driver Design Series

TI precision labs has provided an excellent seven-part video series that demonstrates how to design the input drivers for a SAR ADC. Reviewing this material will help to further understand the high-speed op-amp based signal conditioning design process and options.

Link to Video Training Series: TI Precision Labs - SAR ADC Input Driver Design

1.1.4 Analog Engineer's Calculator

The analog engineer's calculator tool provides a variety of very useful GUI-based calculation tabs to assist with common analog circuit design tasks. The high-speed op-amp design methodology takes advantage of the Data Converters → ADC SAR Drive calculator.

Link to Tool Folder: Analog Engineer's Calculator

1.1.5 TI Precision Labs - Op Amps: Stability Series

TI precision labs has provided an excellent seven-part video series on op-amp stability. If charge-sharing input circuits do require an op-amp, the amplifier is usually exposed to a very large capacitive load. It is best practice to simulate to ensure that the source resistor is sufficiently large to ensure op-amp stability.

Link to Video Training Series: TI Precision Labs - Op amps: Stability.

2 Charge-Sharing Concept

The following sections describe the conceptual operation of charge-sharing input circuits.

2.1 Traditional High-Speed ADC Driving Circuits

In a traditional ADC input driving circuit as shown in Figure 2-1, the circuit is designed to generally minimize the overall circuit time constant (within some minor constraints), including the external source resistance (R_s) and external source capacitance (C_s). A high bandwidth op-amp is also generally needed to take advantage of this fast time constant. In the end, this circuit is capable of quickly settling the value on C_H during the allotted S+H window even when the ADC is sampling at high speed. The input signal being sampled can also have very high bandwidth.

For more information on design of op-amp based high-speed ADC signal conditioning circuits, see the TI precision labs video series: TI Precision Labs - SAR ADC Input Driver Design as well as the C2000 specific application report ADC Input Circuit Evaluation for C2000 MCUs.

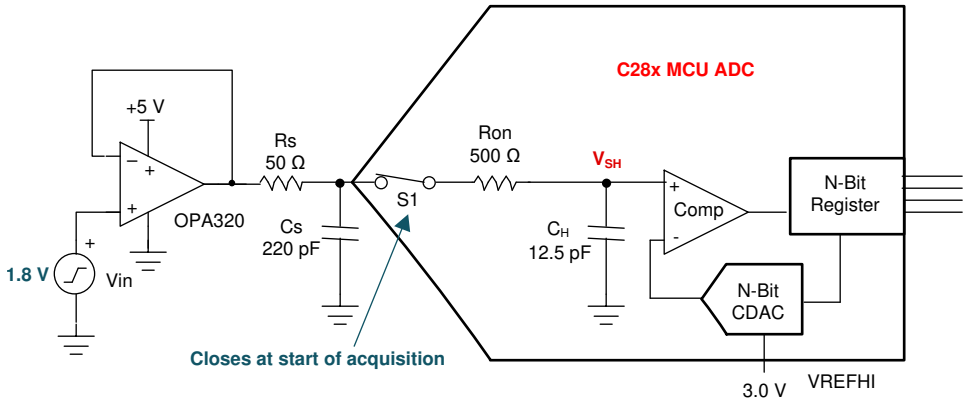

Figure 2-1. High Speed ADC Driving Circuit

2.2 Increased C_s in High-Speed ADC Driving Circuits

To implement a charge-sharing input design, C_s will be made very large. Care must be taken, however, because a large C_s is detremental in a typical high-speed ADC driving circuit. The need to keep R_s and C_s small in the high speed ADC driving circuit can be understood by looking at the equation for the approximate time constant and settling time given by the equations below.

An approximation of the required settling time can be determined using an RC settling model. The time constant for the model is given by the equation:

$$\tau = (Rs + Ron) \cdot Ch + Rs \cdot (Cs + Cp) \tag{1}$$

And the number of time constants needed is given by the equation:

$$k = ln\left(\frac{2^n}{settling\ error}\right) - ln\left(\frac{C_S + C_P}{CH}\right) \tag{2}$$

So the total S+H time should be set to approximately:

$$t = k \cdot \tau \tag{3}$$

Where the following parameters are provided by the ADC input model in the device data manual:

- n = ADC resolution (in bits)
- R_{ON} = ADC sampling switch resistance (in Ohms)
- C_H = ADC sampling capacitor (in pF)
- C_P = ADC channel parasitic input capacitance (in pF)

And the following parameters are dependent on the application design:

- settling error = tolerable settling error (in LSBs)
- R_s = ADC driving circuit source impedance (in Ohms)
- C_S = capacitance on ADC input pin (in pF)

From the above equations, it is clear that increasing R_s will result in strictly longer settling time because R_s is present in both terms of τ and has no effect on k. On the other hand, increasing C_S will increase τ but simultaneously reduce k due to increasing the ratio of C_s to C_H in the second term in k. However, increased C_s will result in longer settling time as the examples in Table 2-1demonstrate. This is because the time constant, τ, increases linearly while the number of time constants needed, k, decreases logarithmically. Therefore, high-speed ADC driving circuit designs generally keep the magnitude of C_s small (typically 20 times C_H) because increasing C_s results in additional settling time.

Table 2-1. Settling Time with Increasing C_s in High-Speed ADC Driver

Parameter	Example 1	Example 2	Example 3
C_S	220 pF	1 nF	2.2 nF
C_H	12.5 pF	12.5 pF	12.5 pF
C_p	10 pF	10 pF	10 pF
R_s	50	50	50
R_{ON}	425Ω	425Ω	425Ω
n	12 bits	12 bits	12 bits
settling error	0.5 LSBs	0.5 LSBs	0.5 LSBs
τ	17.4 ns	56.4 ns	116.4 ns
k	6.1	4.6	3.8
Settling time	106.1 ns	259.4 ns	442.3 ns

2.3 Very Large C_s in ADC Driving Circuits

While the previous section showed that increasing C_s results in increased settling time, there is one exception: if C_s is made sufficiently large that the second term of the equation for k (reproduced below) becomes equal to (or greater) than the first term, k will become zero (or negative) and thus the settling time, given by k·τ, will become zero (or negative) regardless of the size of τ. Because the predicted settling time is effectively zero, the minimum S+H duration specified in the ADC data manual can be used! When this condition is used in the design of the ADC driving circuit, the circuit is said to be using "charge-sharing".

$$k = ln\left(\frac{2^n}{settling\ error}\right) - ln\left(\frac{C_S + C_P}{CH}\right) \quad (4)$$

Table 2-2 shows an example of evaluating the equations under charge-sharing conditions.

Table 2-2. Settling Time Under Charge-Sharing Conditions

Parameter	Charge Sharing Example
C_S	102.4 nF
C_H	12.5 pF
C_p	10 pF
R_s	50
R_{ON}	425Ω
n	12 bits
settling error	0.5 LSBs
τ	5.1 µs
k	0.0
Settling time	0.0 ns

Conceptually, the second term in the equation for k is compensating for the driver not needing to fully charge both C_s and C_H. Instead, C_s is assumed to be pre-charged to the applied source voltage. This pre-charging occurs during the time when the ADC is converting and the S+H is inactive. When the S+H switch closes, the charge on C_s and C_H will equalize. At the same time, the source will exponentially settle both C_s and C_H towards the applied voltage. The large C_s is, the closer the voltage between C_s and C_H will be to the source voltage after equalization. In the charge-sharing case, C_s is made so large that equalization alone is sufficient to get C_H to within the settling error target.

CAUTION

For either high speed op-amp based design or charge-sharing based designs, sometimes simulation or analysis will predict that a S+H duration less than the minimum duration in the device data manual will allow for sufficient settling performance. Even in these cases, always select a S+H duration that meets the device data manual minimum specified S+H duration.

2.4 Charge-Sharing Operation

Figure 2-2 demonstrates a typical charge-sharing input circuit design as well as the conceptual settling operation sample-to-sample. C_s is set to a very large value. Specifically in this case, C_s is set to 100nF, which is roughly $2^{(12+1)}$ times as large as the internal ADC S+H capacitor, C_H. This will ensure that the drop in charge on C_s when sampling is only 0.5 LSBs at 12-bit ADC resolution.

The right sub-plot of Figure 2-2 shows the conceptual settling operation for this charge-sharing input design. At the beginning of each sample, the charge between C_s and C_H quickly equalizes, causing C_s to drop less than 0.5 LSBs and C_H to charge to within 0.5 LSBs of the applied voltage. This ensures that C_H reaches the settling target even when the S+H duration is very short. In the time between samples C_H is recharged from the source voltage through R_s. This example assumes the ADC is sampling slow enough that C_s can be almost completely recharge between samples. The next section will explore how feasible this assumption is.

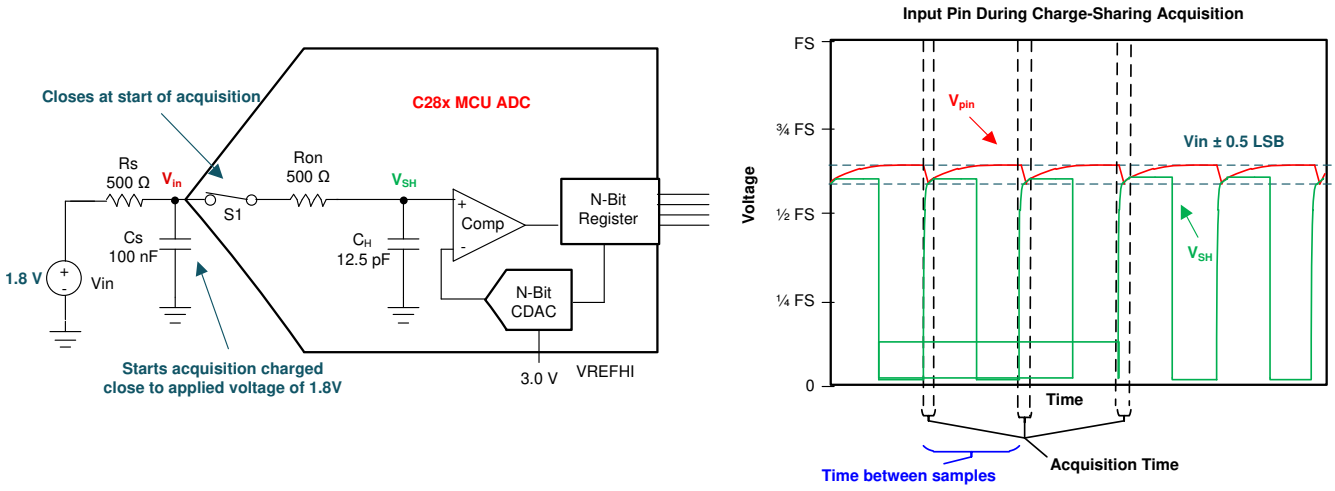

Figure 2-2. Charge-Sharing ADC Driving Circuit

Note

Figure 2-2 shows a 500Ω source resistance, R_s. While high speed op-amp based signal conditioning circuits usually determine and place this value intentionally, charge sharing designs are many times used to work around an existing source impedance without resorting to adding an additional op-amp to the design. This source resistance could be the output impedance of a sensor or the equivalent resistance of a voltage divider used to sense a high voltage bus. If the R_s is intentionally placed in a charge-sharing input circuit design, it is usually done so to form a low-pass filter with C_s..

2.5 Sample Rate and Source Impedance vs. Tracking Error

Designers of high speed op-amp based ADC signal conditioning circuits are required to trade-off settling speed against op-amp bandwidth and external component sizes. Meeting the charge-sharing criterion for source capacitor size ensures that the minimum ADC S+H window duration can be used regardless of source impedance. However, this creates a new trade-off that needs to be optimized: sample rate and source impedance vs. tracking error.

Significant tracking error occurs when the ADC samples too fast relative to the source's ability to recharge C_s through R_s in the time between samples. This is illustrated by simulating the circuit shown in Figure 2-3. The results from the this simulation can be seen in Figure 2-4: each step down in the sawtooth waveform is a charge equalization due to ADC sampling. In this situation, the first sample causes the voltage on the pin to drop by about 0.5 LSBs, resulting in a good sample of the DC input voltage. However, the external source is only able to partially able to recharge C_s before the next sample occurs. Each sample subsequently bleeds off some of the charge on C_s. Eventually, an equilibrium is reached when the delta between the pin voltage and the source voltage increases enough to drive 0.5 LSBs of recovery in the time between samples. In the simulation results of Figure 2-4, the equilibrium is reached at about 3.5mV of tracking error.

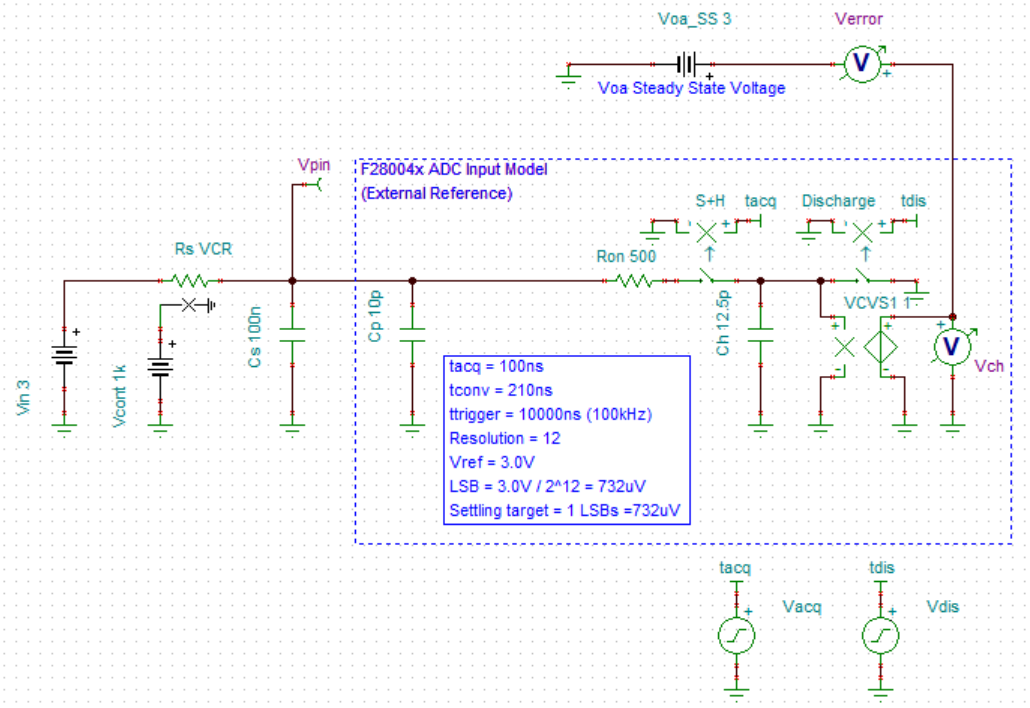

Figure 2-3. ADC Input Circuit With 1 kΩ R_s and 100 kHz Sample Rate

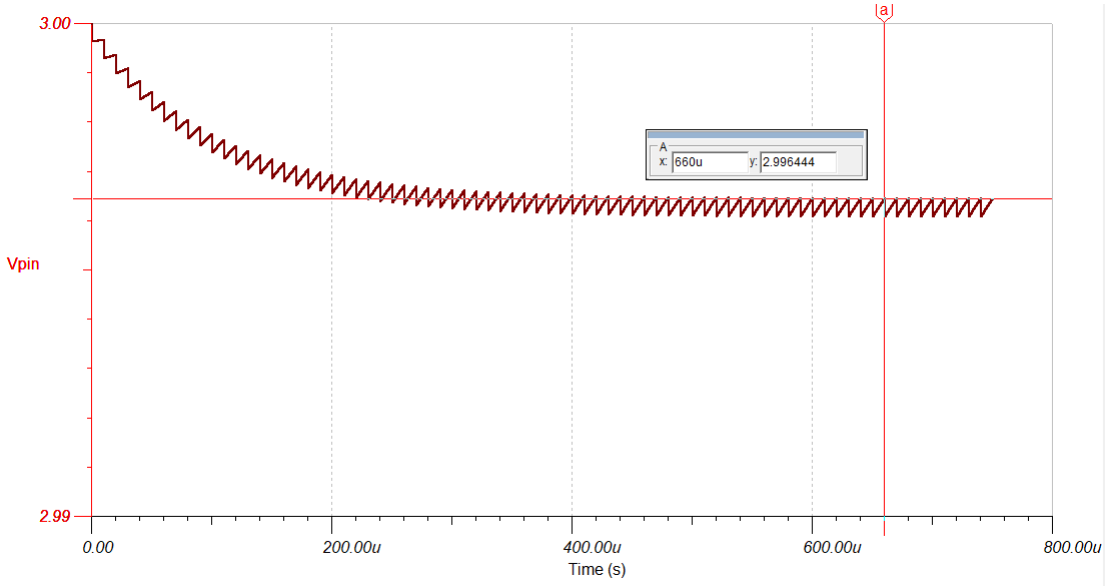

Figure 2-4. Simulation Results for 1kΩ R_s and 100 kHz Sample Rate

The settling error target is usually set to 0.5 LSBs, but applications may be able to tolerate more or less settling error. If a 1 LSB settling error target is assumed, the previous example circuit is still far out of target range with 0.5 LSBs of charge-share error plus 3.5mV of tracking error (about 5 LSBs). To get the tracking error within tolerance, either the sample rate needs to be reduced or the source impedance, R_s, needs to be reduced (or both).

Figure 2-5 and Figure 2-6 show that by significantly reducing the source impedance or the sample rate the tracking error can be made to be of a similar magnitude to the error from charge equalization, resulting in an overall settling error within the target of 1 LSBs.

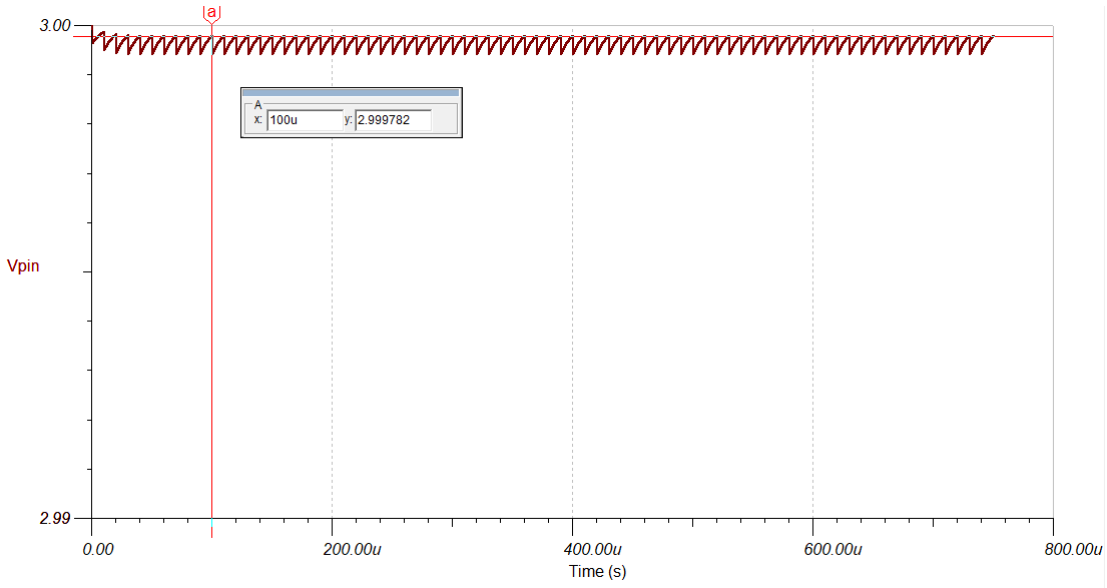

Figure 2-5. Simulation Results for 100Ω R_s and 100 kHz Sample Rate

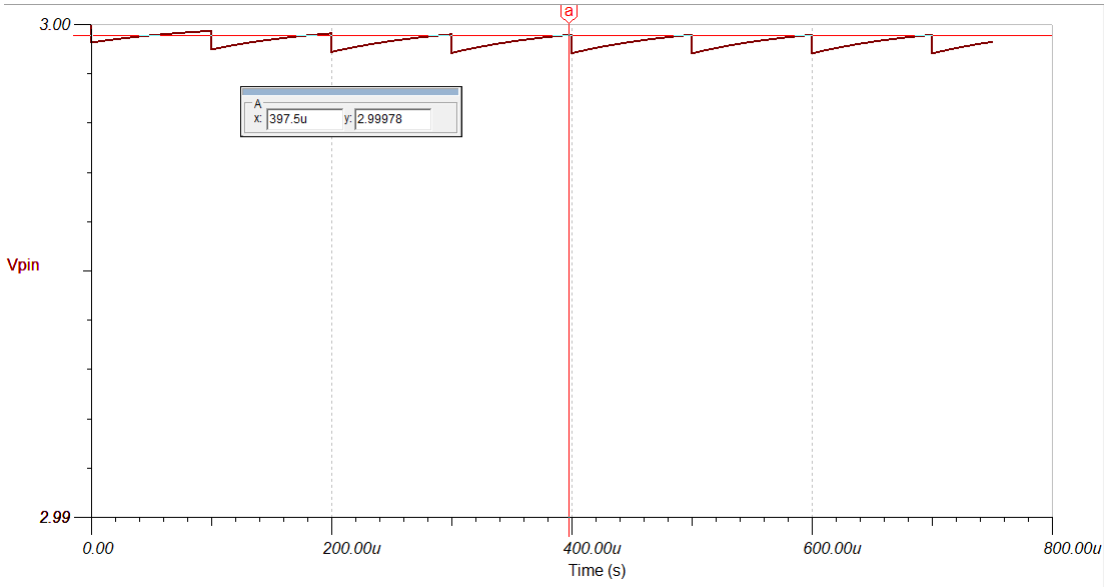

Figure 2-6. Simulation Results for 1kΩ R_s and 10kHz Sample Rate

Note

The example above shows a DC source voltage with a S+H capacitor that always starts fully discharged to 0 V. This makes the resulting tracking error look like a droop on the ADC input pin. In the case of an AC input signal the voltage on the pin will lag behind the applied voltage. In the case the S+H capacitor starts at a voltage other than 0 V (likely in multiplexed ADCs) the pin voltage will be pulled towards that other voltage (possibly the previously sampled channel in the mux sampling sequence).

2.6 Analytical Solution to Tracking Error

In a charge-sharing design, the total settling error is made up of two error components: the charge-sharing error and the tracking error. The charge-sharing error is determined by the relative sizes of the source capacitance, C_s, and the ADC's internal S+H capacitance, C_H. The tracking error is determined by the ability of the source to recharge C_s through the external source resistance, R_s, in the time between samples. Since the recharge primarily occurs while the ADC sampling switch is open, a first-order exponential RC settling model is appropriate where the RC time constant, τ, is determined by R_s and C_s.

To simplify analysis, it is assumed that the total settling error budget is equally divided between charge-sharing error and tracking error. In the case of a total settling error budget of 0.5 LSBs, the target for each of the sub-components would be 0.25 LSBs. Regardless of the absolute magnitude of the error components, allowing 50% recovery in the time between samples results in equal error component magnitudes (equivalent to approximately 0.7 RC time constants). The equal error magnitudes in equilibrium are illustrated in Figure 2-7. At the beginning of each sample, charge equalizes between C_S and C_H, resulting in a 0.25 LSBs drop in voltage. Then, in the time until the next conversion, the pin voltage charges exponentially back towards the applied DC voltage. Recovering from 0.5 LSBs to 0.25 LSBs requires 50% settling.

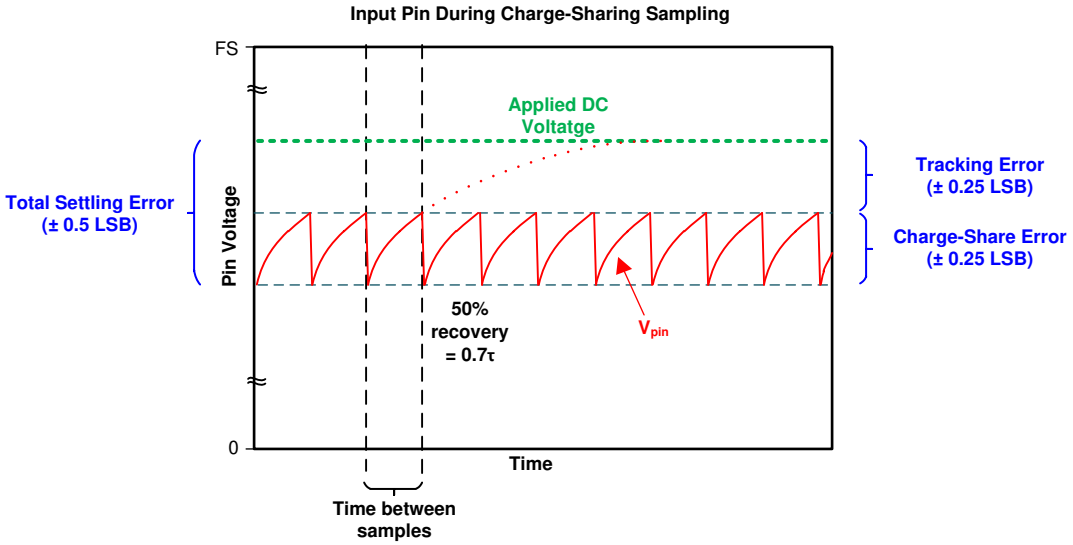

Figure 2-7. Charge Sharing Steady State With DC Input

Since the criteria for equal error components requires 0.7 time constants, the following equation determines the approximate maximum sample rate given a fixed source impedance:

$$f_s \leq 1 / (0.7 \cdot R_S C_S) \quad (5)$$

Alternately, if a specific sample rate is required, the above equation can be rearranged to give the maximum source impedance for a known sample rate:

$$R_s \leq 1 / (0.7 \cdot f_S C_S) \quad (6)$$

For example, consider a circuit with 12.5pF CH, target sample rate of 10ksps, and settling error target of 0.5 LSBs at 12-bit resolution. To get charge sharing error of 0.25 LSBs, Cs will be set to approximately 12.5pF·(4096/0.25) = 204.8nF. This will then yield a maximum source impedance of:

$$R_s \leq 1 / (0.7 \cdot 10\text{kHz} \cdot 204.8\text{nF}) \quad (7)$$

$$R_s \leq 698\ \Omega \quad (8)$$

Note

In the case that the maximum sample rate does not meet the application requirements, an op-amp can be added to isolate the existing source resistance from the circuit. R_s should then be selected to be large enough to ensure the op-amp is stable when driving C_s. This op-amp should also have a bandwidth of at least 4 times that of the RC time constant formed from R_s and C_s.

2.7 Charge-Sharing in Multiplexed ADCs

Multiplexed ADCs connect many analog input channels to a single ADC. The ADC can then scan through the multiple input channels either continuously or in bursts based on an external trigger (many times an ePWM trigger in C2000 applications).

For the sake of charge-sharing, the sample rate on a given channel is important, not the full sample rate of the ADC. This is because charge-sharing equalization will only occur when the particular multiplexed channel is sampled and the source capacitance will have the entire time between sampling to recharge, even if other channels are sampled in the meantime. In applications where the ePWM is triggering the ADC periodically, the sample rate on a given multiplexed channel will match the ePWM triggering frequency.

2.8 Charge-Sharing Circuit Advantages

The previous sections describe how a charge sharing circuit can be constructed as an alternate to high-speed op-amp based ADC driving circuits. This can be done for a variety of reasons:

- **Low Latency**

  A charge-sharing design can always use the minimum S+H time. If the application goal is to reduce the latency between ADC trigger and ADC sample complete, using a shorter S+H time can be advantageous. Achieving equivalent settling time with a high-speed op-amp based design may require extremely high op-amp bandwidth.
- **Low Cost**

  Charge-sharing designs can sometimes entirely eliminate an op-amp channel from the design. If the channel sample rate is slow enough, a charge-sharing design can be used to directly interface to sensors with large output impedance. This also includes directly interfacing to a voltage divider, which will have a large equivalent output impedance in order to minimize static current draw.
- **Low-Pass Filtering**

  High-speed op-amp designs generally can not provide significant low-pass filtering (including anti-aliasing filtering) in the drive stage due to the need to keep the R and C component values very low to ensure fast settling. In these designs if significant low-pass filtering is needed, a separate filter stage is built before the ADC drive stage. In contrast, charge-sharing input designs can many times also provide significant low-pass filtering due to the large source capacitor size needed to meet the charge-sharing criterion.

2.9 Charge-Sharing Circuit Disadvantages

Charge-sharing ADC input designs are not appropriate for all signal conditioning requirements. Care should be taken to select a high-speed op-amp based design when it is more appropriate, including:

- **High Speed Sampling**

  When sampling at high speed on a single channel, the tracking error in a charge-sharing design will become prohibitively large. In this case, a high-speed op-amp based ADC driver will be needed.
- **Compatibility with Oversampling Methods**

  Sampling the same signal multiple times back-to-back and then averaging the results can be a good method to reduce system noise or sampling noise. However, in the case of a charge-sharing ADC driver, these multiple samples will increase the effective sample rate on the channel, increasing the tracking error. In the case the extra samples are back-to-back, the channel sample rate becomes as fast as the ADC sample rate, which will likely create excessive tracking error.
- **High Bandwidth Signals**

  The large capacitor needed to meet the charge-sharing criterion will inherently provide some amount of low-pass filtering. For undersampling applications or other applications that require sampling of a high bandwidth signal, charge sharing may not be feasible.

- **Extremely Low Distortion**

  C0G and NP0 type capacitors provide very low capacitance vs. voltage nonlinearity. If the ADC signal chain uses these capacitors it is possible to achieve excellent distortion performance. These capacitors are less dense than higher distortion alternatives (for example X7R type). This can make component selection for the very large capacitances needed for charge-sharing designs infeasible, particularly at high resolution (for example 16-bit resolution). See Selecting capacitors to minimize distortion in audio applications.

3 Charge Sharing Design Flow

The following sections walk through the steps necessary to design a charge-sharing ADC input driver. A worksheet is provided in Section 3 for convenience.

1. Gather circuit information and requirements
2. Size C_s
3. Verify sample rate, source impedance, and bandwidth
4. Simulate Circuit Settling Performance

3.1 Gather Required Information

The following information will be needed to proceed with designing and verifying the charge sharing input circuit. As these values are gathered, they can be filled into the worksheet provided in Section 3.5.

- **N**: Target settling resolution (bits). Usually the same as the resolution of the ADC. Lower resolution can be targeted to relax the input design requirements.
- **V_{fs}**: Full scale voltage range. In external reference mode, this is the voltage supplied to the VREFHI pin (usually 3.0 V or 2.5 V).
  In internal reference mode, this is the effective input range based on the selected reference mode (usually 3.3 V or 2.5 V).
- **C_H**: ADC S+H capacitance. Provided in the data manual table "Input Model Parameters".
- **C_p**: ADC pin parasitic capacitance. Provided in the data manual table "Per-Channel Parasitic Capacitance".
- **R_s**: Source Resistance. Output resistance of source driving ADC. Can also be intentionally selected.
- **F_s**: Sample rate on channel of interest. Usually a requirement from the application.
- **BW_s**: Source signal required bandwidth.

3.2 Size C_s

C_s should be sized such that the charge-share error is 0.25 LSBs. The design process will ensure that the tracking error is also within 0.25 LSBs, resulting in a total settling error within 0.5 LSBs. To achieve this, select Cs to be at least as large as the below equation indicates. It will then be necessary to round the results to a standard capacitor component size.

$$C_s = (2^{N+2} \cdot C_H) - C_p \tag{9}$$

In many designs, the size of C_p compared to the size of the selected C_s will be negligible and thus C_p can be ignored.

3.3 Verify Sample Rate, Source Impedance, and Bandwidth

Once the source capacitor has been sized, several items can be validated in the design. These include:

- **Maximum Sample Rate**

  If the source resistance is known the maximum sampling rate that can be supported without exceeding the tracking error budget can be calculated using the equation below.

$$f_{smax} = 1 / (0.7 \cdot R_s \cdot C_s) \tag{10}$$

  The application required sample rate (on the channel under consideration) f_s should be less than f_{smax}.

- **Maximum Source Resistance**

  Alternately, if the application sample rate is fixed, the maximum source impedance that will result in tracking error within the error budget can be calculated using this equation.

  $$R_{smax} = 1 / (0.7 \cdot f_s \cdot C_s) \quad (11)$$

  This can then be checked against the source impedance of one or more input channels that are utilizing a charge-sharing input design to ensure that $R_s < R_{smax}$.
- **Bandwidth**

  The filter bandwidth of the low-pass filter formed from C_s and R_s can be calculated using the following formula.

  $$BW_{RsCs} = 1 / (2\pi \cdot C_S \cdot R_S) \quad (12)$$

  Ensure that the source signal bandwidth, BW_s, is greater than the low-pass filter bandwidth from this step. If the filter bandwidth is too low, frequencies of interest of the input signal will be attenuated.

3.4 Simulate Circuit Settling Performance

The formulas above will target N + 1 bit settling performance which can further be divider into N + 2 bits of charge-share error and N + 2 bits of tracking error. In order to compare these targets to simulation results in volts, the absolute settling error target can be calculated as:

$$V_{errmax} = V_{fs} / 2^{N+1} \quad (13)$$

The settling simulation can then be run to verify that the measured settling error is within this error budget.

For specifics on how to perform the settling simulation with a charge-sharing circuit, see Section 4.

3.5 Input Design Worksheet

Table 3-1 shows a blank worksheet for a charge sharing input design.

Table 3-1. ADC Charge Sharing Design Worksheet

Symbol	Description	Value	Comments
N	Target settling resolution (bits)		Usually the same as the resolution of the ADC. Lower resolution can be targeted to relax the input design requirements
V_{fs}	Full scale voltage range		In external reference mode, this is the voltage supplied to the VREFHI pin (usually 3.0 V or 2.5 V) In internal reference mode, this is the effective input range based on the selected reference mode (usually 3.3 V or 2.5 V)
V_{errmax}	Maximum error target		V_{fs} / 2^{N+1} Can be further divided into two components: charge-sharing error and tracking error, each V_{errmax} / 2
t_{sh}	S+H time		As long as C_s is sized appropriately for charge-sharing, the minimum value from the ADC data manual can be used.
C_h	ADC S+H capacitance		Provided in the data manual table "Input Model Parameters"
C_p	ADC pin parasitic capacitance		Provided in the data manual table "Per-Channel Parasitic Capacitance"
C_s	Source capacitance		At least ($2^{N+2} \cdot C_H$) - C_p
R_s	Source resistance		Output resistance of source driving ADC. Can also be intentionally selected.
f_s	Sample Rate		Sample rate on channel of interest. Usually a requirement from the application.
BW_s	Source signal required bandwidth.		Source signal required bandwidth.
R_{smax}	Max allowable source resistance		If f_s is known, calculate as 1 / ($0.7 \cdot f_s \cdot C_s$) , then ensure that $R_s < R_{smax}$. If the condition is not met, additional design iteration is needed.
f_{smax}	Max allowable sampling frequency		If R_s is known, calculate as 1 / ($0.7 \cdot R_s \cdot C_s$, then ensure that $f_s < f_{smax}$. If the condition is not met, additional design iteration is needed.
BW_{RsCs}	Filter bandwidth from C_s and Rs		1 / (2 π C_s R_s) Ensure that $BW_{RsCs} > BW_s$, otherwise additional design iteration is needed.
V_{oa_ss}	Steady state op-amp output voltage		If no op-amp is used, set $V_{oa\_ss} = V_{fs}$. Otherwise, this can be generated from DC nodal analysis of the V_{oa} node. Copy to Voa_ss before proceeding with other simulations.
BWOPA	ADC driver op-amp minimum bandwidth		If an op-amp is needed, bandwidth should be at least 4 times BW_{RsCs}
Op-amp	Selected Op-amp part number		Record selected op-amp here (if needed).
V_{err}	Actual settling error from simulation		Ensure $V_{err} < V_{errmax}$ Otherwise, additional design iteration is needed

4 Charge-Sharing Circuit Simulation Methods

The following sections describe how to perform simulations to determine the settling error from a charge-sharing ADC driving circuit. TINA-TI models for many C2000 devices are provided with this application report here: http://www.ti.com/lit/zip/spracv0. More detail on building a TINA-TI based ADC input model can be found in TI Precision Labs - SAR ADC Input Driver Design. More detail on building a C2000-specific TINA-TI model can be found in ADC Input Circuit Evaluation for C2000 MCUs.

4.1 Simulation Components

Figure 4-1 and Figure 4-2 show the components in the TINA-TI simulation setup.

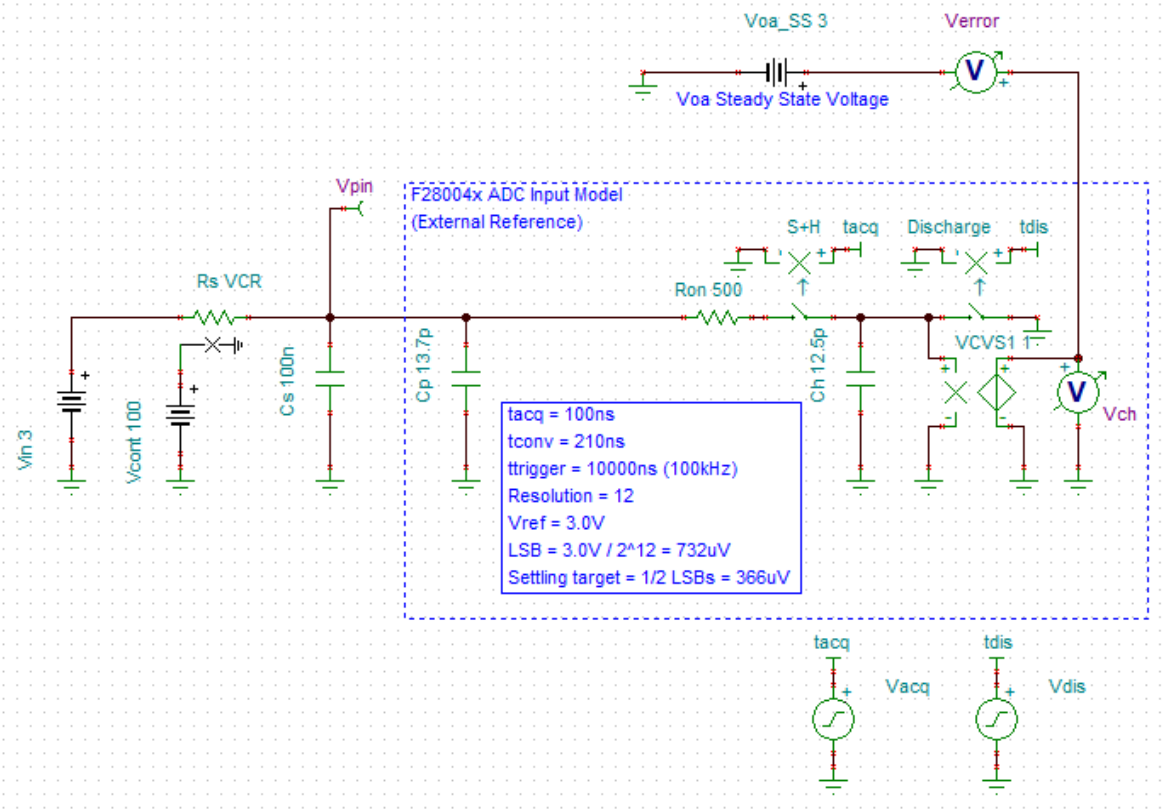

Figure 4-1. Simulation Schematic (No Op-Amp)

4.1.1 V_{in}

V_{in} is the applied voltage. The S+H capacitor (C_H) will need to be charged to within the settling error tolerance by the end of the S+H period. While any input can be simulated, applying a full-scale DC input voltage while the model fully discharges C_H between every sample will provide worst-case settling conditions.

4.1.2 V_{oa} , V_{oa_SS}, and V_{error}

TINA-TI op-amp models incorporate various non-idealities, which results in the DC steady state output of the op-amp at V_{oa} not exactly matching V_{in}. The steady state output at V_{oa} can be simulated and entered into V_{oa_ss} such that V_{error} is an accurate representation of only the input settling error. In the case that no op-amp is used in the charge-sharing input design, V_{oa_SS} should be set to exactly V_{in}.

4.1.3 R_s, C_s, and V_{cont}

R_s and C_s are the source resistance and source capacitance. These values correspond to R_s resistance is controlled by the control voltage V_{cont}. R_s is a voltage-controlled resistor with gain of 1 (1 V = 1 Ω, 10 V = 10 Ω, and so forth) instead of a simple resistor to allow parameter sweeping when there are two R_s resistors in the differential models.

4.1.4 C_h, R_{on}, and C_p

Component values for the ADC input model.

C_h, the S+H capacitor. The goal of the simulation is to charge this capacitor to as close as possible to V_{in} during the S+H window.

C_p is the pin-specific input capacitance. Can be optionally added to the simulation to improve simulation accuracy. This is particularly helpful for pins that are multiplexed with VDAC (alternate DAC voltage reference pin) that have a value of C_p, which is greater than 100 pF on most devices.

Pins that are multiplexed with the buffered DAC output on F2837x and F2807x devices have a parasitic 50k Ω pull-down resistor present on these pins. It is recommended to add this resistor to the model (not shown in Figure 4-1 or Figure 4-2) to better represent behavior of these pins.

4.1.5 S+H Switch, Discharge Switch, t_{acq}, and t_{dis}

Switch "S+H" controls when the S+H capacitor, C_h, is being charged by the driving circuit. The timings for this switch are controlled by t_{acq}.

Switch "Discharge" controls when the S+H capacitor, C_h, is being reset by being discharged to ground. The timings for this switch are controlled by t_{dis}.

When neither t_{acq} or t_{dis} are active, the value of the S+H capacitor is held at its final settled values.

Additional information on how to configure these switches based on the desired charge-sharing simulation parameters can be found in Section 4.2.

CAUTION

While the ADC input models for multiple C2000 devices are bundled with this application report, input model component values should always first be verified with the device-specific data manual before proceeding. Values for C_h and R_{on}can be obtained from the *Input Model Parameters* table in the device-specific data manual while values for C_p can be obtained from the *Per-Channel Parasitic Capacitance* table. In any cases where the device-specific data manual values disagree with the values in this document or in the provided models, the device-specific data manual values should always be considered the correct values.

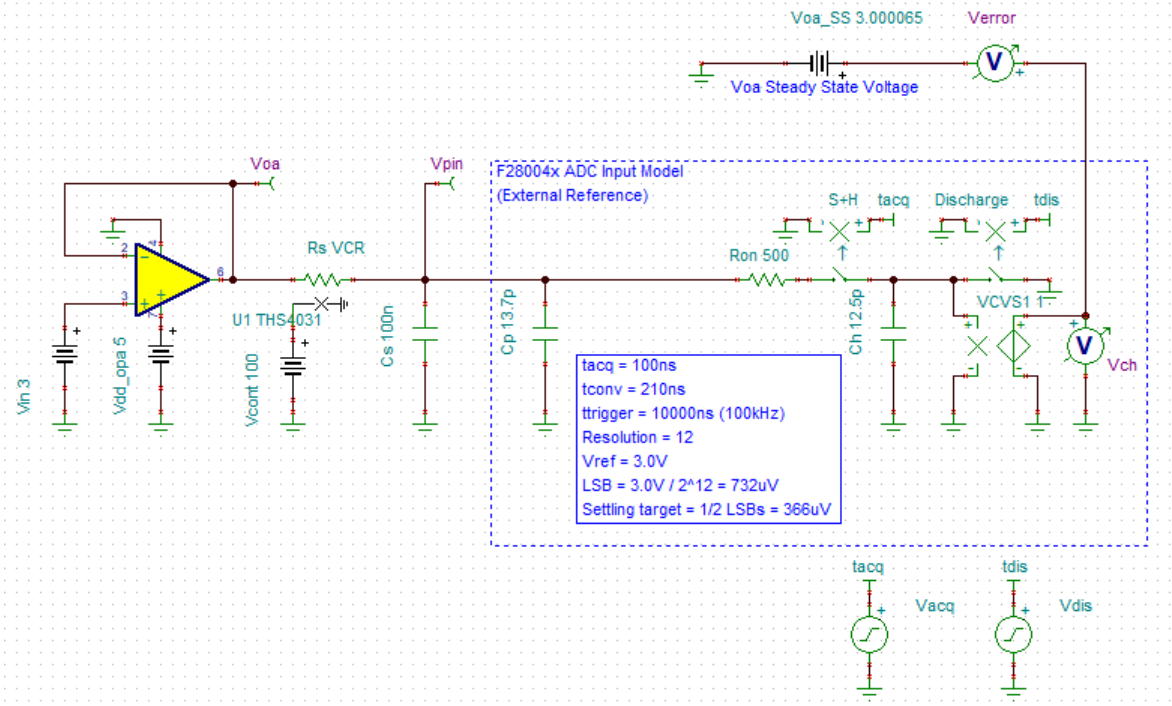

Figure 4-2. Simulation Schematic

4.2 Configure the Simulation Parameters

The primary configuration that needs to be done for charge-sharing simulations is to set the sample rate. This is controlled by settings of the piecewise linear voltage sources t_{acq} and t_{dis}.

Sample t_{acq} timing configurations for a 100 ns acquisition window and 100kHz sampling are shown in Figure 4-3. The first four lines configure the S+H window to occur from 0 to 102 ns with 1 ns rise and fall times. The last line (which is of primary interest) configures how often the waveform repeats. This effectively sets the sample rate, so 10000 ns (10 µs) is equivalent to 100 kHz sampling.

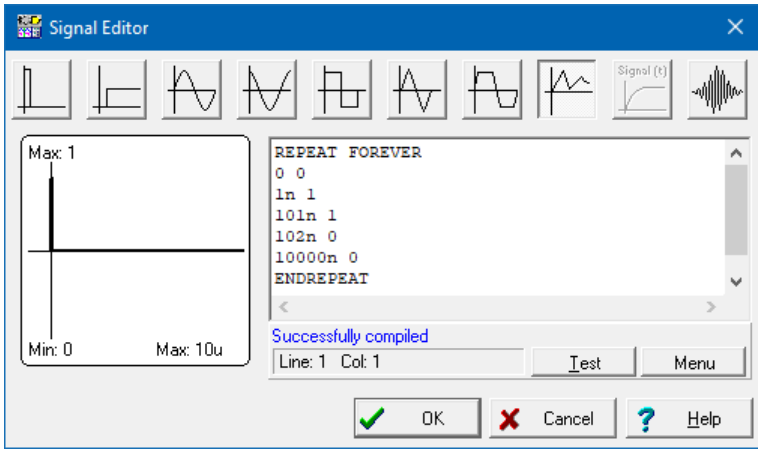

Figure 4-3. Example Timings for t_{acq} (Piecewise Linear)

Sample t_{dis} timing configurations for a 100 ns discharge period and 100 kHz sampling are shown in Figure 4-4. The first five lines specify a 100 ns discharge period with 10ns rise and fall times starting at 9.87 µs. The last line configures how often the waveform repeats. This effectively sets the sample rate, so 10000 ns (10 µs) is equivalent to 100 kHz sampling. Ensure that the last line of the tdis and t_{acq} timings always exactly match! It is not necessary for this discharge period to occur exactly at the end of the triggering period, so it is acceptable to change the sampling rate by only changing the last line. For example, changing the final line of both t_{dis} and t_{acq} to 20000 ns will change the sample rate to 50 kHz. Do, however, ensure that the discharge period does not overlap with the S+H period in t_{acq} as this will result in the input being shorted to ground instead of charging C_H.

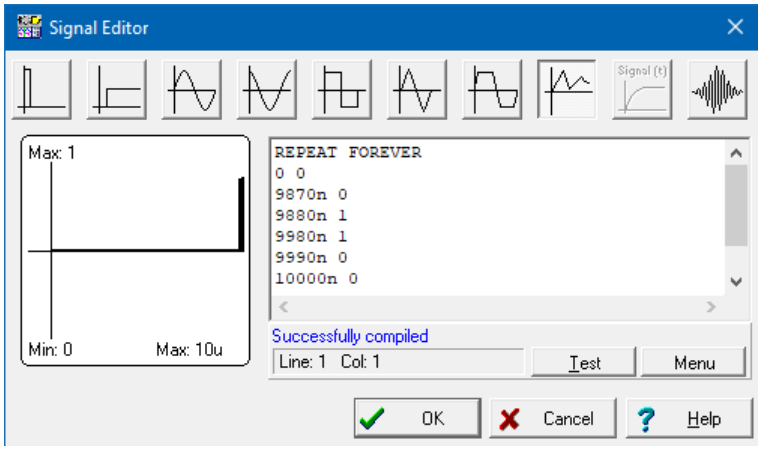

Figure 4-4. Example Timings for t_{dis} (Piecewise Linear)

Note that the timings are configured to emulate conversions triggered at 100 kHz frequency. This slower sample rate on a specific channel is typical of a charge-sharing input design (instead of back-to-back continuous conversions at the max ADC sample rate). The triggering rate can be modified to match the actual application ePWM trigger rate by modifying the period of the t_{acq} and t_{dis} timing sources. Do, however, ensure that the trigger rate is slower than the total S+H plus acquisition time for the ADC conversion. The ADC conversion time can be found in the device-specific data manual table "ADC Timings".

CAUTION

The first time a settling simulation is run, the TINA-TI simulation parameters also need to be configured for maximum accuracy. This procedure can be seen in the Building the SAR ADC Input Model video from TI precision labs in the "Optimizing Simulation Results" section.

4.3 Simulating Op-amp Steady-State Voltage

Charge-sharing settling input designs do not always include an op-amp, but when the signal chain of interest does, steps must be taken to account for the DC voltage errors modeled in the TINA-TI models. This ensures that the simulation only measures settling performance.

To accomplish this, run a DC nodal analysis by using the menu options "Analysis" → "DC Analysis" → "Calculate nodal voltages". Then copy the voltage produced at the op-amp output node to the V_{oa_SS} voltage source as shown in Figure 4-5.

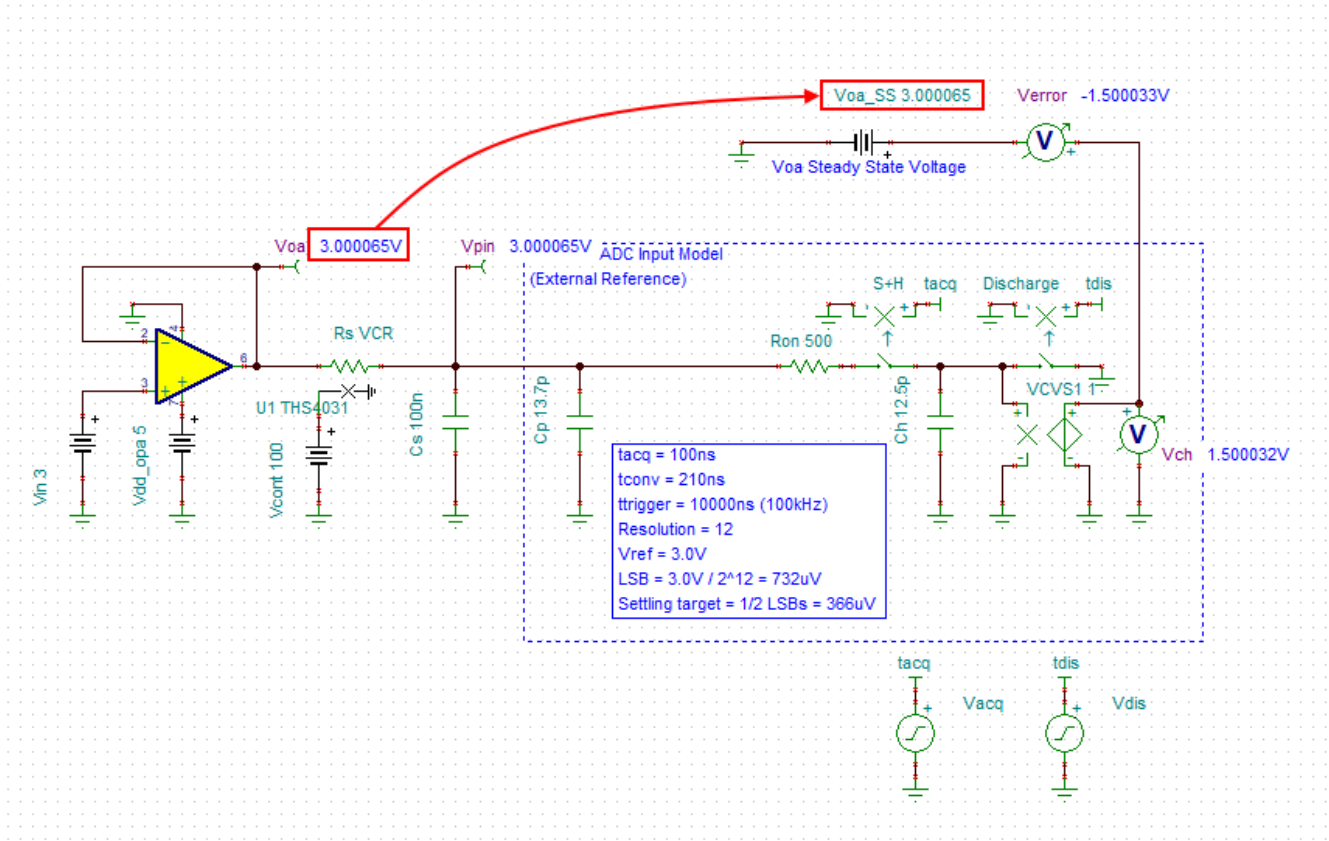

Figure 4-5. Nodal Analysis Example

This same method can be used to determine the expected output voltage of a voltage divider. Apply a DC input voltage to the divider and copy the nodal output voltage to V_{oa_ss}.

4.4 Measure the Settling Error

Once the circuit is built in TINA-TI, the steady-state voltage is measured (if applicable), and the sample rate is configured, measuring the settling error is relatively straightforward. This can be accomplished by running a transient analysis over enough periods to ensure that the system reaches steady state.

To run the transient analysis, use the TINA-TI commands "Analysis"→ "Transient..." then enter a simulation time period and select "OK". A good starting point is about 30 sampling periods.

Figure 4-6 shows the results of this transient simulation applied to the example circuit in Figure 4-5 which has 100 nF C_s, 100Ω R_s , and a 100 kHz sampling rate. After simulation, signals were split into separate traces using the "View" → "Separate Curves" menu option. All traces other than V_{error} and V_{pin} were then deleted by selecting the curves and hitting the delete key.

To measure the total settling error, place a cursor at any point other than the S+H window on the V_{error} trace. This simulation shows about 589 µV of settling error from this method (cursor B). Alternately, the minimum value of V_{pin} can also be measured. This method shows approximately 3 V - 2.99942 V = 580 µV of settling error (cursor A).

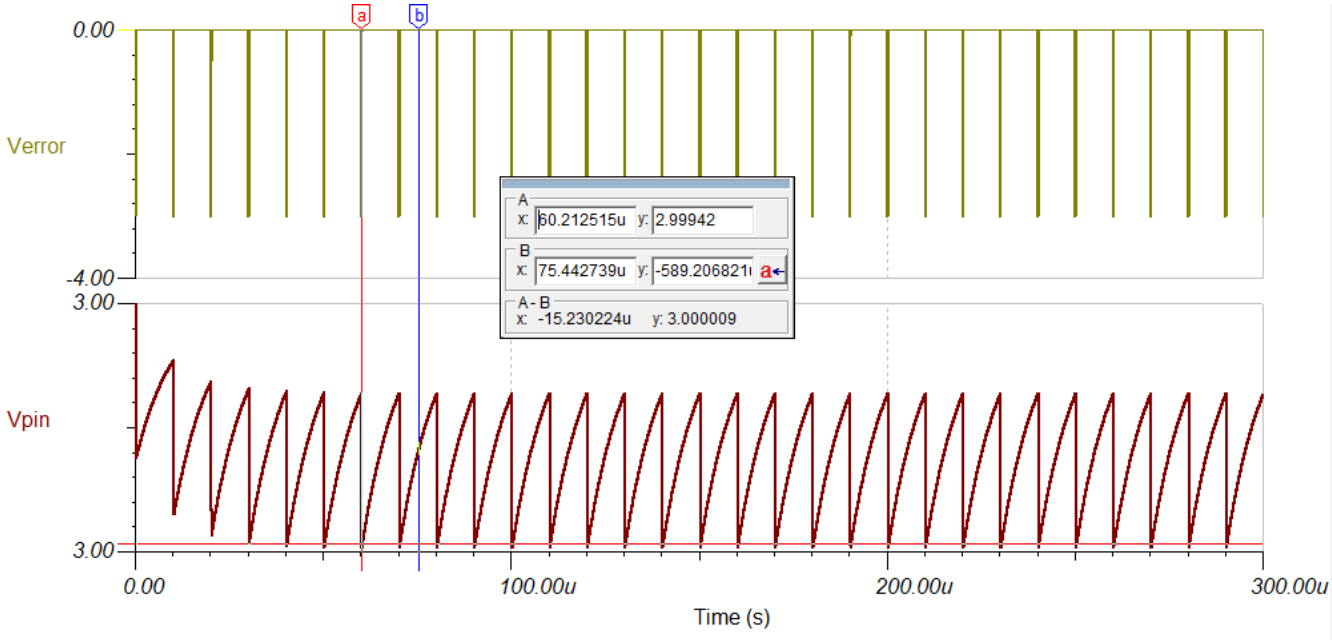

Figure 4-6. Settling Error Measurement

In addition, it is possible to separately measure the charge-share and tracking errors. Figure 4-7 shows the results of narrowing the simulation to 20 periods and also deleting the V_{error} trace. The distance from 3 V to max value of V_{pin} in steady state is the approximate tracking error. In this case, the tracking error is 3 V - 2.999781 V = 219 µV (cursor A). Similarly, the charge-share error is the difference between the tracking error point and the minimum pin voltage in the steady state. In this case, the charge-share error is 2.99781 V - 2.999418 V = 363 µV (cursor A minus cursor A).

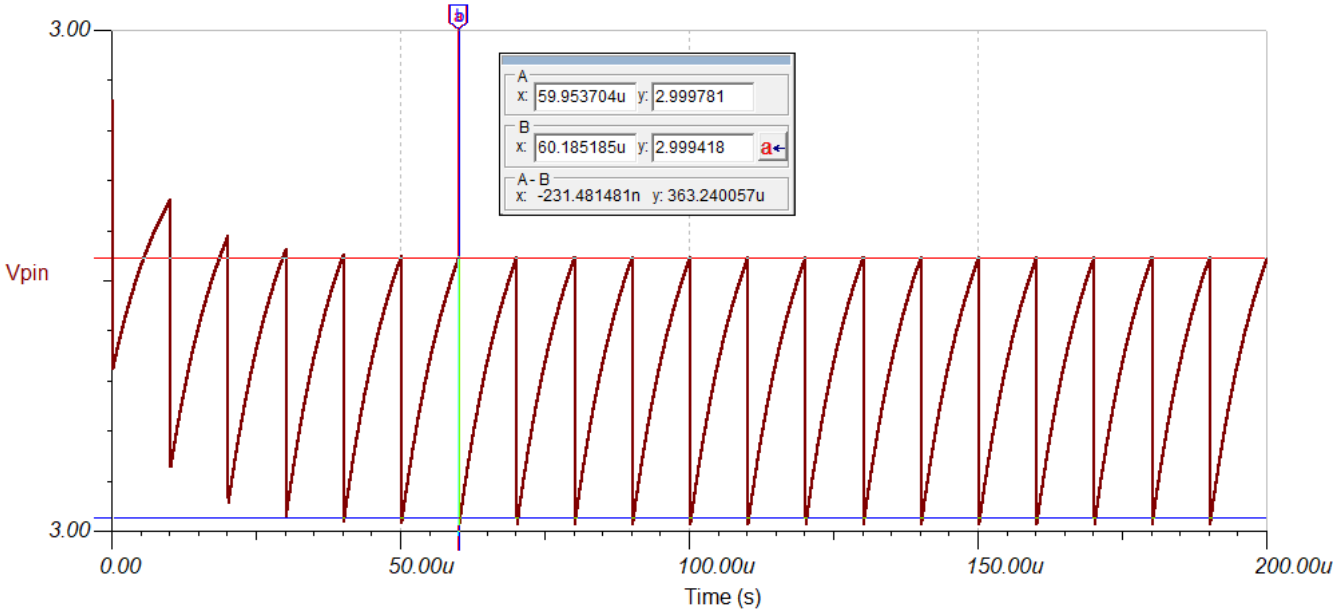

Figure 4-7. Settling Error Component Measurement

4.5 Sweeping Source Resistance

It may sometimes be helpful to run simulations for a range of R_s values. To accomplish this, select the TINA-TI menu options "Analysis" → "Set Control Object" and then click on V_{cont} voltage source (which controls the source resistance, R_s). The sweep of the component can then be configured as shown in Figure 4-8.

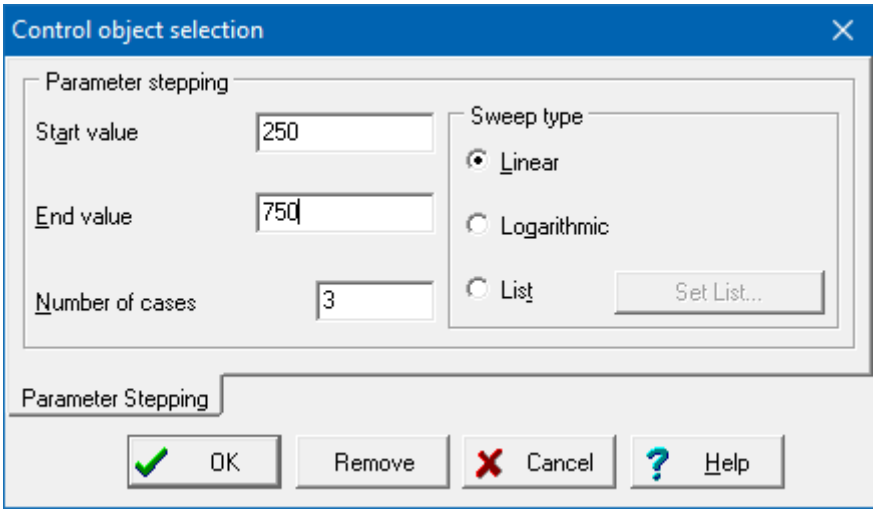

Figure 4-8. Sweep Configuration Dialog

Once the component sweep is configured, the transient analysis can be run as usual and then separate the outputs using the "View" → "Separate Outputs" menu command. The simulation will now produce one output curve for each resistance value in the sweep. Figure 4-9 shows the results of simulating 100kHz sampling with 250Ω, 500Ω, and 750Ω source resistance values. It is recommended to view the results of all output curves simultaneously by placing the cursor, then creating a legend as shown in Figure 4-9.

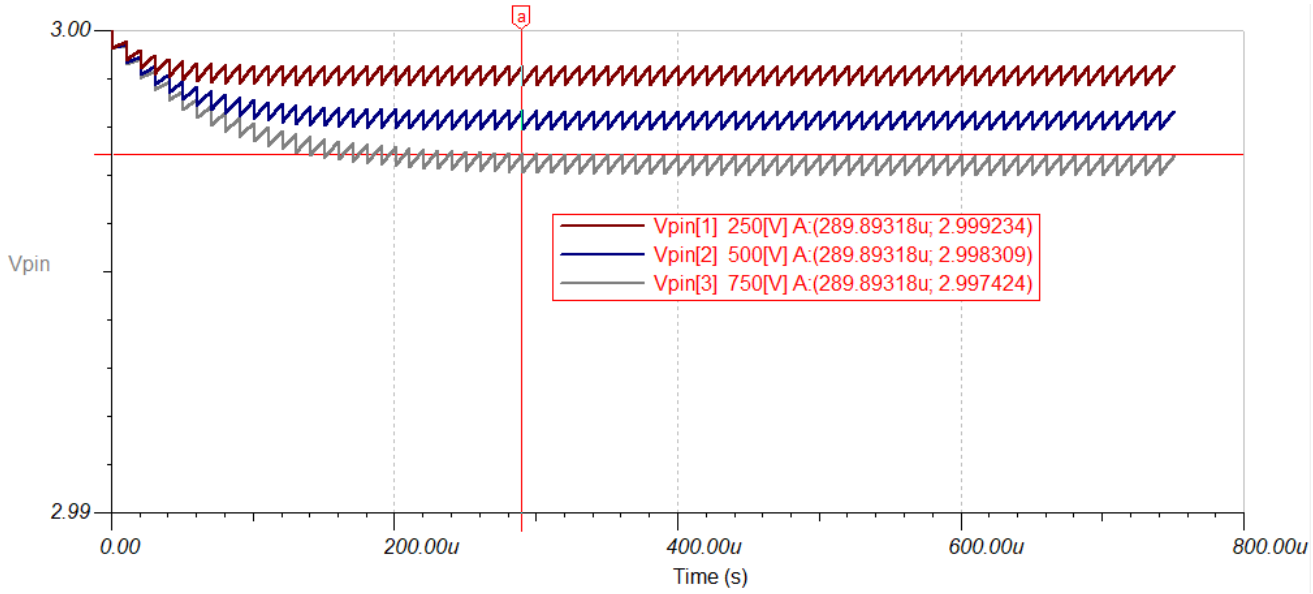

Figure 4-9. Source Impedance Sweep Results

5 Example Circuit Designs

The following sections apply the analysis and simulation methods to a series of examples.

5.1 Example 1: Determining Maximum Sample Rate

In this example a sensor with known output impedance of 500Ω is to be connected to the 12-bit ADC of an F28004x device without an op-amp (if possible). The ADC is operating with a 3.0V external reference. Analysis and simulation will be used to determine the maximum rate the sensor should be sampled at. Full settling performance of 12+1 bits is desired and the signal bandwidth is low (assume 500Hz).

5.1.1 Example 1: Analysis

The C_H value of the F28004x ADC is determined to be 12.5pF from the device data manual. C_p is assumed to be negligible. C_s is therefore sized accordingly:

$C_s = (2^{N+2} \cdot C_H) - C_p = (2^{12+2} \cdot 12.5pF) - 0pF = 205nF$

Which is then rounded up to C_s = 220nF. The maximum sample rate is then calculated using the equation:

$f_{smax} = 1 / (0.7 \cdot R_s \cdot C_s) = 1 / (0.7 \cdot 500\Omega \cdot 220nF) = 13kHz$

Finally, the external low-pass filter bandwidth is:

$BW_{RsCs} = 1 / (2\pi \cdot C_s \cdot R_s) = 1/ (2\pi \cdot 220nF \cdot 500\Omega) = 1.4kHz$

5.1.2 Example 1: Simulation

The circuit to simulate is shown in Figure 5-1. No steady state analysis is needed because there is no op-amp. A transient analysis is done over 2.5 ms as shown in Figure 5-2, resulting in a measured total settling time measurement of 3 V - 2.999662 = 338 µV, which is under the target settling error of 3 V / 2^{12+1} = 366 µV.

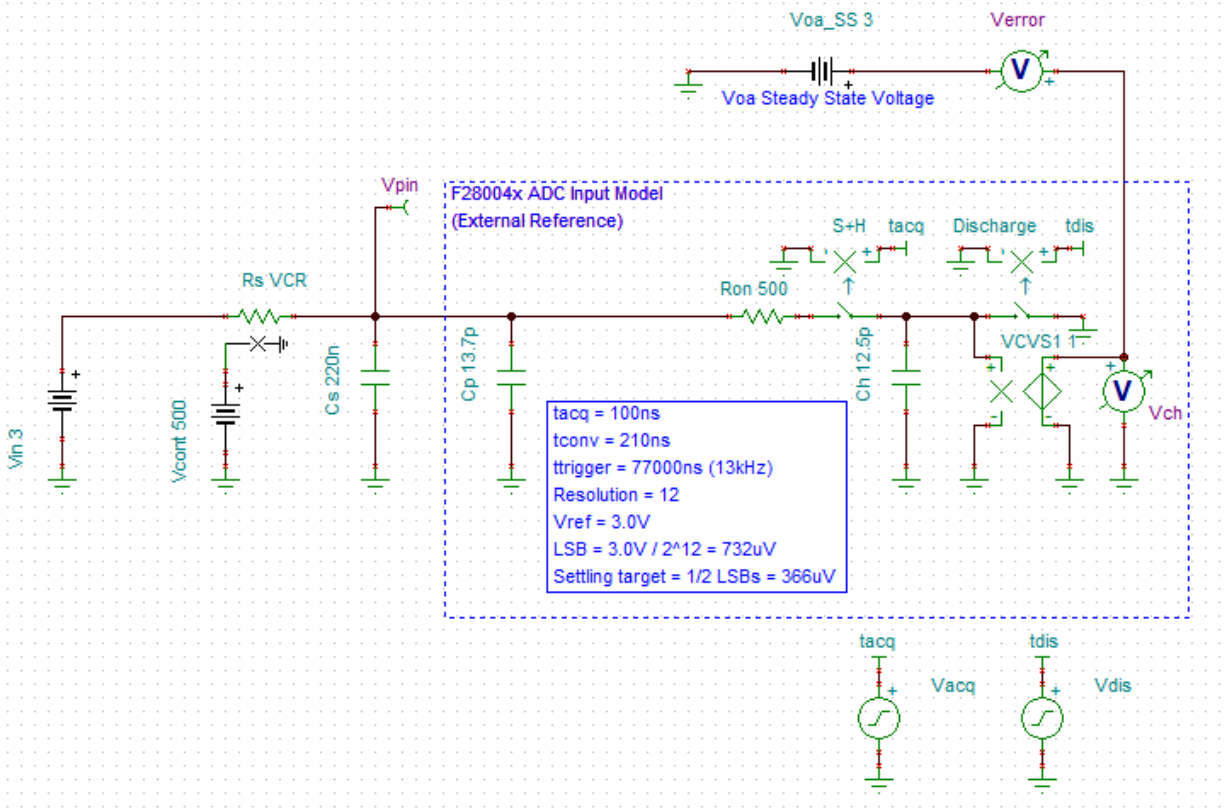

Figure 5-1. Example 1: Simulation Circuit

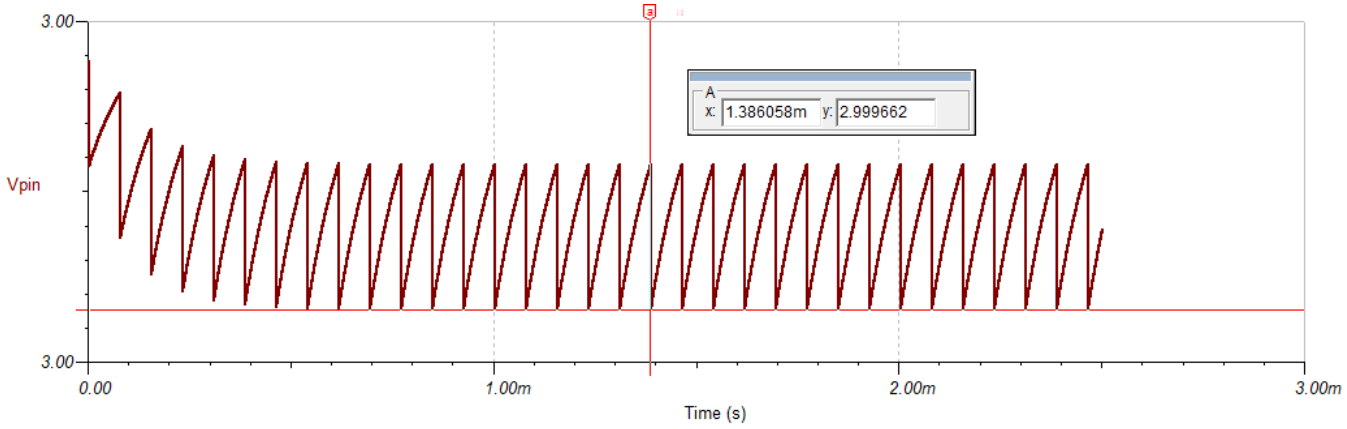

Figure 5-2. Example 1: Simulation Results

5.1.3 Example 1: Worksheet

Table 5-1. Example 1: ADC Charge Sharing Design Worksheet

Symbol	Description	Value	Comments
N	Target settling resolution (bits)	12	Usually the same as the resolution of the ADC. Lower resolution can be targeted to relax the input design requirements
V_{fs}	Full scale voltage range	3.0 V	In external reference mode, this is the voltage supplied to the VREFHI pin (usually 3.0 V or 2.5 V) In internal reference mode, this is the effective input range based on the selected reference mode (usually 3.3 V or 2.5 V)
V_{errmax}	Maximum error target	366 µV	V_{fs} / 2^{N+1} Can be further divided into two components: charge-sharing error and tracking error, each V_{errmax} / 2
t_{sh}	S+H time	80 ns	As long as C_s is sized appropriately for charge-sharing, the minimum value from the ADC data manual can be used.
C_h	ADC S+H capacitance	12.5 pF	Provided in the data manual table "Input Model Parameters"
C_p	ADC pin parasitic capacitance	0 pF (assumed negligible)	Provided in the data manual table "Per-Channel Parasitic Capacitance"
C_s	Source capacitance	220 nF	At least ($2^{N+2} \cdot C_H$) - C_p
R_s	Source resistance	500Ω	Output resistance of source driving ADC. Can also be intentionally selected.
f_s	Sample Rate	N/A	Sample rate on channel of interest. Usually a requirement from the application.
BW_s	Source signal required bandwidth.	500 Hz	Source signal required bandwidth.
R_{smax}	Max allowable source resistance	N/A	If f_s is known, calculate as 1 / ($0.7 \cdot f_s \cdot C_s$) , then ensure that $R_s < R_{smax}$. If the condition is not met, additional design iteration is needed.
f_{smax}	Max allowable sampling frequency	13 kHz	If R_s is known, calculate as 1 / ($0.7 \cdot R_s \cdot C_s$), then ensure that $f_s < f_{smax}$. If the condition is not met, additional design iteration is needed.
BW_{RsCs}	Filter bandwidth from C_s and R_s	1.4 kHz	1 / ($2 \pi C_s R_s$) Ensure that BW_{RsCs} > BW_s , otherwise additional design iteration is needed.
V_{oa_ss}	Steady state op-amp output voltage	3.0V	If no op-amp is used, set $V_{oa\_ss} = V_{fs}$. Otherwise, this can be generated from DC nodal analysis of the V_{oa} node. Copy to Voa_ss before proceeding with other simulations.
BWOPA	ADC driver op-amp minimum bandwidth	N/A	If an op-amp is needed, bandwidth should be at least 4 times BWRsCs
Op-amp	Selected Op-amp part number	N/A	Record selected op-amp here (if needed).
V_{err}	Actual settling error from simulation	338 µV	Ensure $V_{err} < V_{errmax}$ Otherwise, additional design iteration is needed

5.2 Example 2: Adding an Op-amp

In this example, consider a situation similar to Section 5.1. A sensor with known output impedance of 500Ω is to be connected to the 12-bit ADC of an F28004x device. However, this time assume the sensor bandwidth is much higher: 10kHz, and the system uses a fixed sampling rate of 24ksps. The ADC is operating with a 3.0V external reference and full settling performance of 12+1 bits is still desired.

5.2.1 Example 2: Analysis

Example 1 determined that the maximum sample rate with 500Ω source resistance was 13ksps. Since the requirement for 24ksps sampling was added in this example, some changes will be needed. One possibility would be to relax the settling performance (see Section 5.3), but this example will instead isolate the source resistance using an op-amp.

C_s will remain 220nF and the maximum R_s can then be calculated using the equation:

R_{smax} = 1 / ($0.7 \cdot f_s \cdot C_s$)= 0.7 / (0.7·24kHz·220nF) = 270Ω

Since the op-amp isolates the original source resistance of 500Ω, R_s can be selected to be any value less than 270 Ω. Since the signal has 10kHz bandwidth, R_s should be selected to be no more than 68Ω, since this gives a bandwidth just over the signal bandwidth of 10kHz:

$BW_{RsCs} = 1 / (2\pi \cdot C_s \cdot R_s) = 1/ (2\pi \cdot 220nF \cdot 68) = 10.6kHz$

R_s could also be selected to be 56Ω, as this standard resistor value gives a filter bandwidth just over 12kHz, resulting in an anti-aliasing filter for the 24kHz sampling.

When selecting the op-amp, a bandwidth of at least 4 time BW_{RsCs}

should be selected. In this case, the bandwidth required would be at least 40kHz, which is a very easy requirement to meet. TLV07 was selected due to low cost, low noise, low V_{os}, and ample bandwidth for this application.

5.2.2 Example 2: Simulation

Since this input design contains an op-amp, the first step is perform a DC nodal analysis to determine the steady-state output voltage of the op-amp. The voltage is determined to be 2.999997V. The full simulation circuit (populated to include V_{oa_ss} = 2.999997V) can be seen in Figure 5-3.

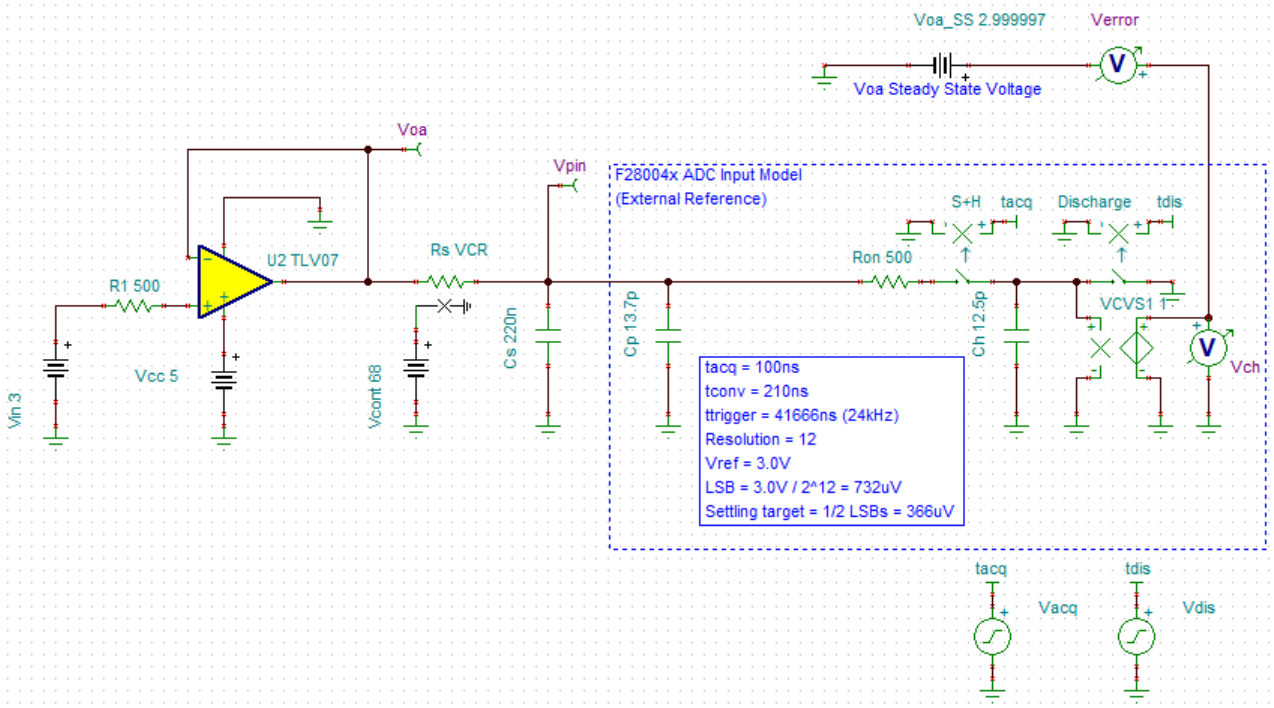

Figure 5-3. Example 2: Simulation Circuit

Running a transient analysis from 1 ms to 2 ms gives the results seen in Figure 5-4. The overall settling error is around 2.999997 V - 2.999814 V = 183 µV. This is well within the settling error target of 366 µV.

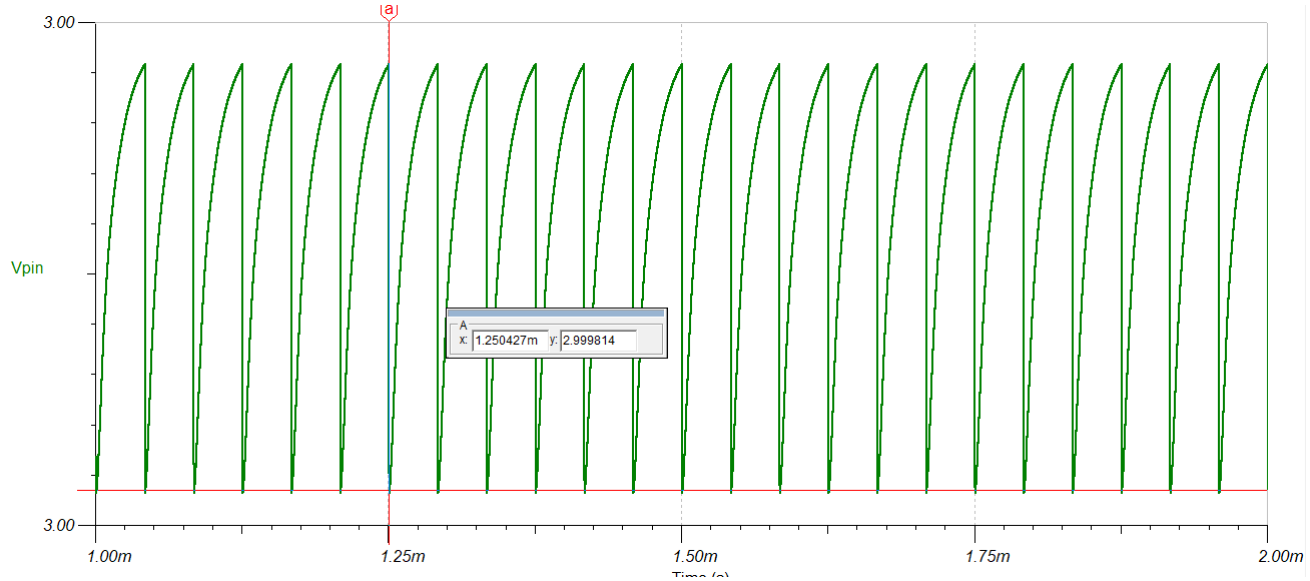

Figure 5-4. Example 2: Simulation Results

Because the op-amp is driving a large capacitive load, it is also good practice to run a phase margin simulation to ensure the driving op-amp is stable. The circuit setup for this can be seen in Figure 5-5 and the results can be seen in Figure 5-6. The measured phase margin is 64 degrees. Since this is >45 degrees, the circuit can be assumed to be stable. For more information on how to run the stability simulation refer to the TI precision labs video series: TI Precision Labs - Op amps: Stability.

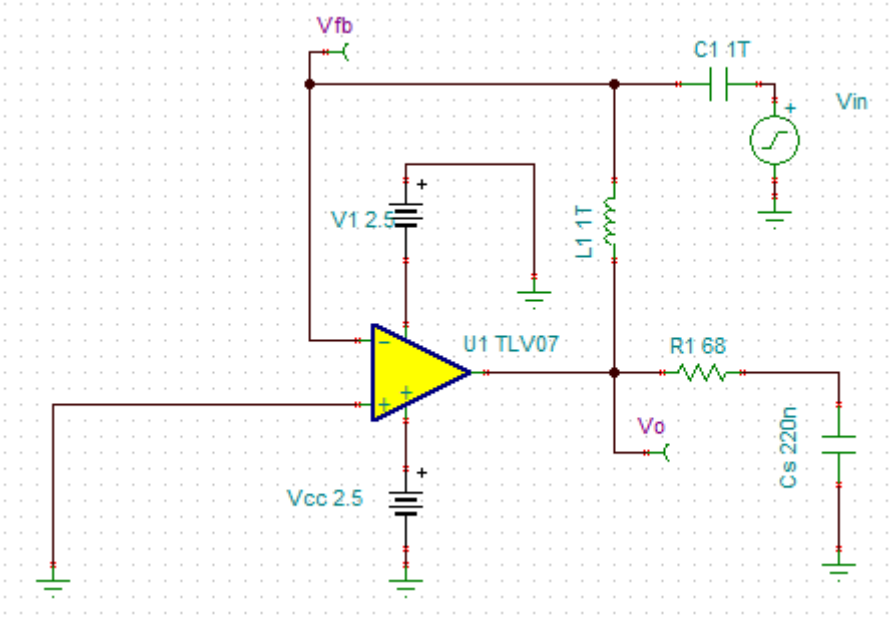

Figure 5-5. Example 2: Stability Simulation Circuit

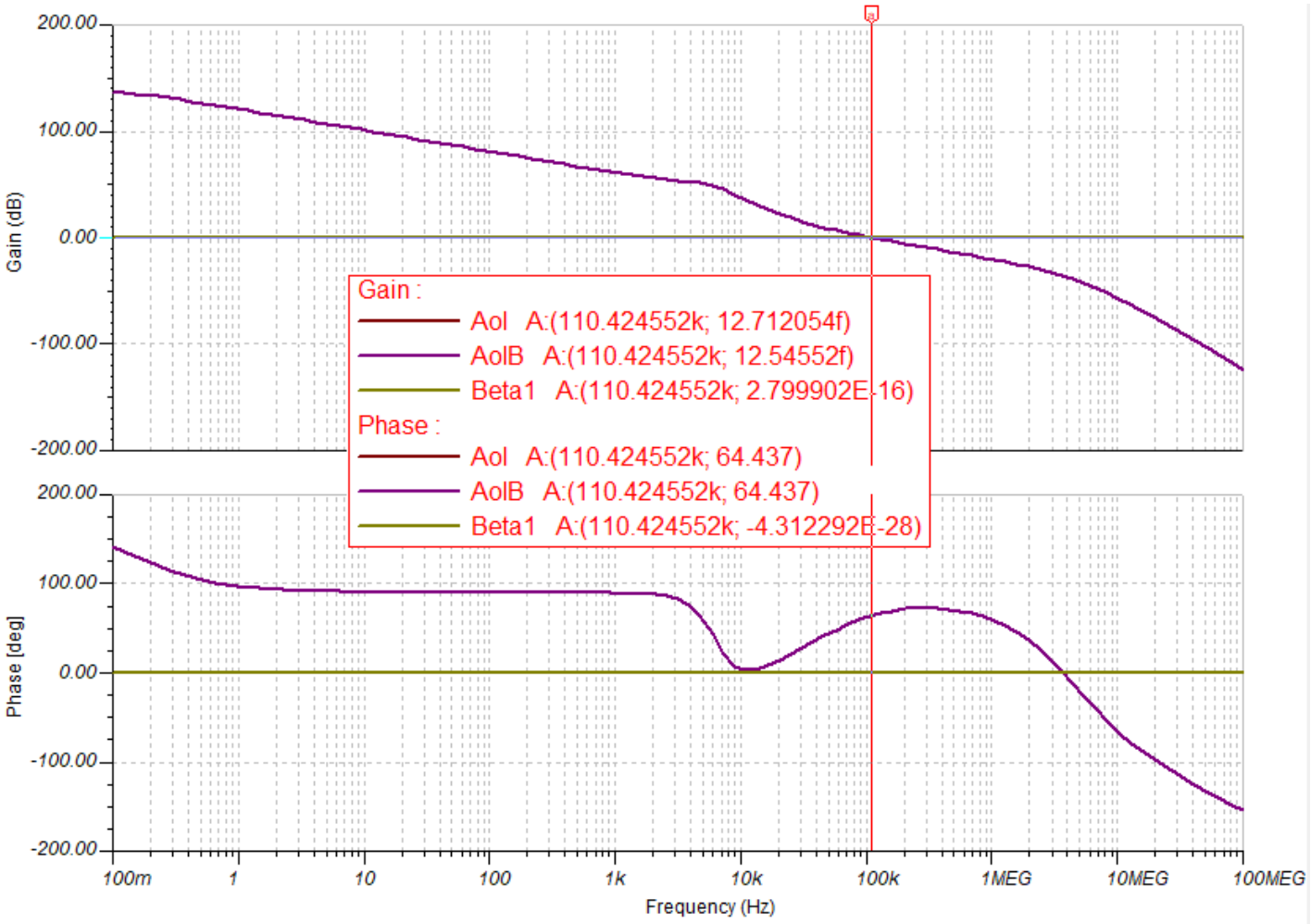

Figure 5-6. Example 2: Stability Simulation Results

5.2.3 Example 2: Worksheet

Table 5-2. Example 2: ADC Charge Sharing Design Worksheet

Symbol	Description	Value	Comments
N	Target settling resolution (bits)	12	Usually the same as the resolution of the ADC. Lower resolution can be targeted to relax the input design requirements
V_{fs}	Full scale voltage range	3.0 V	In external reference mode, this is the voltage supplied to the VREFHI pin (usually 3.0 V or 2.5 V) In internal reference mode, this is the effective input range based on the selected reference mode (usually 3.3 V or 2.5 V)
V_{errmax}	Maximum error target	366 µV	V_{fs} / 2^{N+1} Can be further divided into two components: charge-sharing error and tracking error, each V_{errmax} / 2
t_{sh}	S+H time	80 ns	As long as C_s is sized appropriately for charge-sharing, the minimum value from the ADC data manual can be used.
C_h	ADC S+H capacitance	12.5 pF	Provided in the data manual table "Input Model Parameters"
C_p	ADC pin parasitic capacitance	0 pF (assumed negligible)	Provided in the data manual table "Per-Channel Parasitic Capacitance"
C_s	Source capacitance	220nF	At least ($2^{N+2} \cdot C_H$) - C_p
R_s	Source resistance	68Ω	Output resistance of source driving ADC. Can also be intentionally selected.
f_s	Sample Rate	24 ksps	Sample rate on channel of interest. Usually a requirement from the application.
BW_s	Source signal required bandwidth.	10 kHz	Source signal required bandwidth.

Table 5-2. Example 2: ADC Charge Sharing Design Worksheet (continued)

Symbol	Description	Value	Comments
R_{smax}	Max allowable source resistance	270Ω	If f_s is known, calculate as 1 / (0.7·f_s·C_s) , then ensure that R_s < R_{smax} . If the condition is not met, additional design iteration is needed.
f_{smax}	Max allowable sampling frequency	N/A	If R_s is known, calculate as 1 / (0.7·R_s · C_s) , then ensure that f_s < f_{smax}. If the condition is not met, additional design iteration is needed.
BW_{RsCs}	Filter bandwidth from C_s and R_s	10.6 kHz	1 / (2 π C_s R_s) Ensure that BW_{RsCs} > BW_s , otherwise additional design iteration is needed.
V_{oa_ss}	Steady state op-amp output voltage	2.999997 V	If no op-amp is used, set V_{oa_ss} = V_{fs}. Otherwise, this can be generated from DC nodal analysis of the V_{oa} node. Copy to Voa_ss before proceeding with other simulations.
BWOPA	ADC driver op-amp minimum bandwidth	40 kHz	If an op-amp is needed, bandwidth should be at least 4 times BWRsCs
Op-amp	Selected Op-amp part number	TLV07	Record selected op-amp here (if needed).
V_{err}	Actual settling error from simulation	183 µV	Ensure V_{err} < V_{errmax} Otherwise, additional design iteration is needed

5.3 Example 3: Reduced Settling Target

In this example, consider a system with a fixed sampling rate of 96ksps. A set of analog temperature sensors (yet to be selected) is to be connected to the 12-bit ADC of an F28004x device. The ADC is operating with a 3.0V external reference. Analysis and simulation will be used to determine the maximum source resistance the sensor should exhibit to be directly connected using charge-sharing. The sensors only require 8-bit settling performance (~0.4%). Analysis and simulation will be used to determine the maximum source resistance that can be supported for this set of sensors.

5.3.1 Example 3: Analysis

The C_H value of the F28004x ADC can be found to be 12.5pF in the device data manual. C_p is assumed to be negligible. C_s is therefore sized, assuming a reduced settling performance:

$C_s = (2^{N+2} \cdot C_H) - C_p = (2^{8+1} \cdot 12.5pF) - 0pF = 6.4nF$

Which is then rounded up to C_s = 6.8nF. The maximum source resistance can then be calculated using the equation:

$R_{smax} = 1 / (0.7 \cdot f_s \cdot C_s) = 1 / (0.7 \cdot 96ksps \cdot 6.8nF) = 2188Ω$

So if the temperature sensor has an output impedance of about 2.2kΩ or lower, it should be possible to directly interface it to the ADC using a charge-sharing capacitor.

And the external low-pass filter bandwidth (assuming the maximum source resistance) would be:

$BW_{RsCs} = 1 / (2\pi \cdot C_s \cdot R_s) = 1/ (2\pi \cdot 6.8nF \cdot 2188Ω) = 10.7kHz$

Which should be plenty for a temperature sensor. Furthermore, if the selected temperature sensor has output resistance lower than 2.2kΩ, intentional series resistance could be added to reduce the filter bandwidth (for noise rejection purposes). Alternately, C_s could also instead be increased, which has the advantage of providing better charge-sharing settling performance and not adding an additional component.

5.3.2 Example 3: Simulation

The simulation is setup using the worst-case source impedance as shown in Figure 5-7. A transient analysis is then run from 500 µs to 750 µs, resulting in the measured waveform as shown in Figure 5-8. The final measured settling error is 3 V - 2.989126 V = 10.9 mV = 14.8 LSBs = 0.36% of full-scale range. This is within the settling error target of 0.4%.

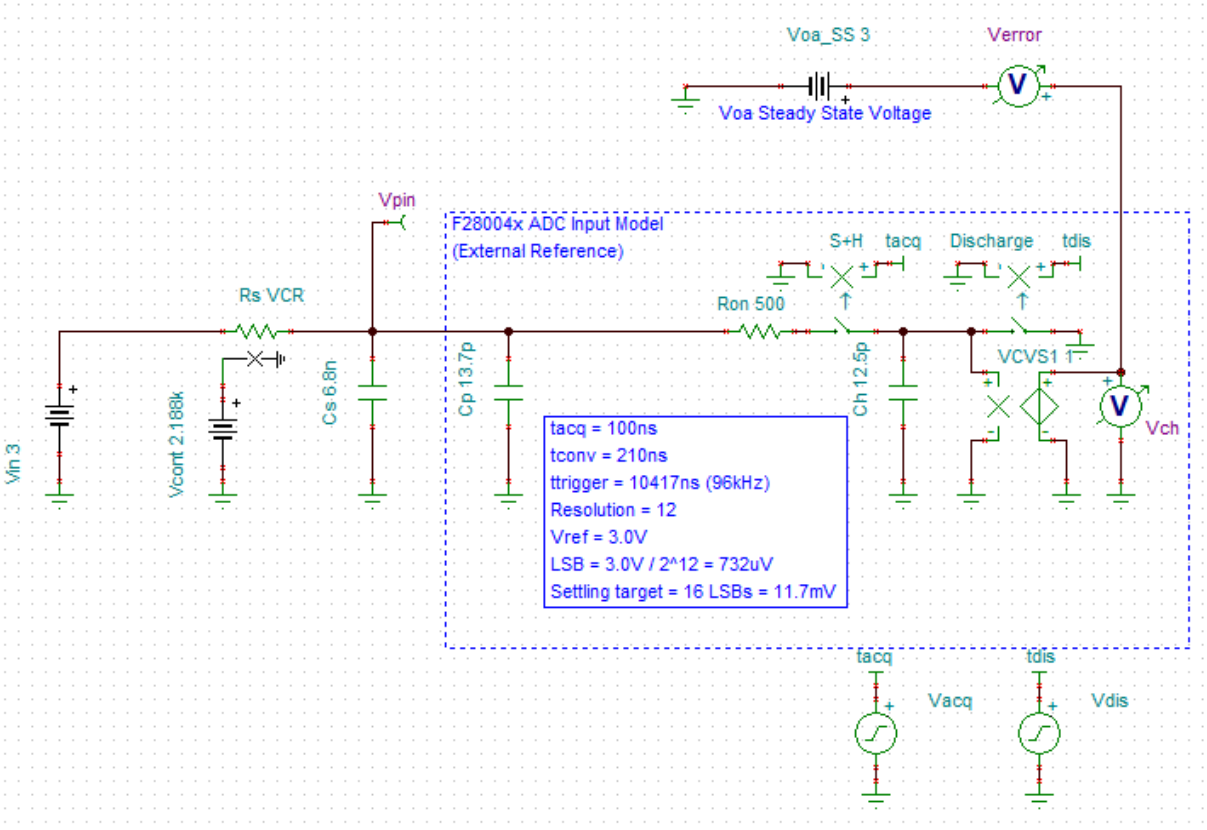

Figure 5-7. Example 3: Simulation Circuit

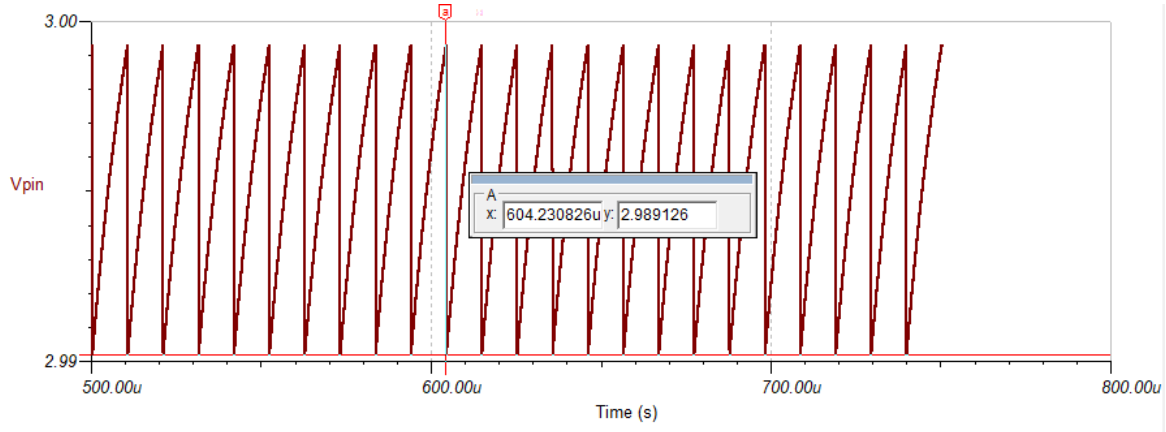

Figure 5-8. Example 3: Simulation Results

5.3.3 Example 3: Worksheet

Table 5-3. Example 3: ADC Charge Sharing Design Worksheet

Symbol	Description	Value	Comments
N	Target settling resolution (bits)	7 (to get 8-bit settling)	Usually the same as the resolution of the ADC. Lower resolution can be targeted to relax the input design requirements
V_{fs}	Full scale voltage range	3.0 V	In external reference mode, this is the voltage supplied to the VREFHI pin (usually 3.0 V or 2.5 V) In internal reference mode, this is the effective input range based on the selected reference mode (usually 3.3 V or 2.5 V)
V_{errmax}	Maximum error target	11.7 mV	V_{fs} / 2^{N+1} Can be further divided into two components: charge-sharing error and tracking error, each V_{errmax} / 2
t_{sh}	S+H time	80 ns	As long as C_s is sized appropriately for charge-sharing, the minimum value from the ADC data manual can be used.
C_h	ADC S+H capacitance	12.5 pF	Provided in the data manual table "Input Model Parameters"
C_p	ADC pin parasitic capacitance	0 pF (assumed negligible)	Provided in the data manual table "Per-Channel Parasitic Capacitance"
C_s	Source capacitance	6.8 nF	At least ($2^{N+2} \cdot C_H$) - C_p
R_s	Source resistance	N/A	Output resistance of source driving ADC. Can also be intentionally selected.
f_s	Sample Rate	96 ksps	Sample rate on channel of interest. Usually a requirement from the application.
BW_s	Source signal required bandwidth.	low	Source signal required bandwidth.
R_{smax}	Max allowable source resistance	2188Ω	If f_s is known, calculate as 1 / ($0.7 \cdot f_s \cdot C_s$), then ensure that $R_s < R_{smax}$. If the condition is not met, additional design iteration is needed.
f_{smax}	Max allowable sampling frequency	N/A	If R_s is known, calculate as 1 / ($0.7 \cdot R_s$. C_s), then ensure that $f_s < f_{smax}$. If the condition is not met, additional design iteration is needed.
BW_{RsCs}	Filter bandwidth from C_s and R_s	10.7 kHz	1 / (2 π C_s R_s) Ensure that $BW_{RsCs} > BW_s$, otherwise additional design iteration is needed.
V_{oa_ss}	Steady state op-amp output voltage	3 V	If no op-amp is used, set $V_{oa\_ss} = V_{fs}$. Otherwise, this can be generated from DC nodal analysis of the V_{oa} node. Copy to Voa_ss before proceeding with other simulations.
BWOPA	ADC driver op-amp minimum bandwidth	N/A	If an op-amp is needed, bandwidth should be at least 4 times BWRsCs
Op-amp	Selected Op-amp part number	N/A	Record selected op-amp here (if needed).
V_{err}	Actual settling error from simulation	10.9 mV	Ensure $V_{err} < V_{errmax}$ Otherwise, additional design iteration is needed

5.4 Example 4: Voltage Divider

In this example, consider sampling of a 400 V bus using a voltage divider. A voltage divider comprised of a 160 kΩ and 1.2 kΩ resistors will provide an attenuation factor of 0.00744, mapping a 400V input to 2.978 V on the ADC input. This will be connected to the 12-bit ADC of an F28004x device. The ADC is operating with a 3.0 V external reference. Analysis and simulation will be used to determine the maximum sampling rate and the signal bandwidth this divider can support. 10 + 1 bit (<0.1%) settling performance is required.

5.4.1 Example 4: Analysis

The C_H value of the F28004x ADC is determined to be 12.5 pF from the device-specific data manual. C_p is assumed to be negligible. C_s is therefore sized accordingly:

$$C_s = (2^{N+2} \cdot C_H) - C_p = (2^{10+2} \cdot 12.5\ pF) - 0\ pF = 51.2\ nF$$

Which is then rounded to C_s = 51 nF.

The equivalent series resistance of the voltage divider is 1.2kΩ || 160kΩ = 1191Ω. The maximum sample rate is then calculated using the equation:

$$f_{smax} = 1/\ (0.7 \cdot R_s \cdot C_s) = 1\ /\ (0.7 \cdot 1191\Omega \cdot 51\ nF) = 23.5\ kHz$$

And the external low-pass filter bandwidth is:

$$BW_{RsCs} = 1\ /\ (2\pi \cdot C_s \cdot R_s\ ) = 1/\ (2\pi \cdot 51\ nF \cdot 1191\Omega\ ) = 2.6\ kHz$$

If a higher sample rate is needed, an op-amp can be added to isolate the equivalent resistance of the voltage divider from the ADC input (see Section 5.2). Alternately, both legs of the voltage divider can be proportionally reduced in resistance. This results in a lower equivalent resistance (and thus faster allowable sampling speed) at the expense of additional static current draw through the voltage divider.

5.4.2 Example 4: Simulation

The first step for simulating the ADC driver behavior is to determine the DC voltage at the output of the voltage divider assuming a 400 V input. This can done using the same method as the op-amp steady state voltage output: a DC nodal analysis. The annotated circuit following this analysis is shown in Figure 5-9. It can be seen that the voltage divider output is 2.977667 V. This value is copied to V_{oa_ss} so that the value of Verror correctly reflects only the settling error. Finally, a transient analysis is run from 1 ms to 2 ms. The results can be seen in Figure 5-10. The final settling error is 2.977667 V - 297622 V = 1.45 mV

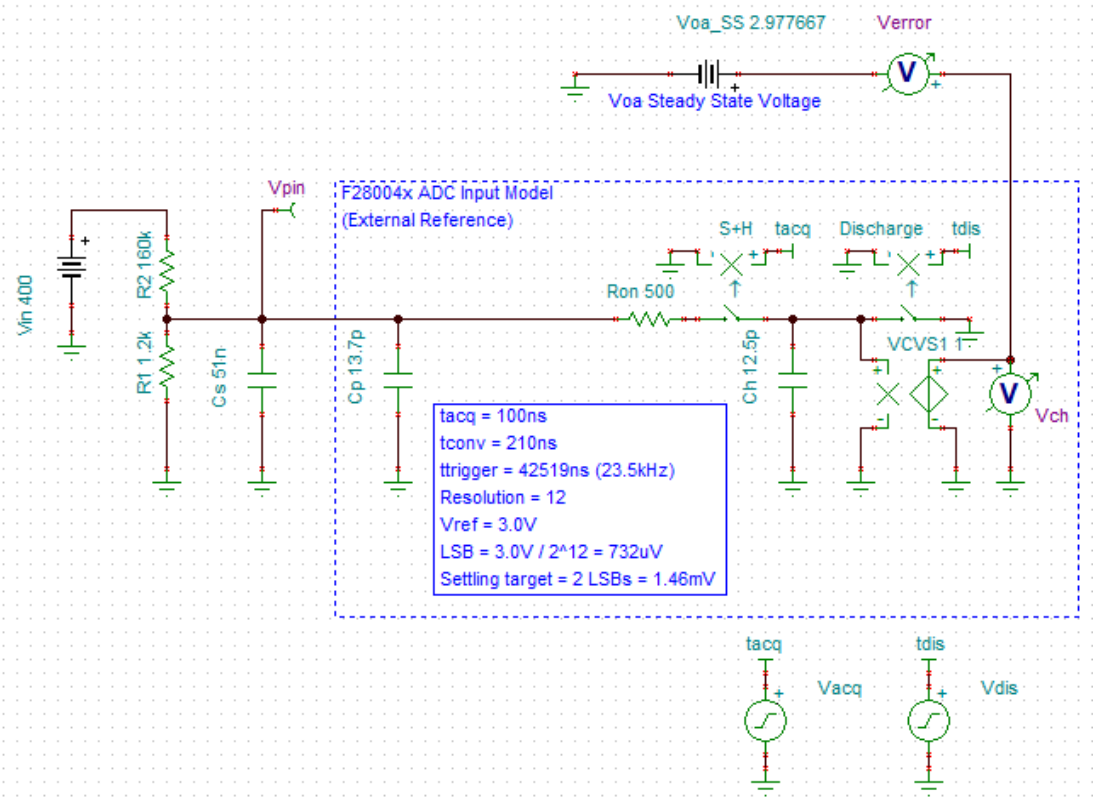

Figure 5-9. Example 4: Simulation Circuit

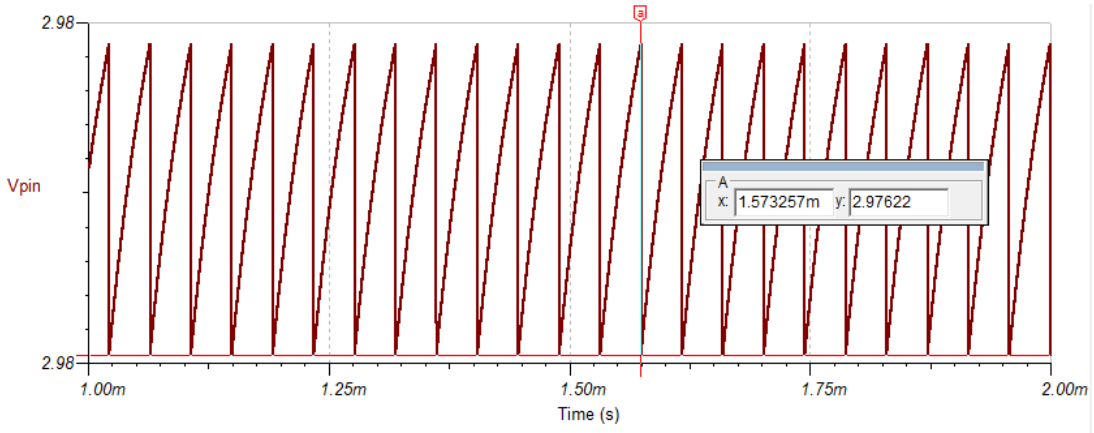

Figure 5-10. Example 4: Simulation Results

5.4.3 Example 4: Worksheet

Table 5-4. Example 4: ADC Charge Sharing Design Worksheet

Symbol	Description	Value	Comments
N	Target settling resolution (bits)	10	Usually the same as the resolution of the ADC. Lower resolution can be targeted to relax the input design requirements
V_{fs}	Full scale voltage range	3.0 V	In external reference mode, this is the voltage supplied to the VREFHI pin (usually 3.0 V or 2.5 V) In internal reference mode, this is the effective input range based on the selected reference mode (usually 3.3 V or 2.5 V)
V_{errmax}	Maximum error target	1.46 mV	V_{fs} / 2^{N+1} Can be further divided into two components: charge-sharing error and tracking error, each V_{errmax} / 2
t_{sh}	S+H time	80 ns	As long as C_s is sized appropriately for charge-sharing, the minimum value from the ADC data manual can be used.
C_h	ADC S+H capacitance	12.5 pF	Provided in the data manual table "Input Model Parameters"
C_p	ADC pin parasitic capacitance	0 pF (assumed negligible)	Provided in the data manual table "Per-Channel Parasitic Capacitance"
C_s	Source capacitance	51 nF	At least ($2^{N+2} \cdot C_H$) - C_p
R_s	Source resistance	1191Ω	Output resistance of source driving ADC. Can also be intentionally selected.
f_s	Sample Rate	N/A	Sample rate on channel of interest. Usually a requirement from the application.
BW_s	Source signal required bandwidth.		Source signal required bandwidth.
R_{smax}	Max allowable source resistance	N/A	If f_s is known, calculate as 1 / ($0.7 \cdot f_s \cdot C_s$), then ensure that $R_s < R_{smax}$. If the condition is not met, additional design iteration is needed.
f_{smax}	Max allowable sampling frequency	23.5 ksps	If R_s is known, calculate as 1 / ($0.7 \cdot R_s \cdot C_s$), then ensure that $f_s < f_{smax}$. If the condition is not met, additional design iteration is needed.
BW_{RsCs}	Filter bandwidth from C_s and R_s	2.6 kHz	1 / ($2 \pi C_s R_s$) Ensure that $BW_{RsCs} > BW_s$, otherwise additional design iteration is needed.
V_{oa_ss}	Steady state op-amp output voltage	2.977667 V	If no op-amp is used, set $V_{oa\_ss} = V_{fs}$. Otherwise, this can be generated from DC nodal analysis of the V_{oa} node. Copy to Voa_ss before proceeding with other simulations.
BWOPA	ADC driver op-amp minimum bandwidth	N/A	If an op-amp is needed, bandwidth should be at least 4 times BWRsCs
Op-amp	Selected Op-amp part number	N/A	Record selected op-amp here (if needed).
V_{err}	Actual settling error from simulation	1.45 mV	Ensure $V_{err} < V_{errmax}$ Otherwise, additional design iteration is needed

6 Summary

Designing ADC signal conditioning circuits for proper input settling is necessary to achieve good sampling performance in real-time control applications. Using the analysis and simulation methods presented in this report, it is possible to create simple low-cost ADC driving circuits using the charge-sharing method. These circuits can also result in reduced sampling latency by allowing minimum S+H time and can reduce sampled noise by simultaneously providing low-pass filtering.

A Appendix: ADC Input Settling Motivation

The following sections provide additional background on ADC input settling and the types of errors that can occur if proper input settling design is not achieved.

A.1 Mechanism of ADC Input Settling

To convert a sensed analog voltage to a digital conversion result, the ADC first must accurately capture the applied input voltage into its sample-and-hold circuit (S+H). As shown in Figure A-1, this entails charging the internal ADC S+H capacitor (C_h) to within some acceptable tolerance (typically 0.5 LSBs) of the applied voltage within the configured acquisition window time (also referred to as the S+H time).

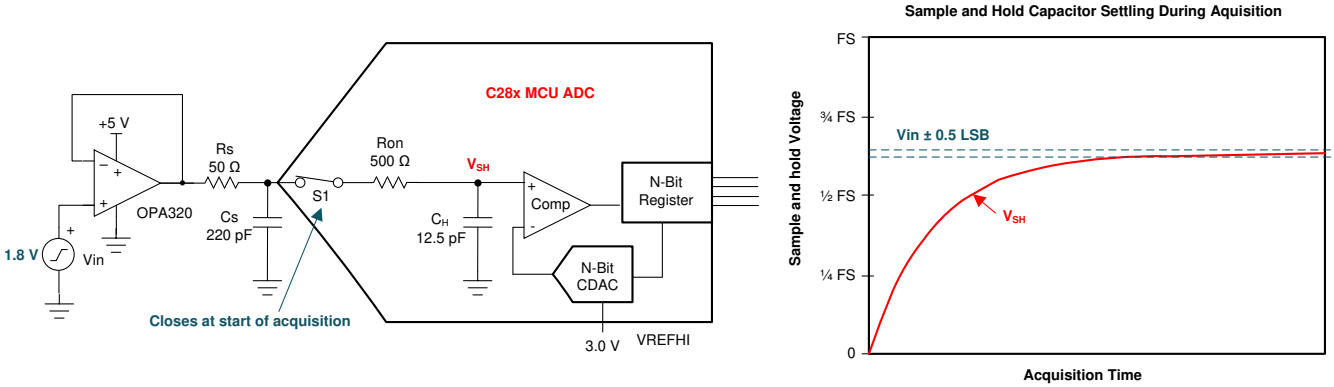

Figure A-1. Settling of the ADC S+H Capacitor

Quickly charging C_h to the applied voltage is complicated by the finite bandwidth and settling time of the external ADC driver circuit and of the settling time of the internal ADC S+H circuit. In Figure A-1, the driver is show as an op-amp (OPA320), which has a finite bandwidth, and the driver circuit also has intentionally placed source resistance (R_s) and intentionally placed source capacitance (Cs) which have a finite settling time determined by their RC time constant. Note that other circuit topologies are possible for driving the ADC, and these circuits may have additional components which need to be modeled to ensure appropriate settling time. These components could include unintentional parasitics such as the output impedance of a sensor or the effective source resistance of a voltage divider. Figure A-1 also shows that the ADC has an internal parasitic switch resistance (R_{on}). This, along with C_h, will provide an additional RC time constant that limits settling speed.

A.2 Symptoms of Inadequate Settling

Once a voltage has been captured into the S+H capacitor, the ADC will translate this voltage into a digital conversion result during the conversion phase. The CPU can then use this result to control or monitor the system. However, if the captured voltage does not accurately represent the applied voltage due to settling error, the final conversion result will have errors even if the ADC conversion process is perfect.

These settling errors will manifest differently depending on whether the ADC is sampling the same channel repeatedly or scanning through multiple channels in a sequence. The settling errors will also manifest differently depending on the starting voltage on the S+H capacitor at the beginning of the acquisition phase. Some ADC architectural implementations will have a starting S+H voltage close to the previously sampled voltage while other architectures will usually start the acquisition phase with a discharged S+H capacitor.

A.2.1 Distortion

In the case where the ADC is repeatedly sampling the same signal, settling error typically manifests as distortion of the input signal. In architectures where the S+H voltage starts near the previously sampled voltage, slow moving portions of the input signal will settle better than fast moving portions. An architecture where sequential samples begin their settling from the voltage sampled and held in the previous conversion is illustrated in Figure A-2.

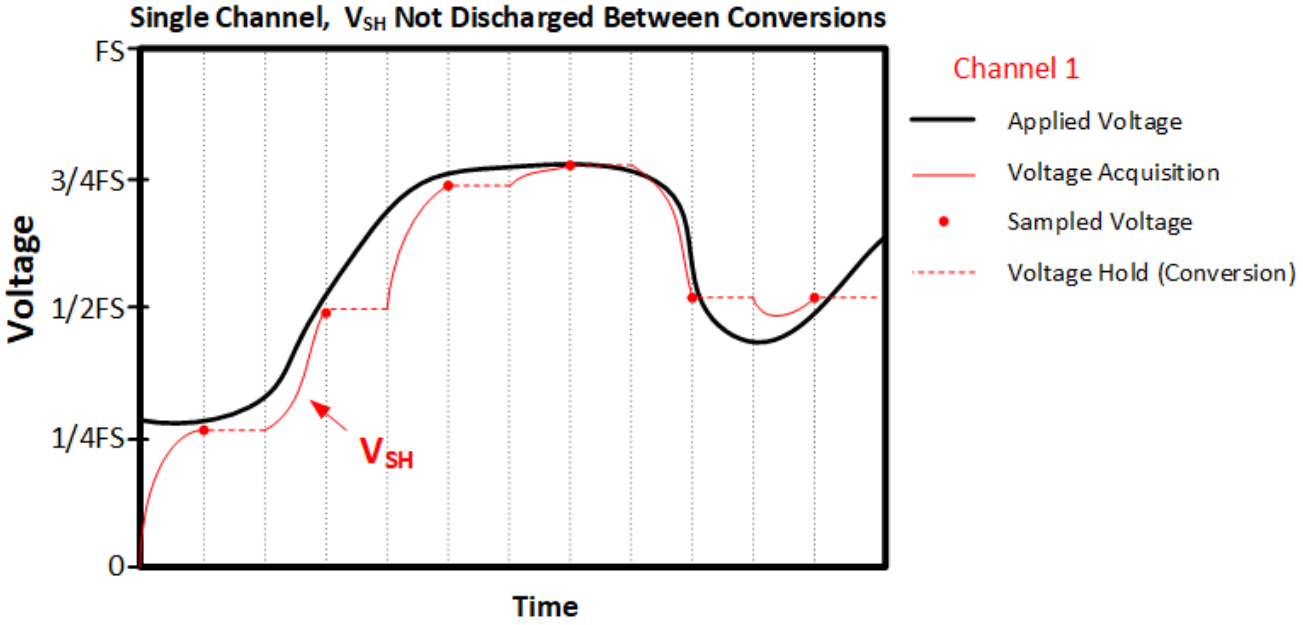

Figure A-2. Sequence of Samples With C_H Retained Between Conversions

In architectures where the S+H capacitor starts each acquisition phase discharged, higher input voltages will have worse settling, resulting in distorted scaling of the signal. An architecture where sequential samples always beginning their settling from near zero-scale is illustrated in Figure A-3.

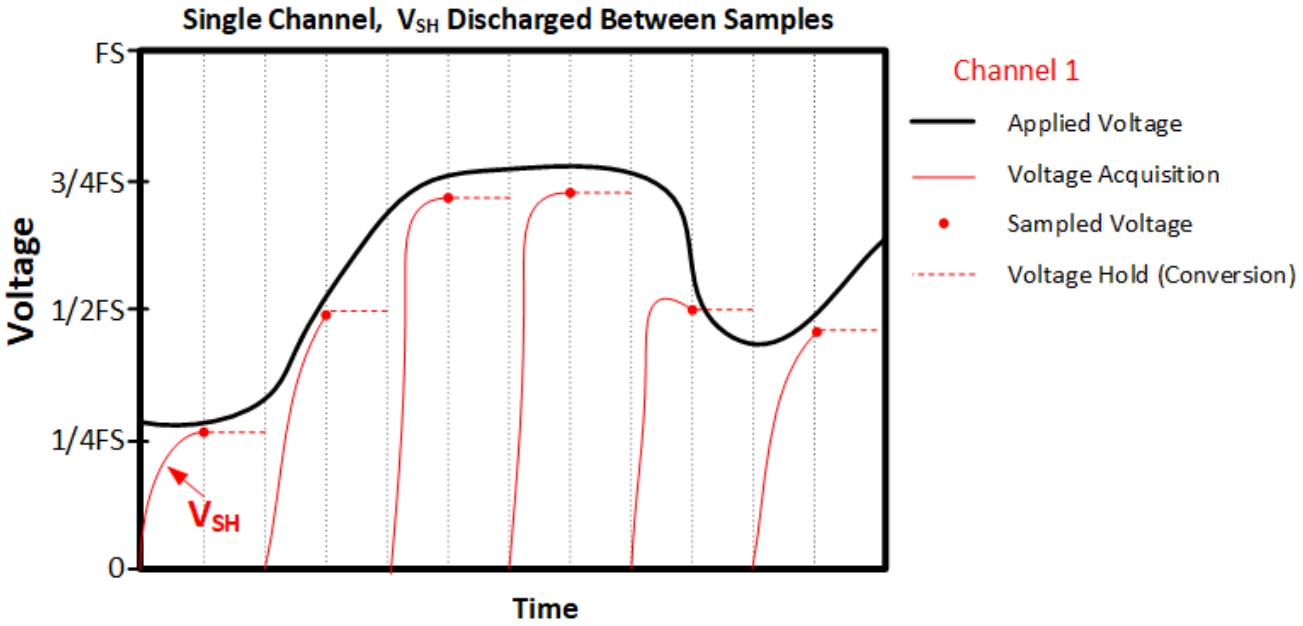

Figure A-3. Sequence of Samples With C_H Discharged Between Conversions

A.2.2 Memory Cross-Talk

In many C2000 MCU applications, a typical use case is using the ADC input multiplexer to scan through multiple channels in a sequence. If a converted channel has inadequate settling, the channel may be pulled towards the voltage of the previous conversion in the sequence. This occurs because the S+H voltage starts near the previously converted voltage and then settles towards (but does not reach) the applied voltage. This tendency for the previous conversion result in a sequence of conversions to affect the current conversion is called memory cross-talk. Memory cross-talk can generally be completely mitigated via appropriate settling design.

A situation where a shared sample and hold must settle back-and-forth between two different multiplexed input signals is illustrated in Figure A-4.

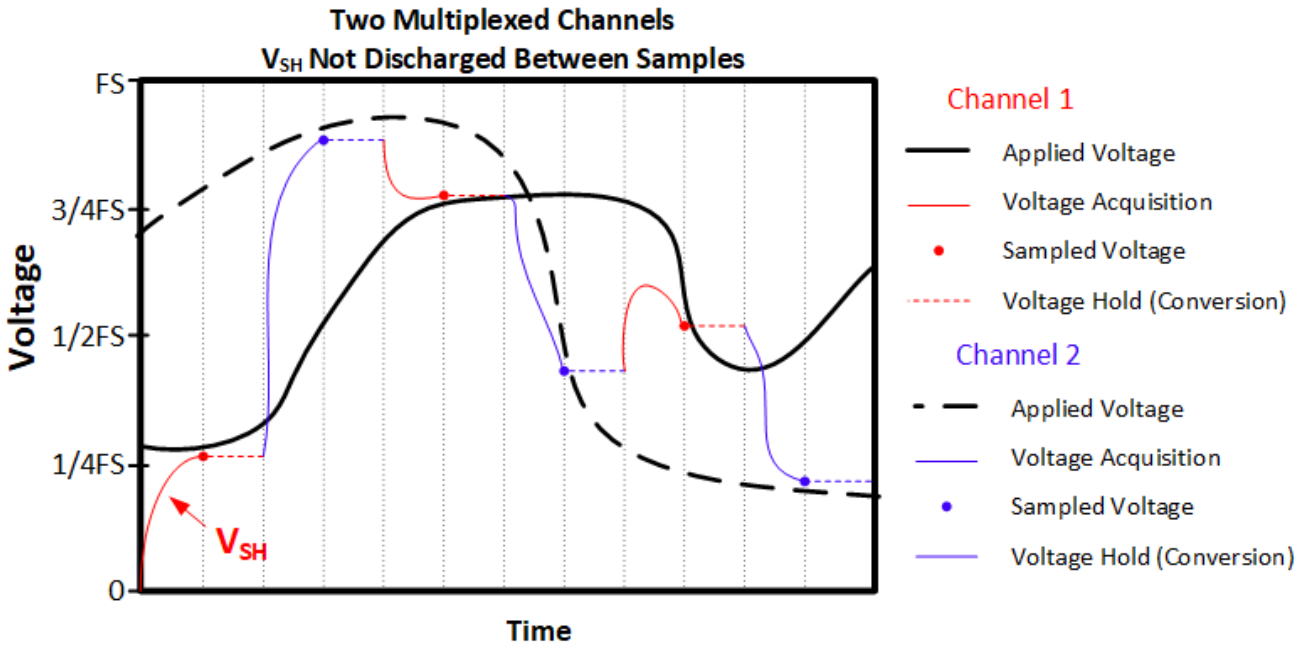

Figure A-4. Sequence of Multiplexed Samples

Converter architectures that start with the S+H capacitor completely discharged generally do not experience significant memory cross-talk (but still experience input settling related distortion if the ADC driving circuits are not appropriate for the allocated acquisition time).

A.2.3 Accuracy

The errors introduced by inadequate input settling generally can not be calibrated out or reduced via oversampling and averaging. Therefore, applications that are concerned with absolute sampling accuracy also need to ensure proper ADC input settling even if the sensed input signal is low-frequency or even DC.

A.2.4 C2000 ADC Architecture

C2000 MCU ADCs will generally start with the S+H capacitor pre-charged to a voltage close to the previous conversion result. The exception to this is for ADCs which support differential signaling, but which are operating in single-ended mode. In this case, the S+H capacitor will start discharged when the previous conversion was from an even numbered channel and the current channel is an odd numbered channel, or vice-versa. For example, the S+H capacitor will start discharged if channel A4 is being sampled after A3 (or vice-versa) but will start close to the previously converted voltage when sampling channel A4 after channel A2 or channel A1 after channel A3.

CAUTION

The above statements about the C2000 ADC architecture are only intended to help with diagnosing problems with inadequate settling. Do not rely on these properties to ensure sufficient ADC input settling. Instead, always ensure that the input can fully settle in the allocated S+H time regardless of any assumptions about the starting voltage of the S+H circuit.

References

- TI Precision Labs - SAR ADC Input Driver Design
- Analog Engineer's Calculator
- TINA-TI
- TI Precision Labs - Op amps: Stability
- Texas Instruments: *TMS320F28004xMicrocontrollers Data Manual*
- Selecting capacitors to minimize distortion in audio applications

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