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Using the Enhanced Quadrature Encoder Pulse (eQEP) Module in TMS320x280x, 28xxx as a Dedicated Capture

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ABSTRACT

This document provides a guide for the use of the eQEP module as a dedicated capture unit and is applicable to the TMS320x280x, 28xxx family of processors.

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1 Introduction

Some applications using the TMS320x280x, 28xxx series of processors may require capture units in addition to the dedicated capture units provided by these processors. In such cases the enhanced quadrature encoder pulse (eQEP) modules can be used as 16-bit capture units.

The eQEP modules are primarily intended to get position, direction, and speed information from rotating machines for high performance motion control applications. Each peripheral is equipped with a capture unit sub-module. When, in an application, one or more of these modules are not being used for their primary function, they can be used as general-purpose capture units using the capture sub-modules. Thus, the device can potentially provide additional capture units.

The speed, direction, and position measurements are critical aspects of high performance motor control applications. This information is extracted from a group of encoder signals generated by optical encoders mounted on the motor. This group typically consists of two square waves and a pulse signal that occurs once every motor revolution. The square waves are 90° apart, which helps detect the direction of rotation by determining which signal leads/lags the other. The third signal provides an index pulse and is identified using different terms such as index, marker, home position, and zero reference. This index signal can be used to indicate an absolute position.

The frequency of the square wave signal is a direct indicator of the speed of the motor. The eQEP module provides the frequency information of the input encoder signals to the DSP for the speed calculations.

Figure 1 shows the functional block diagram of the eQEP peripheral.

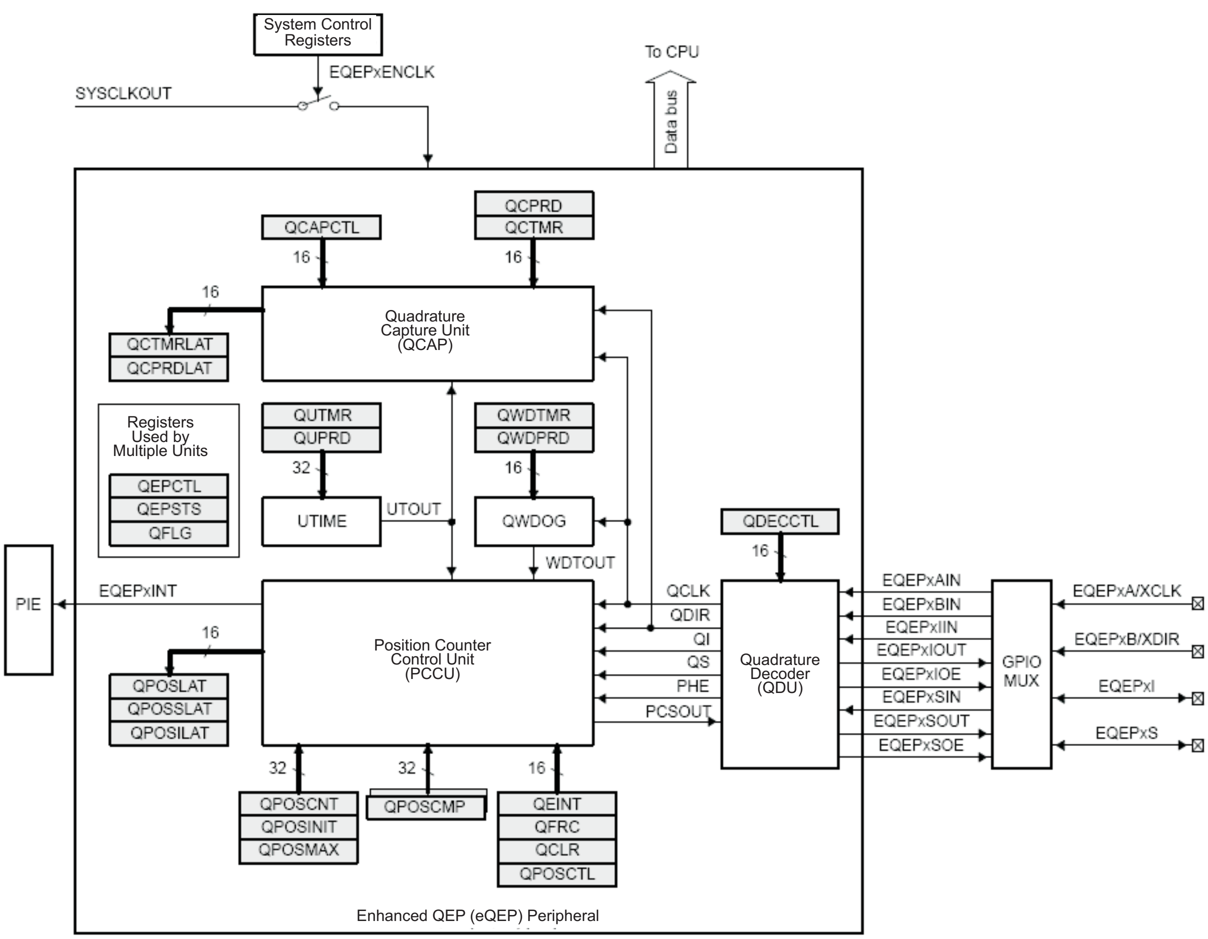

Figure 1. Functional Block Diagram of the eQEP Peripheral

The quadrature decoder unit provides QCLK and QDIR signals to the position counter control unit (PCCU). These signals are derived from the input encoder signals. The position counter counts the number of QCLK pulses for a particular direction for a known period of time. This gives the number of encoder pulses in this period so that the frequency of the input signal can be calculated, which works well for medium to high speed measurements but not for low speeds.

For low speed measurements, the eQEP module is equipped with a capture unit that counts the time elapsed between two consecutive QCLK pulses providing an accurate measurement for the speed calculation. Thus, low speeds can be measured.

When one or more of these eQEP modules are not being used for this purpose, they can be used as general-purpose 16-bit capture unit using the capture sub-modules. This can be achieved by supplying the signal to be captured to the eQEPxA input and grounding the eQEPxB and the index input signal (eQEPxI). The next few sections describe this in detail.

2 Capture Unit of the eQEP Module

Figure 2 depicts the eQEP edge capture unit functional block diagram.

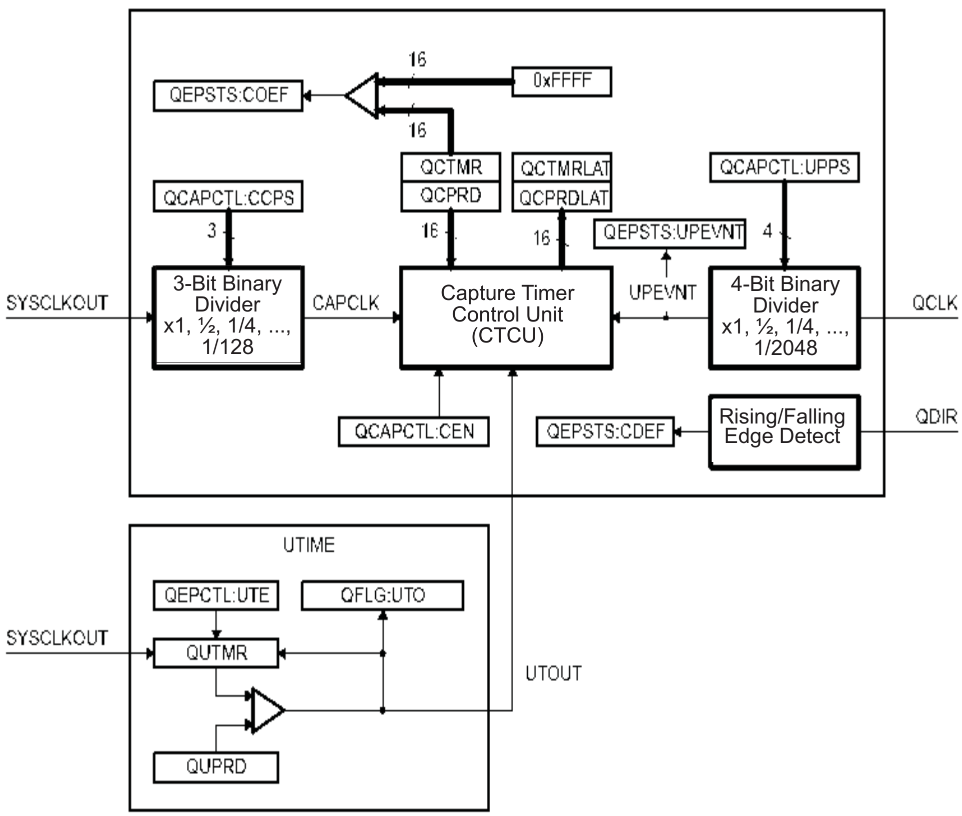

Figure 2. Functional Block Diagram of the eQEP Edge Capture Unit

The quadrature decoder unit generates QCLK and QDIR signals that are input to the capture unit. For speed and direction measurement, the QCLK signal is made up of pulses for each transition on either of the two square wave encoder inputs. Therefore, four QCLK periods correspond to one encoder period as shown in Figure 3.

A 4-bit binary divider generates a unit position event (UPEVNT) signal from the QCLK. On every unit position event, the capture timer (QCTMR) value is latched into the capture period register (QCPRD).

QCTMR is then reset and a flag is set in QEPSTS:UPEVNT, which the software can check and then read the period register for the speed measurement. This flag should be cleared by software by writing a 1. The speed measurement is obtained by measuring the period of the UPEVNT signal. The 4-bit binary divider allows the UPEVNT to be generated on multiples (powers of 2) of the QCLK period (refer to *TMS320x28xx, 28xxx Enhanced Quadrature Encoder Pulse (eQEP) Module Reference Guide* (SPRU790).

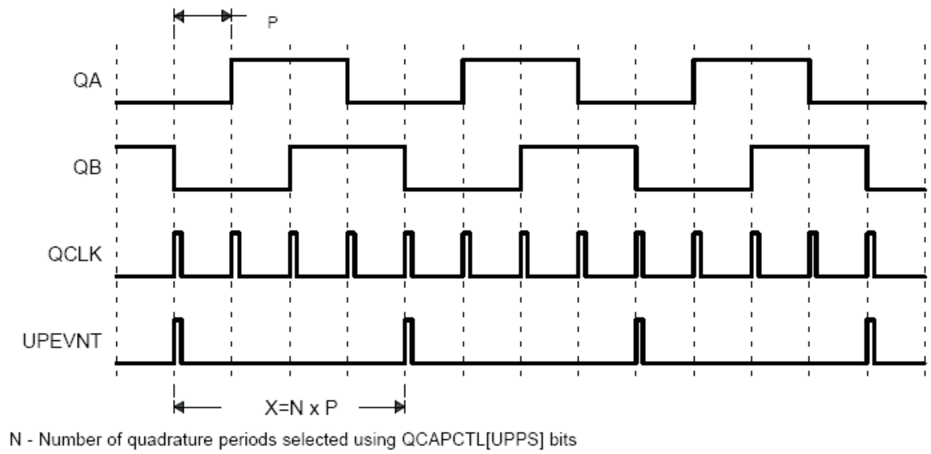

Figure 3. Unit Position Event for Low Speed Measurement (QCAPCTL[UPPS] = 0010)

When the eQEP module is used as a capture unit, the unit position event is generated as shown in Figure 4. The input signal is fed to eQEPxA input pin while the eQEPxB input pin and the index input pin (eQEPxI) are grounded. The UPEVNT is generated every other QCLK pulse.

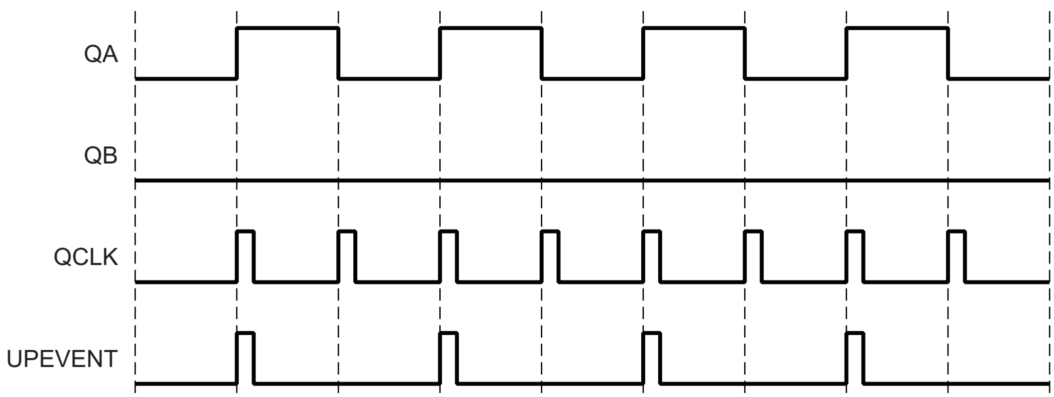

Figure 4. Unit Position Event for Use of eQEP as a Capture Unit (QCAPCTL[UPPS] = 0001)

The capture timer (QCTMR) is clocked by SYSCLKOUT and has a programmable 3-bit prescaler. SYSCLKOUT should be suitably prescaled so that the capture timer doesn't overflow between unit position events. Also, a prescale value that means a timer overflow period close to the UPEVNT period provides a good resolution.

Note: For more information on the eQEP module refer to the *TMS320x28xx, 28xxx Enhanced Quadrature Encoder Pulse Module (eQEP) Reference Guide* (SPRU790).

3 Implementing the Capture Unit

To use the eQEP module as a capture, the following registers need to be configured and used within the code: QPOSMAX, QDECCTL, QEPCTL, QCAPCTL, QPOSCTL, QPOSCMP, QEINT, and QCLR.

3.1 QDECCTL

The quadrature decoder unit allows the QCLK to be derived directly from EQEPxA input. It can be pulsed on the rising and falling edges of the eQEPxA signal or only on its rising edge.

If the QDECCTL:XCR bit is configured as ‘0’, the QCLK pulse is generated on both the edges of eQEPxA. When configured in this manner, it is possible to implement a program that can measure both the period and the pulse width of the input signal by appropriately setting the 4-bit binary divider in the capture unit to generate the UPEVNT every other QCLK.

If the QDECCTL:XCR bit is set to ‘1’, the UPEVNT has to be generated on every QCLK. However, in this case the pulse width measurement is not possible.

To have a QCLK directly derived from eQEPxA, the QDECCTL:QSRC bits have to be set to ‘10’. This always assumes a constant direction, which is not a concern since the eQEPxB pin is always grounded. This also prevents the direction error flag to be set and the position counter to be reset inadvertently. The position counter plays an important role in the use of the eQEP module as a capture unit as discussed next.

3.2 QEPCTL

The capture timer gets latched into the period register on every unit position event (UPEVNT) and is then reset. Once this UPEVNT occurs we need to read the period register value for the capture to complete. The UPEVNT cannot by itself produce an interrupt. However, the position counter can be used to generate an interrupt at an UPEVNT using the position counter overflow (PCO) interrupt.

The position counter is clocked by the QCLK. Therefore, two position counter counts would correspond to an UPEVNT, when the QDECCTL:XCR bit is set to ‘1’. The position counter has to be configured to reset on the maximum position using QEPCTL:PCRM bits. The QPOSMAX register should then be initialized to a value that corresponds to two position counts i.e. one UPEVNT. A position counter overflow interrupt is generated when the counter reaches its maximum count. The period value can then be read from the capture period register in the interrupt service routine. When the QDECCTL:XCR bit is ‘0’ and only the period measurement is required, QPOSMAX should be accordingly initialized to correspond to one position count i.e. one UPEVNT.

A simultaneous pulse width and period measurement can be achieved by using the position-compare unit in addition to the position counter overflow logic discussed above. A position compare interrupt needs to be enabled and the UPEVNT be generated on every other QCLK. The compare value should be programmed such that an interrupt is generated on the very first falling edge after reset, which corresponds to the first position count. The position-compare match interrupt is generated at every compare match. The capture timer value can be read in the interrupt service routine to give the pulse width of the input signal. However, the interrupt service time affects the pulse width measurement since the timer continues to run and its value is not latched while servicing this interrupt. Therefore, this method would serve well to give a good estimate of the pulse width and an exact period value.

Lastly, the position counter needs to be enabled by setting the QEPCTL:QPEN bit.

3.3 QCAPCTL

When the QDECCTL:XCR bit is programmed as ‘1’ (i.e. only period measurement is required), the unit position event (UPEVNT) needs to be generated on every QCLK pulse by programming the QCAPCTL:UPPS bits to ‘0000’. When the QDECCTL:XCR bit is programmed as ‘0’, UPEVNT needs to be generated every other QCLK pulse by initializing the QCAPCTL: UPPS as ‘0001’.

The capture timer (QCTMR) is clocked by SYSCLKOUT and has a programmable 3-bit prescaler: QCAPCTL:CCPS. SYSCLKOUT should be suitably prescaled so that the capture timer does not overflow between unit position events. Also, a prescale value that means a timer overflow period close to the UPEVNT period provides a good resolution.

For example, for a 100 MHz SYSCLKOUT and a 40 Hz input signal, the QCLK period is 12.5 ms. The UPEVNT period is ‘12.5 ms x 2’, where 2 is the 4-bit QCLK binary divider value. For a 16 bit QCTMR, the maximum count can be 65535. To arrive at a possible SYSCLKOUT divider value, we perform the following calculations

$$\frac{12.5\ \text{ms} * 2}{65536} \approx 380\ \text{ns}$$

$$\frac{380\ \text{ns}}{10\ \text{ns}} = 38$$

which are valid for a 100 MHz SYSCLKOUT. The value obtained in this equation would be the divider value that makes the timer count almost use up its full range. However, the only possible divider values are 2, 4, 8…, 64, and 128. So we choose the best possible value of 64. This value for the capture clock prescaler is the best possible value for this particular set of SYSCLKOUT and input frequency value.

This discussion is best suited for applications where a good estimate of the input frequency is available. For cases where a range of frequencies are possible, the divider should be configured such that the capture timer nears its maximum count for the lowest possible frequency required to be measured.

Note: The QCAPCTL register should not be modified dynamically (such as switching CAPCLK prescaling mode from SYSCLKOUT/4 to SYSCLKOUT/8). The capture unit must be disabled before changing the prescaler.

In the event of a QCTMR overflow between unit position events, the capture unit sets the eQEP overflow error flag (QEPSTS:COEF).

A unit timer base unit can be used to generate an interrupt to latch the position counter, capture timer and capture period registers and perform any calculations that might be needed to be carried out at certain time intervals.

3.4 QPOSCTL

This register can be used to enable pulse width measurement by enabling the position-compare (QPOSCTL:PCE = 1).

3.5 QPOSMAX, QPOSCMP, QEINT and QCLR

The maximum position count register (QPOSMAX) and position-compare register (QPOSCMP) need to be initialized with proper values for period and pulse width measurements, as was discussed earlier.

The interrupt control register (QEINT) is used to enable the position counter overflow interrupt and the position-compare interrupt.

The interrupt service routine needs to clear the global interrupt flag bit and the serviced event via the interrupt clear register (QCLR) before any other interrupt pulses are generated.

4 Configuring the Registers

The following is a sample code that can be used for configuring the registers so as to use the eQEP module as a capture unit.

```
EQep1Regs.QEINT.bit.PCO = 1;           // Position Counter Overflow Interrupt Enabled
EQep1Regs.QEINT.bit.PCM = 1;           // Position-Compare Interrupt Enabled

EQep1Regs.QEPCTL.bit.FREE_SOFT=2;
EQep1Regs.QEPCTL.bit.PCRM=01;          // PCRM=01 mode
EQep1Regs.QEPCTL.bit.UTE=0;            // Unit Timeout Enable
EQep1Regs.QEPCTL.bit.QCLM=0;           // Latch on unit time out

// The PCO interrupt is generated for the UPEVNT when QPOSCNT is reset from 1 to 0.
// The values for QPOSMAX and QPOSCMP are arrived at keeping in mind that the position
// counter counts 0-1-0-1-0-1... and so on

EQep1Regs.QPOSMAX=0x00000001;          // Maximum Position Count Register
EQep1Regs.QPOSCMP=0x00000000;          // Position-Compare Register

EQep1Regs.QEPCTL.bit.QPEN=1;           // QEP enable

EQep1Regs.QCAPCTL.bit.UPPS=1;          //   for UPEVNT Generation
EQep1Regs.QCAPCTL.bit.CCPS=6;          // 1/64 for CAP clock (input 40 Hz)
EQep1Regs.QCAPCTL.bit.CEN=1;           // QEP Capture Enable

EQep1Regs.QPOSCTL.bit.PCE = 1;         // Enable Position-Compare

EALLOW;                                // Enable EALLOW
GpioCtrlRegs.GPAMUX2.bit.GPIO20 = 1;   // Assuming GPIO20 is EQEP1A
GpioCtrlRegs.GPAMUX2.bit.GPIO21 = 1;   // Assuming GPIO21 is EQEP1B
GpioCtrlRegs.GPAMUX2.bit.GPIO23 = 1;   // Assuming GPIO23 is EQEP1I
EDIS;                                  // Disable EALLOW
```

5 References

- *TMS320x28xx, 28xxx Enhanced Quadrature Encoder Pulse (eQEP) Module Reference Guide* (SPRU790).

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