Application Report
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Compatibility Considerations: TMS570LS20x/10x to TMS570LS31x/21x

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ABSTRACT

This application report provides a summary of the main changes required for porting an application written on the Hercules™ TMS570LS20x/10x series of microcontrollers over to the Hercules TMS570LS31x/21x series of microcontrollers. A brief description of the process technology differences is also included.

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1 Introduction

The Hercules family of microcontrollers includes the TMS570LS series. This is a high-performance microcontroller series with features that make it easy to develop safety-critical applications.

The microcontrollers included in the TMS570LS20x/10x series are:

- TMS570LS20216
- TMS570LS20206
- TMS570LS10216
- TMS570LS10206
- TMS570LS10116
- TMS570LS10106

The microcontrollers included in the TMS570LS31x/21x series are:

- TMS570LS3137
- TMS570LS3135
- TMS570LS3134
- TMS570LS2135
- TMS570LS2134
- TMS570LS2125
- TMS570LS2124

Overall, the LS31x/21x series of microcontrollers incorporates a superset of functionalities incorporated on the LS20x/10x series of microcontrollers. The LS31x/21x series also implements significant feature enhancements and performance improvements, while still maintaining application code compatibility to the LS20x/10x series. Any application written for the LS20x/10x series runs correctly on the LS31x/21x series as well, as long as only the common functions are exercised.

The two series of microcontrollers are more diverse in terms of hardware compatibility. That is, the 144 PGE package pin-outs for the LS31x/21x series is not compatible at all to the LS20x/10x series. An application board designed for the 144 PGE LS20x/10x microcontrollers cannot be used for the LS31x/21x series without significant changes. The two series are closer to being compatible in the 337 BGA package – there are some important differences which are discussed in this document as well.

2 Device-Level Feature Differences

Table 1 summarizes the high-level feature differences between the superset microcontrollers of the LS20x and LS31x series.

Table 1. High-Level Differences: TMS570LS20216 v/s TMS570LS3137

Feature	TMS570LS20216 337 BGA	TMS570LS20216 144 QFP	TMS570LS3137 337 BGA	TMS570LS3137 144 QFP
Technology Node	F035, 130 nm		F021, 65 nm	
Maximum CPU Frequency	160 MHz	140 MHz	180 MHz	160 MHz
Maximum Frequency for Single-Cycle Read from Flash	36 MHz		45 MHz	
CPU Program Memory: Flash	2MB		3MB	
Flash for Emulated EEPROM	Not Supported		64KB	
CPU Data Memory: RAM	128KB		256KB	
Nominal Supply Voltages	3.3 V I/O, 3.3 V Flash Pump, 1.8 V Core, 3.3 V ADC		3.3 V I/O, 3.3 V Flash Pump, 1.2 V Core, 3.3 V or 5 V ADC	
Memory Protection Unit	8 regions		12 regions	
Code Security	Not Supported		Advanced JTAG Security Module (AJSM)	
Watchdog Timer	Not Supported		Digital Windowed Watchdog	
Dual-Clock Comparator (DCC)	Not Supported		Two DCC Modules	
External Memory Interface (EMIF)	Asynchronous Memories only	Not Supported	Asynchronous Memories and Synchronous DRAM (SDRAM)	Not Supported
Enhanced High-End Timer (NHET)	Single NHET Module: 32 channels	Single NHET Module: 20 channels	Two N2HET Modules: 44 channels	Two N2HET Modules: 40 channels
Multi-buffered ADC (MibADC)	Two 12-bit ADC Cores with 24 Total Channels	Two 12-bit ADC Cores with 20 Total Channels	Two 12-bit ADC Cores with 24 Total Channels	Two 12-bit ADC Cores with 24 Total Channels
Analog Input Channels Shared Between Two ADCs	8	8	16	16
Interrupt-Capable General-Purpose I/Os (GIO)	16	8	16	4
FlexRay Controller	2-channel	2-channel	2-channel	2-channel
Controller Area Network (CAN) Interface Controllers	3	2	3	3
Local Interconnect Network (LIN) Interface Controllers	2, compliant to LIN v2.0	2, compliant to LIN v2.0	1, compliant to LIN v2.1	1, compliant to LIN v2.1
Standard Serial Communication Interface Controller	0	0	1	1
Multi-buffered Serial Peripheral Interface (MibSPI) Controller	3	3	3	3
Standard Serial Peripheral Interface (SPI) Controller	0	0	2	2
Inter-Integrated-Circuit (I2C) Controller	0	0	1	1
Ethernet: Media Independent Interface (MII)/ Reduced Media Independent Interface (RMII)	0	0	10/100 Mbps	10/100 Mbps

3 Module-Level Feature Differences

The following sections highlight the significant module-level enhancements/differences on the TMS570LS31x/21x series of microcontrollers.

3.1 12-bit Analog-to-Digital Converter (ADC)

The main enhancements to the ADC digital interface module of LS31x/21x as compared to LS20x/10x are:

- 10/12-bit mode allows application to configure the module as a true 10-bit converter (10 cycles for conversion)
- Low-power mode allows the ADC to automatically enter power-saving mode when no conversions are pending
- Event triggering allows the use of both rising and falling edges of selected event to trigger conversions
- DMA support allows the application to generate DMA request on "group conversion end"
- Results RAM allows the application to not reset the result memory for a conversion group when new channel selection is made for that group

3.2 Core Compare Module (CCM-R4)

The two CPUs on the LS31x/21x microcontrollers are 2 GCLK cycles out of phase. The two CPUs are 1.5 GCLK cycles out of phase on the LS20x/10x series. This is completely transparent to the application software or hardware designer.

3.3 External Memory Interface (EMIF)

The EMIF on LS31x/21x allows interfacing to asynchronous memories and an external SDRAM module. The EMIF on LS20x/10x only allowed interfacing to external asynchronous memories.

3.4 Error Signaling Module (ESM)

The ESM module on the LS31x/21x microcontrollers can now support up to 64 channels for group1 error conditions. This is functionally compatible and enhanced compared to the ESM module on LS20x/10x microcontrollers which only supported 32 channels for group1 error conditions.

3.5 Global Clock Module (GCM)

Main enhancements to the GCM on the LS31x/21x as compared to the LS20x/10x are:

- Support for additional clock domains: VCLK3, AVCLK3, and AVCLK4. The application needs to configure the clock source selection for these clock domains if the associated functionality is being used in the application. To identify the functions that use these new clock domains, check the device-specific datasheet and TRM.
- Ability to observe the PLL output clock on ECLK while the PLL is still acquiring lock to the reference clock

3.6 Local Interconnect Network Controller (LIN)

The LIN controller module on the LS31x/21x microcontrollers is enhanced to support conformance to LIN specification version 2.1, which is backwards compatible to the LIN protocol specification version 2.0. The LIN module on LS20x/10x microcontrollers is conformant to LIN specification version 2.0.

3.7 Low-Power Oscillator / Clock Detector (LPOCLKDET)

The main enhancements to the LPOCLKDET module of the LS31x/21x as compared to the LS20x/10x are:

- Trim settings for HF LPO and LF LPO increased from a 4-bit value to a 5-bit value, offering greater granularity for controlling the LPO output frequencies
- Improved availability; added ability to restart the main oscillator whenever an oscillator failure is detected

- Improved availability; added ability to restart the PLL whenever a PLL slip is detected

3.8 Multi-buffered Serial Peripheral Interface (MibSPI)

The main enhancements to the MibSPI module of the LS31x/21x as compared to the LS20x/10x are:

- Support for half-duplex mode allows the application to use a TX-only or RX-only SPI communication
- Increased the SPICLK prescaler width from 8 bits to 11 bits allows wider range of SPICLK frequencies for a given peripheral clock frequency.
- Increased the WDELAY parameter width from 6 bits to 8 bits allows configuration of longer delay between successive transfers.

3.9 High-End Timer (N2HET)

The high-end timer module on the LS31x/21x microcontrollers has undergone a design update while still maintaining backwards compatibility to the NHET module design implemented on the LS20x/10x microcontrollers. The most significant enhancements implemented on the N2HET on the LS31x/21x are:

- Added eight new instructions:
  - ADD — Add
  - ADC — Add with Carry
  - AND — Bitwise AND
  - OR — Bitwise OR
  - SUB — Subtract
  - SBB — Subtract with Borrow
  - XOR — Bitwise XOR
  - RCNT — Ratio Count
- Added three new condition flags:
  - C — Carry flag
  - N — Negative flag
  - V — Overflow flag
- Added two new general-purpose 32-bit registers: R and S
- Integrated hardware angle generator allows the application to generate angle values based on a toothed-wheel input
- Enhanced input edge detection scheme allows for input pulse widths smaller than 1 loop-resolution period
- Added hi-res or loop-res option for the PCNT instruction, which allows the application to choose the resolution for the measurement
- AND-shared outputs allows the application to output a logical AND'ed output of two adjacent channels, typically required for sound generation

3.10 Parameter Overlay Module (POM)

The main enhancements to the POM module of the LS31x/21x as compared to the LS20x/10x are:

- Added ability to overlay on to internal RAM
- Added time-out feature to prevent a device hang situation in case of a bus stuck error condition

3.11 Real-Time Interrupt Module (RTI)

The main enhancements to the RTI module are:

- Ability to automatically clear compare interrupt signals, which is useful when RTI compare interrupts are used to periodically trigger a system event, e.g., ADC conversions
- Added digital windowed watchdog functionality, which allows the application to protect against stray code execution.

3.12 CPU Self-Test Controller (STC)

The main enhancements to the STC module of the LS31x/21x as compared to the LS20x/10x are:

- Added the ability to check the STC comparator logic itself before enabling the CPU self-test
- Optimized the CPU self-test patterns to get a higher coverage for a given number of test intervals
- LS31x/21x requires 24 test intervals (32768 cycles total) to get CPU coverage > 90%; LS20x/10x required 32 test intervals (49698 cycles total)
- CPU self-test can be run at CPU clock speeds up to 90 MHz on LS31x/21x; this was limited to 53.33 MHz on LS20x/10x.

3.13 System Module (SYS)

The main enhancements to the SYS module of the LS31x/21x as compared to the LS20x/10x are:

- Added control to select between main oscillator and VCLK as input to the external clock prescaler (ECP)
- Enhanced clock test mode that allows all clock sources and domains to be brought out on device terminals for debug purposes

4 Package Differences

Both the TMS570LS20x/10x and the TMS570LS31x/21x series of microcontrollers are offered in two packages:

- 144-pin quad flat pack (QFP)
- 337-ball grid array (BGA)

The following sections describe the differences in terms of the pin-out and ball-out for these two packages.

4.1 144 QFP Differences

The LS20x/10x and LS31x/21x microcontrollers are completely different in terms of the 144 QFP pin-out. An application that uses the LS20x/10x microcontroller in the 144 QFP package cannot use the LS31x/21x microcontrollers without redesigning the circuit board.

4.2 337 BGA Differences

The LS20x/10x and LS31x/21x microcontrollers are very compatible in terms of the 337 BGA ball-outs with some significant exceptions. These exceptions are summarized in Table 2 and described in the sections following the table.

Table 2. LS31x/21x and LS20x/10x Ball-Map Differences

Signal Name	337 BGA Ball# for LS20x/10x	337 BGA Ball# for LS31x/21x
External Memory Interface (EMIF) Differences		
EMIF_BA[0]	D13	E13
EMIF_nOE	D12	E12
EMIF_nDQM[1]	D11	E11
EMIF_nDQM[0]	D10	E10
EMIF_ADDR[5]	D9	E9
EMIF_ADDR[4]	D8	E8
EMIF_ADDR[3]	D7	E7
EMIF_ADDR[2]	D6	E6
EMIF_DATA[4]	E4	E5
EMIF_DATA[5]	F4	F5
EMIF_DATA[6]	G4	G5
EMIF_DATA[7]	K4	K5
EMIF_CLK	–	K3
EMIF_DATA[8]	L4	L5
EMIF_CKE	–	L3
EMIF_DATA[9]	M4	M5
EMIF_DATA[10]	N4	N5
EMIF_DATA[11]	P4	P5
EMIF_nWAIT	–	P3
EMIF_nRAS	–	R3
EMIF_nCAS	–	R4
EMIF_DATA[12]	T5	R5
EMIF_DATA[13]	T6	R6
EMIF_DATA[14]	T7	R7
EMIF_DATA[15]	T8	R8
EMIF_DATA[3]	N16	N15
EMIF_DATA[2]	M16	M15
EMIF_DATA[1]	L16	L15
EMIF_DATA[0]	K16	K15

Table 2. LS31x/21x and LS20x/10x Ball-Map Differences (continued)

Signal Name	337 BGA Ball# for LS20x/10x	337 BGA Ball# for LS31x/21x
EMIF_nCS[5] (asynchronous chip select)	N17	–
EMIF_nCS[0] (SDRAM chip select)	–	N17
RAM Trace Port (RTP) Differences		
RTPDATA[0]	V11	NC
RTPDATA[1]	U11	NC
RTPDATA[2]	T10	NC
RTPDATA[3]	U10	NC
RTPDATA[4]	T9	NC
RTPDATA[5]	U9	NC
RTPDATA[6]	U8	NC
RTPDATA[7]	U7	NC
RTPDATA[8]	U6	NC
RTPDATA[9]	U5	NC
RTPDATA[10]	U4	NC
RTPDATA[11]	T4	NC
RTPDATA[12]	V3	NC
RTPDATA[13]	U3	NC
RTPDATA[14]	T3	NC
RTPDATA[15]	T2	NC
RTPnENA	U12	NC
RTPSYNC	T11	NC
RTPCLK	W11	NC
Local Interconnect Network (LIN) Interface Differences		
LIN1 TX	V12	NC
LIN1 RX	W12	NC
LIN2 TX	B7	B7
LIN2 RX	A7	A7
Important Note: The control and status registers for the LIN module on LS31x/21x are mapped to the same location as the LIN1 module on LS20x/10x.		
Standard Serial Peripheral Interface (SPI2) Differences		
SPI2 CLK	NC	E2
SPI2 SIMO	NC	D1
SPI2 SOMI	NC	D2
SPI2 nCS[0]	NC	N3
SPI2 nENA	NC	D3

4.2.1 External Memory Interface (EMIF)

The EMIF on LS31x/21x supports interfacing to an external SDRAM in addition to asynchronous memories. Therefore, the EMIF on the LS31x/21x microcontrollers has additional signals to interface to an external SDRAM.

Also, some EMIF signals are multiplexed with Embedded Trace Macrocell (ETM) signals on the LS31x/21x microcontrollers. As a result, the full EMIF port is not available at the same time as the full ETM port. The LS20x/10x microcontrollers has no multiplexing between EMIF/ETM signals. This causes an incompatibility in the ball mapping for the EMIF signals between LS31x/21x and LS20x/10x.

4.2.2 RAM Trace Port (RTP)

The RTP signals on LS31x/21x microcontrollers are all multiplexed with ETM signals are not available independently. Therefore, there is no compatibility between the mapping of RTP signals on the 337 BGA ball-maps of LS31x/21x and LS20x/10x microcontrollers. However, the balls that carry the RTP signals on LS20x/10x are left as *no connects* on LS31x/21x. RTP is typically not used when the application is running and is only used during application debug. Keeping this in mind, this incompatibility only affects the ability to debug using the RTP on both LS31x/21x and LS20x/10x using a common circuit board.

4.2.3 Local Interconnect Network (LIN)

There are two LIN modules on LS20x/10x while there is only one LIN module on the LS31x/21x microcontrollers. The balls for the LIN TX and RX signals on LS31x/21x are the same as those for the LIN2 TX and LIN2 RX signals on LS20x/10x.

Also note that the base address of the LIN module on the LS31x/21x is the same as that of the LIN1 module on the LS20x/10x microcontrollers.

4.2.4 Standard Serial Peripheral Interface 2 (SPI2)

The LS31x/21x include a standard SPI module in addition to the three multi-buffered SPI modules: MibSPI1, MibSPI3, MibSPI5. The LS20x/10x does not have a standard SPI module, and the corresponding balls are left unconnected on these microcontrollers.

4.2.5 Analog-to-Digital Converter (ADC)

The LS20x/10x and LS31x/21x microcontrollers both contain two instances of the 12-bit analog-to-digital converter (ADC) modules. There are 8 analog input channels shared between ADC1 and ADC2 on the LS20x/10x while there are 16 analog input channels shared between ADC1 and ADC2 on the LS31x/21x microcontrollers. The additional shared channels are listed below.

- Ball R16, AD2IN[7] is also shared with AD1IN[23]
- Ball R19, AD2IN[6] is also shared with AD1IN[22]
- Ball T15, AD2IN[5] is also shared with AD1IN[21]
- Ball U15, AD2IN[4] is also shared with AD1IN[20]
- Ball U16, AD2IN[3] is also shared with AD1IN[19]
- Ball U14, AD2IN[2] is also shared with AD1IN[18]
- Ball U13, AD2IN[1] is also shared with AD1IN[17]
- Ball V13, AD2IN[0] is also shared with AD1IN[16]

The LS20x/10x microcontrollers also have a dedicated ball, W13, for the AD2EVT signal. This signal is multiplexed with some other functions on the LS31x/21x microcontrollers and is available on ball V10.

5 Analog IP Differences

The following sections highlight the significant differences in the analog IP between the LS20x/10x and LS31x/21x microcontrollers.

5.1 Flash Bank and Pump

The most significant changes to the Flash pump and Flash bank are listed below. These have no impact to the application software or hardware development.

- The Flash pump on the LS31x/21x allows up to 144 bits to be programmed simultaneously versus 32 on LS20x/10x, which allows faster programming of Flash.
- The Flash pump on LS31x/21x implements a glitch filter on the power-on reset signal, which has a minimum filter time of 500 ns versus 35 ns on LS20x/10x.
- The Flash bank on LS31x/21x supports a maximum CPU clock frequency of 45 MHz for a single-cycle Flash read access; this was limited to 36 MHz on LS20x/10x.

5.2 Phase-Locked-Loops (PLL1, PLL2)

The LS31x/21x as well as the LS20x/10x microcontrollers contain two separate PLL instances: PLL1 and PLL2. Figure 1 and Figure 2 show high-level block diagrams for the PLLs on LS20x/10x and LS31x/21x microcontrollers.

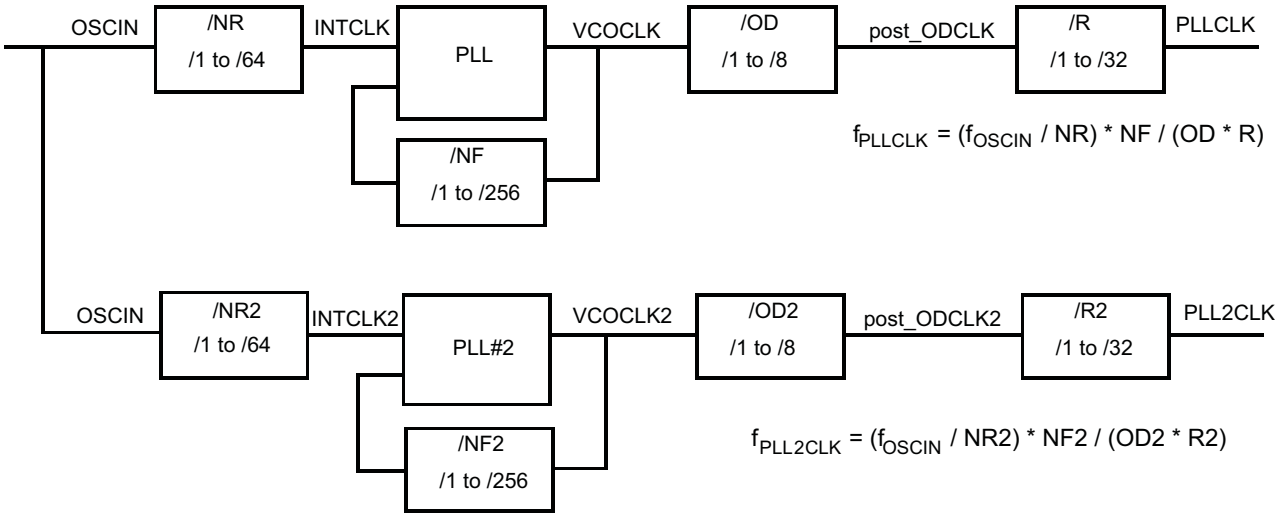

Figure 1. PLLs on TMS570LS31x/21x

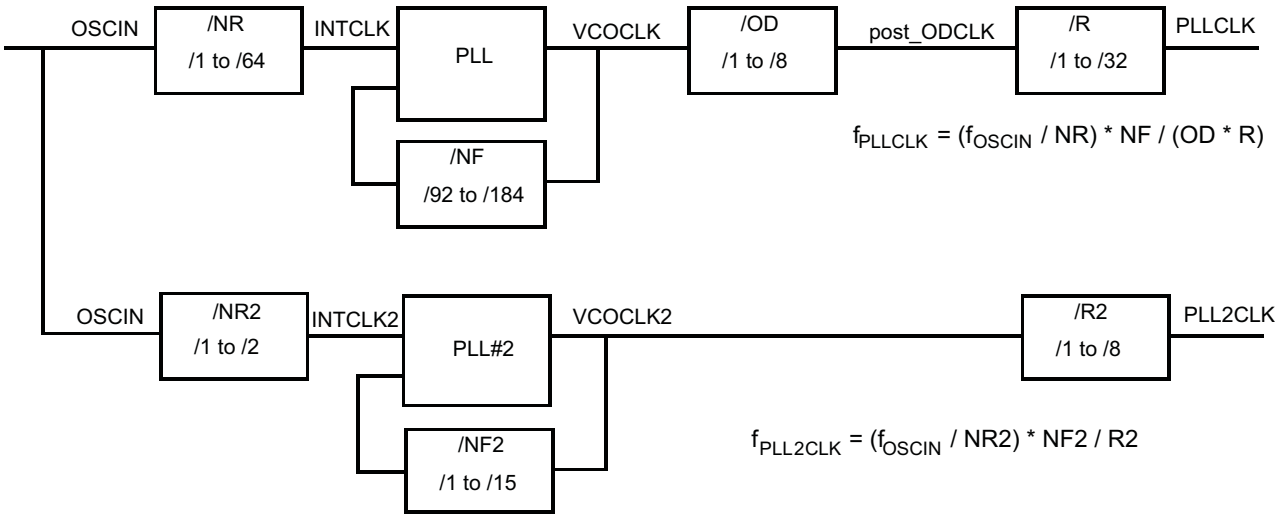

Figure 2. PLLs on TMS570LS20x/10x

There are significant differences in the values of the multipliers and dividers that determine the PLL output frequency between the LS20x/10x and LS31x/21x microcontrollers, as shown in Figure 1 and Figure 2. It is still important to note that any PLL control register setting used on the LS20x/10x microcontrollers can be used as-is on the LS31x/21x as long as frequency modulation is not enabled.

The other differences between the PLLs on LS20x/10x and LS31x/21x microcontrollers are now summarized.

- The PLL1 on LS20x/10x can be powered with the spread-spectrum mode enabled; the SS mode must only be enabled after the FMzPLL powers up on LS31x/21x.
- The PLL1 power-up time for LS20x/10x is 4639 INTCLK cycles; this time is 1024 INTCLK cycles + 134 OSCIN cycles on LS31x/21x.
- The PLL2 power-up time for LS20x/10x is 30 µs regardless of the input clock frequencies; this time is 1024 INTCLK2 cycles + 134 OSCIN cycles on LS31x/21x.
- The INTCLK frequency on LS20x/10x is limited to the range 1.63 MHz to 6.53 MHz; this range is 430 kHz to 100 MHz on LS31x/21x.
- The INTCLK2 frequency on LS20x/10x is required to be in the range 10 MHz to 100 MHz; this range is 430 kHz to 100 MHz on LS31x/21x.
- The VCOCLK frequency on LS20x/10x is limited to the range 120 MHz to 500 MHz; this range is 110 MHz to 550 MHz on LS31x/21x.
- The VCOCLK2 frequency on LS20x/10x is required to be in the range 10 MHz to 250 MHz; this range is 110 MHz to 550 MHz on LS31x/21x.
- The post_ODCLK frequency on LS20x/10x is limited to the range 120 MHz to 160 MHz; this range is 110 MHz to 400 MHz on LS31x/21x for both post_ODCLK and post_ODCLK2.
- The PLLCLK frequency on LS20x/10x is limited to a max of 160 MHz; this value is 180 MHz on LS31x/31x.
- The PLL2CLK frequency on LS20x/10x is limited to a max of 160 MHz; this value is 180 MHz on LS31x/21x.
- The PLL1 slip on LS20x/10x cannot be filtered; the LS31x/21x has a 6-bit programmable slip filter that runs on HF LPO.
- Once a PLL1 slip is indicated on LS20x/10x, the PLL1 output clock cannot be used for any clock domain. On the LS31x/21x, the application has an option to try and restart the PLL so that the application can resume using the PLL output for any clock domain.

5.3 Low-Power Oscillator and Clock Monitor (LPOCLKDET)

The low-power oscillator (LPO) provides two separate clock sources: LF LPO and HF LPO, to be used for any given device clock domain. These form clock source numbers 4 and 5 for the global clock module (GCM). The HF LPO is also used by the clock monitor circuit to detect the availability of the main oscillator as well as provide a gross check on the frequency of the main oscillator. There are some basic differences between the implementations of the LPOCLKDET macro between the LS20x/10x and LS31x/21x microcontrollers. These do not affect the application software or hardware development.

- The LPO on LS20x/10x only requires the core supply (1.5 V nominal) for operation; the LPO on LS31x/21x requires both the core supply (1.2 V nominal) and the I/O supply (3.3 V nominal) for operation.
- The maximum cold start-up time for the LPO on LS20x/10x is 500 µs; this time is 900 µs on LS31x/21x.
- The untrimmed HF LPO frequency ranges from 6.6 MHz to 17.4 MHz on LS20x/10x; this range is 5.5 MHz to 19.5 MHz on LS31x/21x.
- The untrimmed LF LPO frequency ranges from 55 kHz to 145 kHz on LS20x/10x; this range is 19 kHz to 270 kHz on LS31x/21x.
- There are 16 HF LPO and LF LPO trim settings available on LS20x/10x; there are 32 trim settings on LS31x/21x.
- Each trim setting affects the frequency by 6.25% on LS20x/10x; this value is 4% on LS31x/21x.

5.4 Oscillator

The oscillator on LS31x/21x is improved versus the oscillator on LS20x/10x in terms of noise immunity. This has no impact on the application software development. The application hardware designed for LS20x/10x can be reused with the LS31x/21x with the oscillator changed to be able to handle 3.3 V CMOS levels. The following changes lead to the improvement in noise immunity:

- Oscillator buffer is a 3.3 V buffer on LS31x/21x versus 1.5 V on LS20x/10x
- An RC-filter is added on the oscillator input signal path to eliminate high-frequency noise

5.5 I/O Buffers

The I/O buffers on LS31x/21x are designed to be compatible to those on LS20x/10x in terms of the output rise/fall times, input and output signal transition levels, input hysterisis levels, input clamp current, input leakage current, pull up/down currents, as well as the ESD characteristics. There are other significant improvements made to the I/O buffers on the LS31x/21x microcontrollers. These are:

- Adaptive impedance-controlled output mode allows the core noise to be decoupled from the I/O pad
- Available pull up/down when power-on reset is active; the pulls are disabled when power-on reset is asserted on LS20x/10x
- RC-filter on the input signal path to eliminate high-frequency noise

5.6 Internal Voltage Monitor (VMON)

The internal voltage monitoring thresholds for the core supply are different to account for the reduced core supply range. To identify the actual difference in the values of the voltage monitoring thresholds, see the device-specific datasheet.

5.7 Glitch Filters

There are glitch filters implemented on the power-on reset ($\overline{\text{PORRST}}$), warm reset ($\overline{\text{RST}}$) and test reset ($\overline{\text{TRST}}$) signals on both the LS31x/21x as well as the LS20x/10x microcontrollers. The glitch filtering capability is significantly different as shown in Table 3.

Table 3. Glitch Filter Differences

Parameter	LS20x/10x		LS31x/21x	
	MIN	MAX	MIN	MAX
$\overline{\text{PORRST}}$ low-pulse-width glitch filter	30 ns	150 ns	500 ns	2 µs
$\overline{\text{RST}}$ low-pulse-width glitch filter	30 ns	150 ns	500 ns	2 µs
$\overline{\text{TRST}}$ low-pulse-width glitch filter	30 ns	150 ns	500 ns	2 µs

Input with a low pulse-width smaller than the *minimum* value specified will not pass through the glitch filter.

Input with a low pulse-width larger than the *maximum* value specified will definitely pass through the glitch filter.

The application designer must ensure that any reset provided to the LS31x/21x microcontroller asserts the reset ($\overline{\text{PORRST}}$, $\overline{\text{RST}}$, $\overline{\text{TRST}}$) signal for at least the duration specified by the max value of the glitch filter width, that is, 2 µs.

5.8 Analog-to-Digital Converter (ADC)

The main enhancements on the ADC macro on LS31x/21x microcontrollers are:

- Configurable 10-bit or 12-bit modes of operation
- Operating voltage range from 3.0 V to 5.25 V
- Minimum sample time reduced from 1µs to 200 ns
- Maximum ADC input switch on-resistance reduced from 1500Ω to 250Ω
- Maximum ADC sample switch on-resistance reduced from 1500Ω to 250Ω
- Maximum ADC sample capacitance increased from 8 pF to 12 pF

The ADC module on the LS31x/21x is configured to be in the 10-bit conversion mode by default. In order to switch the ADC to be in the 12-bit conversion mode (as on LS20x/10x), the application must set the *10/12-BIT* field of the ADC Operating Mode Control Register (ADOPMODECR, bit 31). For further details, see the device-specific technical reference manual.

6 Other New Features on TMS570LS31x/21x

There are some features added on the LS31x/21x microcontrollers that were not available on the LS20x/10x.

- I/O multiplexing module that allows the application to select between multiplexed functions for each terminal
- Power management module that allows the application to disable unused core logic to reduce the leakage current

7 References

- *TMS570LS3137 16/32-Bit Risc Flash Microcontroller Data Sheet* (SPNS162)
- *TMS570LSxxx5 16/32-Bit Risc Flash Microcontroller Data Sheet* (SPNS164)
- *TMS570LSxxx4 16/32-Bit Risc Flash Microcontroller Data Sheet* (SPNS165)
- *RM48L952 16/32-Bit Risc Flash Microcontroller Data Sheet* (SPNS176)
- *RM48Lx50 16/32-Bit Risc Flash Microcontroller Data Sheet* (SPNS174)
- *RM48Lx40 16/32-Bit Risc Flash Microcontroller Data Sheet* (SPNS175)
- *RM48Lx30 16/32-Bit Risc Flash Microcontroller Data Sheet* (SPNS176)
- *TMS570LS31/21 16/32-Bit RISC Flash Microcontroller Technical Reference Manual* (SPNU499)
- *RM48 16/32-Bit RISC Flash Microcontroller Technical Reference Manual* (SPNU503)

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