Interfacing External Devices to the TPA310xDx Amplifiers

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ABSTRACT

The TPA3100D2, TPA3101D2, TPA3106D1, and TPA3107D2 audio power amplifiers have four gain settings that are controlled by logic pins that are designed to be switched between ground and the voltage regulator internal to the device.

Additionally, the MUTE pin is referenced to the internal voltage regulator, and the use of an interfacing transistor should also be considered.

This Application Brief describes the best practice for interfacing and external logic source (i.e.: a microcontroller) to the TPA310xDx family.

Considerations

When the TPA310xDx is placed in shutdown, the internal voltage regulator (VREG) is powered off to conserve power.

If GAIN0, GAIN1, and/or MUTE functions are driven by an external source that continues to apply voltage to any of these 3 pins during device shutdown, it can inhibit the start up sequence of the internal state machine, and VREG will not be operational; therefore, the amplifier will not pass a signal.

Since $\overline{\text{SHUTDOWN}}$ is an active low, it does not need an external MOSFET to be buffered.

Theory of Operation

Simple MOSFET transistor inverters are suggested to drive the gain pins when it is necessary to change the amplifier's gain or mute from an external source. A MOSFET is suggested because it consumes less power. This circuit is illustrated in Figure 1. A bias junction transistor (BJT) could be considered; however, care must be taken because the ratio of the collector current to the base current can create issues. This can occur because the value of the collector resistor must be kept in the range of 100K so that excessive current is not drawn from the voltage reference inside of the TPA310xDx family.

The drain of the MOSFET (NFET1) is connected through a 100kΩ resistor (R2) to VREG and the junction of the drain and the 100kΩ resistor is connected to the GAIN1 pin, for example.

A 100kΩ resistor (R1) is also connected to the gate of the MOSFET to limit current in the event an error condition should arise. The other end of the gate resistor is connected to external device (i.e.: microcontroller).

This circuit provides the logic inverse; therefore, to set GAIN1 to a logic high, a logic low must be applied to R1.

Since this circuit is powered from VREG, it will shutdown with VREG and eliminate the issue.

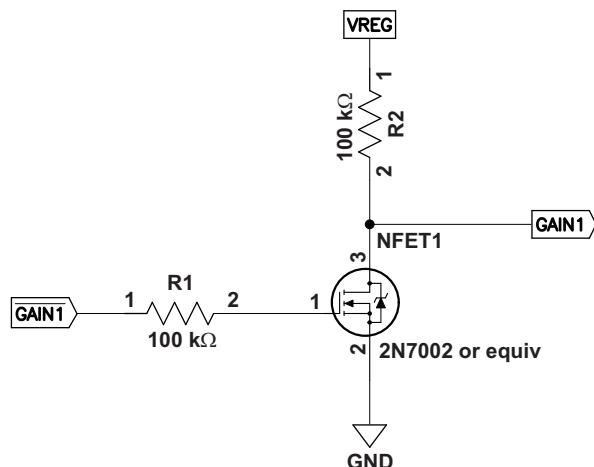Figure 2 shows three of the circuits as they would be connected to a control device (microcontroller).
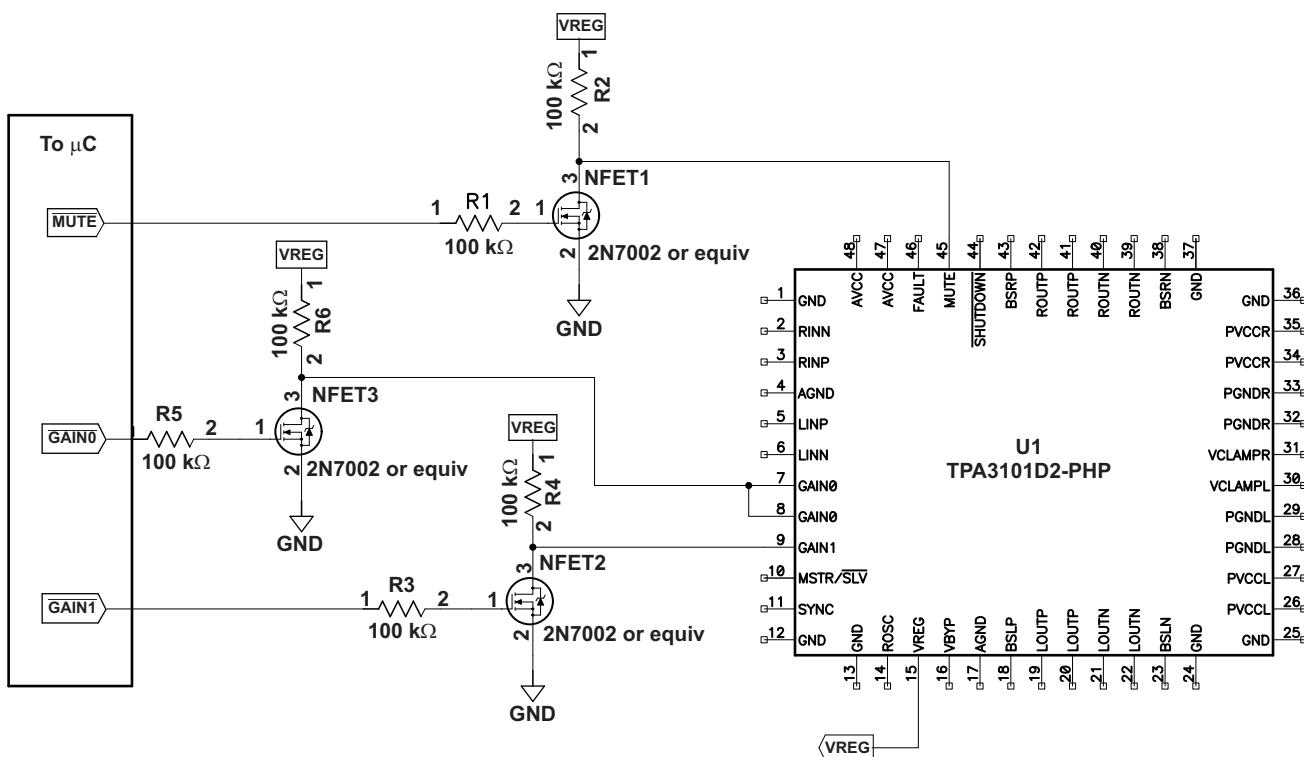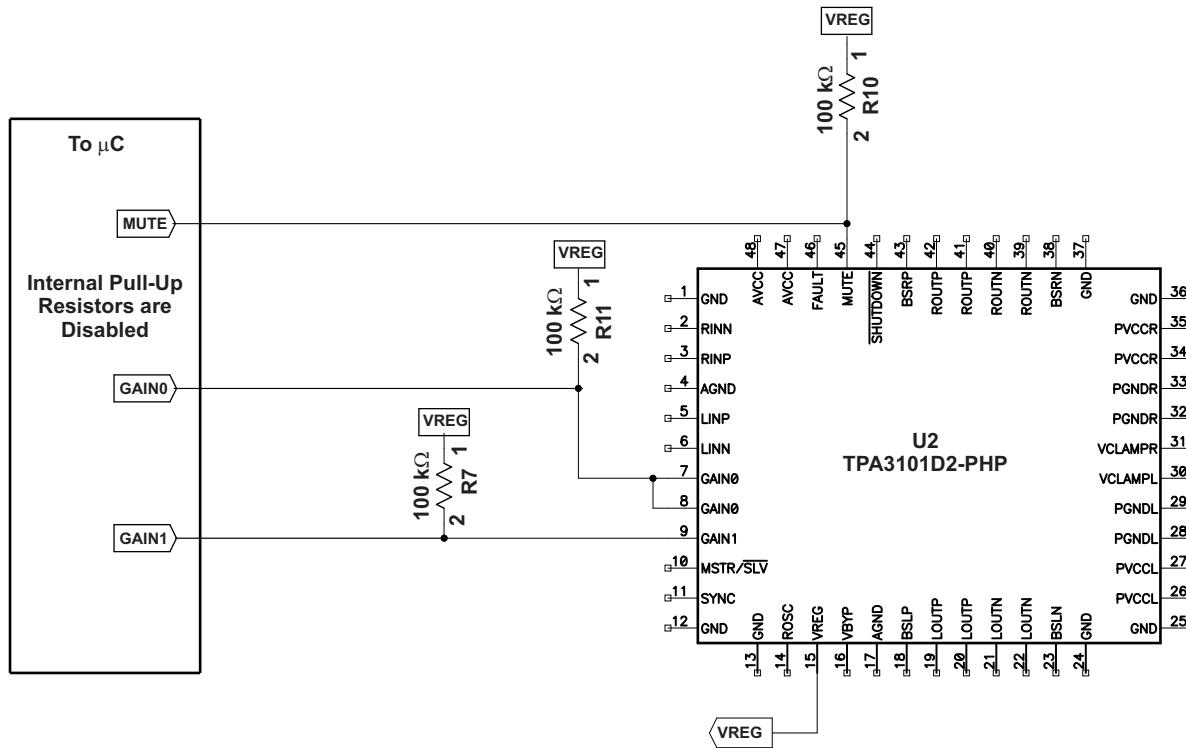
Figure 1. Basic Circuit Diagram

Figure 2. Connection to Amplifier (All Three Circuits Shown)

Alternate Method Number 1

Some microcontrollers have the capability to turn off or disable the internal pull up resistors on the GPIO pins. If this is the case, the system designer can disable the pull up resistors on the pins that is connected to the TPA310xDx, and pull the pins up to VREG with 100kΩ resistors. This should eliminate the possibility of providing an extraneous bias to the device. Figure 3 illustrates the connection of the TPA310xDx family to a microcontroller having the capability of disabling the internal pull-up resistors on its GPIO port.

Figure 3. Alternate Method Number 1 – Circuit Diagram

Alternate Method Number 2

Finally, if the microcontroller can not disable its GPIO pull up resistors, then set all logic inputs to the TPA310x to a logic low, set $\overline{\text{SHUTDOWN}}$ to a logic high, allow the part to come out of its shutdown (low power state), and then set the required gain and mute conditions.

In this method, pull up resistors to VREG are not required.

IMPORTANT NOTICE