Choosing Simulation Models for ESD Devices

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Electrostatic discharge (ESD) protection diodes are unique when it comes to simulations of systems. They are suppose to be invisible during normal operation and shunt current during an ESD event. This means that for running normal behavior of a system, the designer would only care if the ESD diode is affecting the signal trying to be passed. However, sometimes designers want to model the transient behavior of ESD diodes to see if their system will survive ESD events. These transients that are normally used are described in IEC61000-4-X. Therefore, to make this process simpler this document will go through the several key model types and how they relate with ESD diodes.

Model	Purpose with Respect to ESD
IBIS	Connectivity, Drive Strength Clamping
Spice	Transient Clamping of Active FETs
S-parameter	RF & Eye Diagram
SEED	ESD Protection Level

IBIS Models

I/O-buffer-information-specification, or IBIS, models are great for many integrated circuits (ICs) that just need to model the inputs and the outputs of the device quickly. In general, they can be thought of as outputs for a given set of inputs that has actually been measured in the lab. This means it is great when a quick simulation is needed but is limited because it does not actually model the response of the internal circuitry. This is problematic for ESD diodes because the information used in the IBIS model is the RLC parasitics and the DC IV curve of the central clamp. This means its response to a transient event will not be accurate as it is basing that response from a DC stimulation.

IBIS models are great for quick simulations of complex IC's, but when it comes to ESD strikes, the complete transient nature of each device needs to be addressed. Therefore it is not recommended to use IBIS modeling when trying to simulate systems with respect to ESD.

Spice Models

Simulation Program with Integrated Circuit Emphasis, or Spice, models are transistor level models. These models get down into the device itself to model the internal schematic to produce a model that very accurately represents the circuitry inside. For devices such as TI's Flat-Clamp family, this type of modeling allows the user to simulate the transient behavior of the internal FET. These models can be found on each of the Flat-Clamp Family's product folder under the Tools and Software page. This type of model can be useful but takes a long time to simulate for an entire system. In relation to ESD diodes, Spice models are overkill for what is useful for checking if the diode works in the system. As was stated earlier the primary goal of an ESD diode is to be invisible during normal operation and conduct current during a transient event. Adding extra complexity in the system simulation is not ideal especially with the next two model's simplicity.

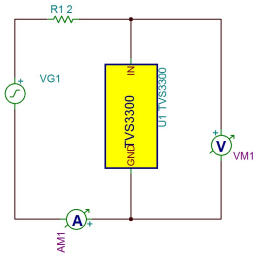

Figure 1. TVS3300 Spice Model

S-parameter Models

Scattering parameter models, or S-parameter, are, in relationship to ESD diodes, used to show that the diode is invisible during normal operation. The S-parameters relates the voltage waves incident on the ports to those reflected from the ports. These models are generated by applying a stimuli to the device across a wide frequency range. While these models do not show DC behavior or show the breakdown of the ESD diode, they are critical in simulating the signal being used in the system. For most ESD diodes the big key parameter that can be taken from the S-parameter is the insertion loss.

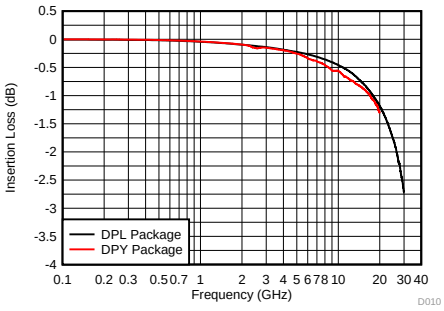

Figure 2. Insertion Loss of TPD1E0B04

The insertion loss shows the extra loss coming from the device itself between the two reference points. The S-parameter model of the ESD diode can be added together with the S-parameter model of the IC it is connected to, to show the total insertion loss for the signal. Depending on what communication protocol is used, different levels of insertion loss are acceptable. Check with the protocol standard to see what is the maximum insertion loss allowed at the frequency of the data being sent.

SEED (System Efficient ESD Design)

System Efficient ESD Design (SEED) uses the ESD diodes TLP graph added with the down stream IC's TLP graph to show the total level of protection. The TLP graph is the most useful device when trying to determine if an ESD diode can protect an IC or not. While not technically a model type, the TLP graph will allow simulations to be done instantly if both the ESD's and downstream IC's TLP curve is known. The TLP pulse is a short 100ns pulse with a 10ns rise time that closely represents the second peak of the IEC61000-4-2 ESD pulse as shown in Figure 3. When the 30ns clamping voltage is plotted together with the current level at 30ns, these pulses make an IV curve that can show the clamping voltage of an ESD diode during an increasing ESD strike.

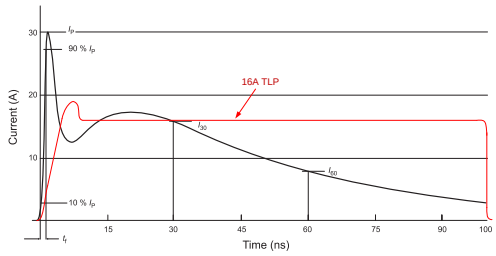

Figure 3. TLP vs. IEC61000-4-2 ESD Pulse

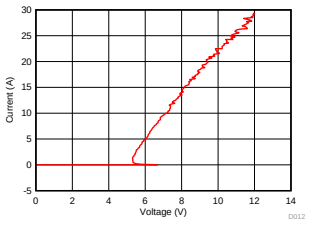

Figure 4. TLP Curve for TPD1E04U04

The TLP curve of TPD1E04U04 can be seen in Figure 4. Also from Figure 3 it can be seen that 2A TLP is equivalent to 1kV ESD. Therefore, for TPD1E04U04 at 8kV ESD (16A TLP), the clamping voltage is ~9V.

All IC's have some internal ESD protection and therefore can have TLP run on them. Obviously their internal protection will be very small in comparison to a discrete diode which is why if you add the two currents at a given voltage for the TLP curves together, you can see the total level of protection. This is shown in Figure 5.

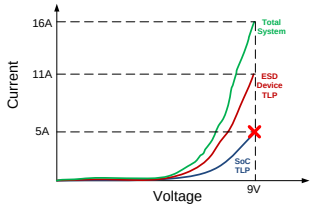

Figure 5. Total Level of Protection

In conclusion, there are several different types of models designers use when trying to simulate their system. However, when trying to simulate ESD events in total system, the most effect use is to have the TLP curve of the ESD diode which is provided in the datasheet, and the TLP of the downstream IC. Likewise, when trying to simulate signal integrity, an S-parameter model should be used to ensure the ESD diode does not interfere with normal operation. In thinking about system level solutions, with every new ESD device released, TI is releasing the S-parameter model and the TLP curve to provide the most useful and efficient information to customers.

Table 1. Alternative Device Recommendations

Device	Optimized Parameters	Performance Trade-Off
TPD1E01B04	High Bandwidth 1-Channel ESD Diode	Higher Clamping Voltage
TPD1E04U04	Low Clamping 1-Channel ESD Diode	Higher Capacitance
ESD224	Ultra Low Clamping 4-Channel ESD Diode	Higher Capacitance, Trace Discontinuity
TVS3300	Flat-Clamp TVS Diode	Slew Rate Control on Input

1 Related Documentation

- ESD Essentials
- ESD By Interface
- System-Level ESD Protection Guide

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