Application Report

SLLA305–May 2010

Reading and Understanding an ESD Protection Datasheet

Wolfgang Kemper

High Volume Analog

ABSTRACT

System engineers must choose all components for their designs carefully. Picking the right ESD protection elements can be challenging as the matter of protecting devices on the PCB against ESD stress has become an increasingly complex task.

Texas Instruments offers a wide range of ESD protection elements. Understanding the datasheet parameters of ESD protection elements is paramount to the task of selecting the right protection element for a successful design.

This application note explains the key terminology, sections, and figures of an ESD protection device datasheet.

Topic **Page**

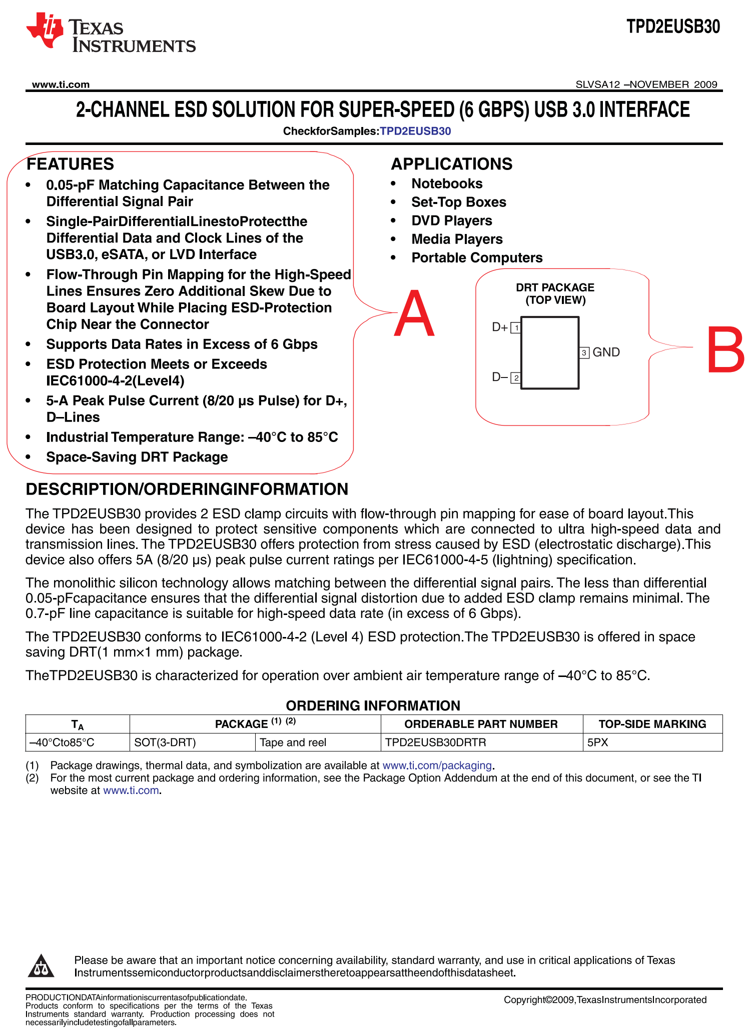
1 Datasheet Overview

Figure 1 shows a typical TI datasheet for an ESD protection device. Each of the different parts of the datasheet is explained in subsequent sections.

2 Front Page

The first page provides an overview of the device and quickly highlights its key features.

If one of the Features (A) or package options (B) draws your attention, it will be worthwhile to keep reading the rest of the datasheet.



TEXAS INSTRUMENTS TPD2EUSB30

www.ti.com SLVSA12 –NOVEMBER 2009

2-CHANNEL ESD SOLUTION FOR SUPER-SPEED (6 GBPS) USB 3.0 INTERFACE

CheckforSamples:TPD2EUSB30

FEATURES

- 0.05-pF Matching Capacitance Between the Differential Signal Pair
- Single-PairDifferentialLinestoProtectthe Differential Data and Clock Lines of the USB3.0, eSATA, or LVD Interface
- Flow-Through Pin Mapping for the High-Speed Lines Ensures Zero Additional Skew Due to Board Layout While Placing ESD-Protection Chip Near the Connector
- Supports Data Rates in Excess of 6 Gbps
- ESD Protection Meets or Exceeds IEC61000-4-2(Level4)
- 5-A Peak Pulse Current (8/20 µs Pulse) for D+, D–Lines
- Industrial Temperature Range: –40°C to 85°C
- Space-Saving DRT Package

A

APPLICATIONS

- Notebooks
- Set-Top Boxes
- DVD Players
- Media Players
- Portable Computers

DESCRIPTION/ORDERINGINFORMATION

The TPD2EUSB30 provides 2 ESD clamp circuits with flow-through pin mapping for ease of board layout.This device has been designed to protect sensitive components which are connected to ultra high-speed data and transmission lines. The TPD2EUSB30 offers protection from stress caused by ESD (electrostatic discharge).This device also offers 5A (8/20 µs) peak pulse current ratings per IEC61000-4-5 (lightning) specification.

The monolithic silicon technology allows matching between the differential signal pairs. The less than differential 0.05-pFcapacitance ensures that the differential signal distortion due to added ESD clamp remains minimal. The 0.7-pF line capacitance is suitable for high-speed data rate (in excess of 6 Gbps).

The TPD2EUSB30 conforms to IEC61000-4-2 (Level 4) ESD protection.The TPD2EUSB30 is offered in space saving DRT(1 mm×1 mm) package.

TheTPD2EUSB30 is characterized for operation over ambient air temperature range of –40°C to 85°C.

ORDERING INFORMATION

T_A	PACKAGE (1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°Cto85°C	SOT(3-DRT)	Tape and reel	TPD2EUSB30DRTR	5PX

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instrumentssemiconductorproductsanddisclaimerstheretoappearsattheendofthisdatasheet.

PRODUCTIONDATAinformationiscurrentasofpublicationdate. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarilyincludetestingofallparameters.

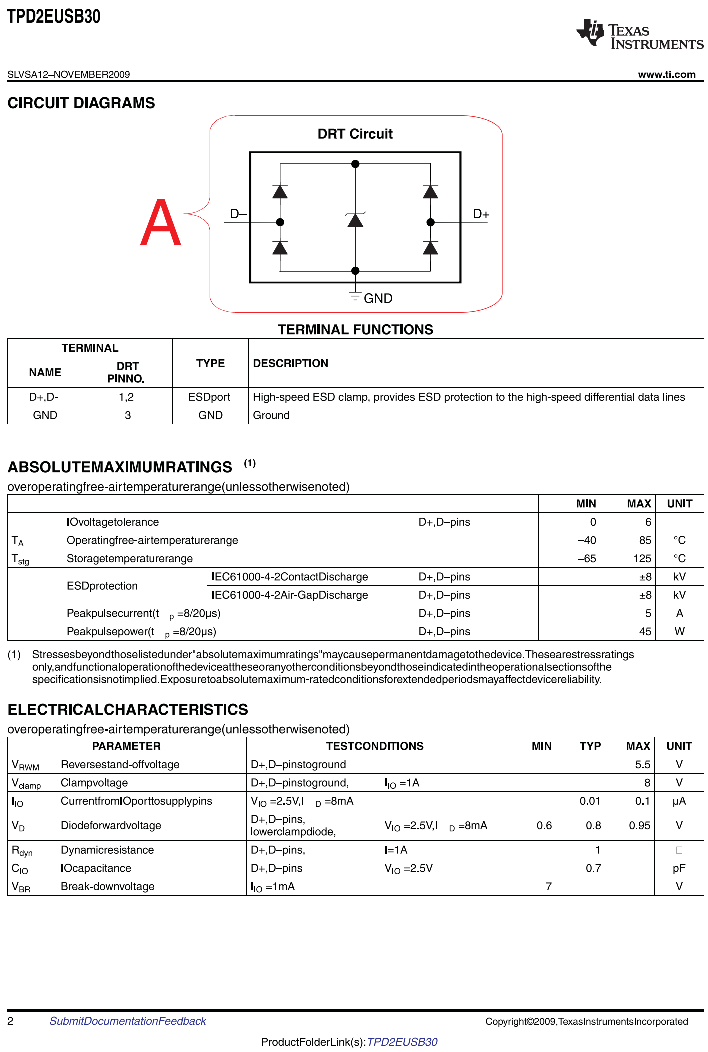
Copyright©2009,TexasInstrumentsIncorporated

Figure 1. Datasheet Front Page

In the example above, the TPD2EUSB30 datasheet highlights the device's best in class <50 pF matching capacitance and easy to route flow-through package pinout. It is likely that these features would be beneficial for your high-speed designs and we should keep reading.

3 Second Page

The second page of a TI datasheet typically shows a simplified circuit diagram (see Figure 2). This simplified schematic is intended to give a functional overview of the device while not distracting with detailed information. The System level designer should see all necessary information required for evaluating the ESD device in the system level design. The detailed inner circuitry information does not usually provide any useful information for completing a system level simulation. If the detailed information is required, it can be requested through your local TI sales office.



TPD2EUSB30

SLVSA12–NOVEMBER2009 www.ti.com

CIRCUIT DIAGRAMS

TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	DRT PINNO.		
D+,D-	1,2	ESDport	High-speed ESD clamp, provides ESD protection to the high-speed differential data lines
GND	3	GND	Ground

ABSOLUTEMAXIMUMRATINGS (1)

overoperatingfree-airtemperaturerange(unlessotherwisenoted)

				MIN	MAX	UNIT
	IOvoltagetolerance		D+,D–pins	0	6	
T_A	Operatingfree-airtemperaturerange			–40	85	°C
T_{stg}	Storagetemperaturerange			–65	125	°C
	ESDprotection	IEC61000-4-2ContactDischarge	D+,D–pins		±8	kV
		IEC61000-4-2Air-GapDischarge	D+,D–pins		±8	kV
	Peakpulsecurrent(t_p =8/20μs)		D+,D–pins		5	A
	Peakpulsepower(t_p =8/20μs)		D+,D–pins		45	W

(1) Stressesbeyondthoselistedunder"absolutemaximumratings"maycausepermanentdamagetothedevice.Thesearestressratings only,andfunctionaloperationofthedeviceattheseoranyotherconditionsbeyondthoseindicatedintheoperationalsectionsofthe specificationsisnotimplied.Exposuretoabsolutemaximum-ratedconditionsforextendedperiodsmayaffectdevicereliability.

ELECTRICALCHARACTERISTICS

overoperatingfree-airtemperaturerange(unlessotherwisenoted)

PARAMETER		TESTCONDITIONS		MIN	TYP	MAX	UNIT
V_{RWM}	Reversestand-offvoltage	D+,D–pinstoground				5.5	V
V_{clamp}	Clampvoltage	D+,D–pinstoground,	I_{IO} =1A			8	V
I_{IO}	CurrentfromIOporttosupplypins	V_{IO} =2.5V,I_D =8mA			0.01	0.1	μA
V_D	Diodeforwardvoltage	D+,D–pins, lowerclampdiode,	V_{IO} =2.5V,I_D =8mA	0.6	0.8	0.95	V
R_{dyn}	Dynamicresistance	D+,D–pins,	I=1A		1		□
C_{IO}	IOcapacitance	D+,D–pins	V_{IO} =2.5V		0.7		pF
V_{BR}	Break-downvoltage	I_{IO} =1mA		7			V

2 SubmitDocumentationFeedback Copyright©2009,TexasInstrumentsIncorporated

ProductFolderLink(s):TPD2EUSB30

Figure 2. Datasheet Second Page

4 Absolute Maximum Ratings and Electrical Characteristics

The absolute maximum ratings table of the device must be reviewed carefully. ESD protectors are typically not designed to handle DC overstress and an excess voltage above the absolute maximum ratings will most likely trigger the ESD device.

While short time pulses (0–300 ns) will not damage the protector; DC like stress (>1ms) will result in damage if no current limitation is provided (typically ≈500 mA). TI will provide information about the DC characteristic of the ESD protection devices upon customer request, but it is generally not recommended to use an ESD protector as a DC voltage limiter.

ABSOLUTE MAXIMUM RATINGS [(1)]

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
	IO voltage tolerance		D+,D–pins	0	6	
T_A	Operating free-air temperature range			–40	85	°C
T_{stg}	Storage temperature range			–65	125	°C
	ESD protection	IEC61000-4-2 Contact Discharge	D+,D–pins		±8	kV
		IEC61000-4-2 Air-Gap Discharge	D+,D–pins		±8	kV
	Peak pulse current (t_p = 8/20 μs)		D+,D–pins		5	A
	Peak pulse power (t_p = 8/20 μs)		D+,D–pins		45	W

(1) Stresses beyond those listed under"absolute maximum ratings"may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Figure 3. Absolute Maximum Ratings

The electrical characteristics section of the datasheet is arguably the most important. This section will be discussed in greater detail as ESD protectors have specific key parameters which must be understood thoroughly.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	D+,D–pins to ground				5.5	V
V_{clamp}	Clamp voltage	D+,D–pins to ground,	I_{IO} =1 A			8	V
I_{IO}	Current from IO port to supply pins	V_{IO} =2.5V,I_D =8 mA			0.01	0.1	μA
V_D	Diode forward voltage	D+,D–pins, lower clamp diode,	V_{IO} =2.5 V, I_D=8mA	0.6	0.8	0.95	V
R_{dyn}	Dynamic resistance	D+,D–pins,	I = 1 A		1		Ω
C_{IO}	IO capacitance	D+,D–pins	V_{IO} =2.5 V		0.7		pF
V_{BR}	Break-downvoltage	I_{IO} =1mA		7			V

Figure 4. Electrical Characteristics

5 Special Electrical Characteristics of ESD Protectors

5.1 Breakdown Voltage (V_{BR})

The voltage limit where the ESD protector will start to conduct significant amounts of current when exceeded. The Breakdown Voltage, in combination with the Dynamic Resistance (Rdyn), are very important factors in choosing the right ESD protector for a system level design.

5.2 Standoff Voltage (V_{st-off})

The standoff voltage describes the voltage level up to which there is no significant influence to the protected circuitry or data line other than the ESD device parasitics (capacitance, leakage, etc.).

5.3 Dynamic Resistance (R_{dyn})

The equivalent resistance of the protection device during an ESD discharge. R_{dyn} is an important factor for evaluating the effectiveness of the ESD clamp. During an ESD discharge, currents in the multiple ampere range are forced to flow through the protection device. The discharge current through R_{dyn} will cause a voltage drop over the device under test (DUT) . If the generated voltage is too high, damage may result to the parts of the system which were intended to be protected. Lower R_{dyn} will result in lower stress voltages to the system during an ESD event.

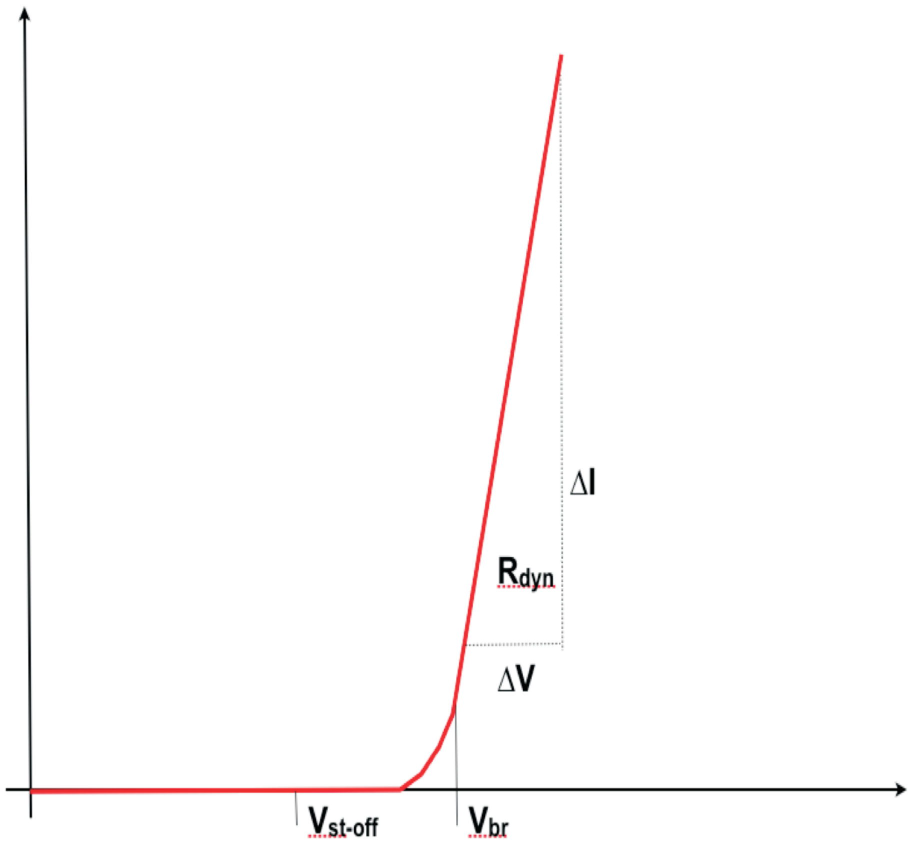


Figure 5. Standoff and Breakdown Voltage

6 Understanding ESD Characteristics Plots

ESD protection devices often include specialized plots that aid in selecting the right protection element for a given system-level design.

This section provides a detailed discussion of the ESD-specific plots not normally seen in standard datasheets.

6.1 Transmission Line Pulser Plots (TLP)

The TLP plot gives an overview of the device behavior during an ESD stress event. Typical TLP generators will use a rectangular current pulse of 1 to 5 ns rise time and 100 ns pulse width. The current pulse can be varied between 0 to 10 A. Important parameters provided by the plot are the breakdown voltage and the dynamical resistance of the clamp. In the given example plot from the TPD2EUSB30 Datasheet, the device's snap-back characteristic is clearly visible. The snap-back technique is employed to reduce the overall voltage drop during an ESD stress event. For more details about TI's special snap-back protection elements, please refer to the application note *Snap-Back Protection Scheme for ESD Protection Devices* (TI literature number SLLA306).

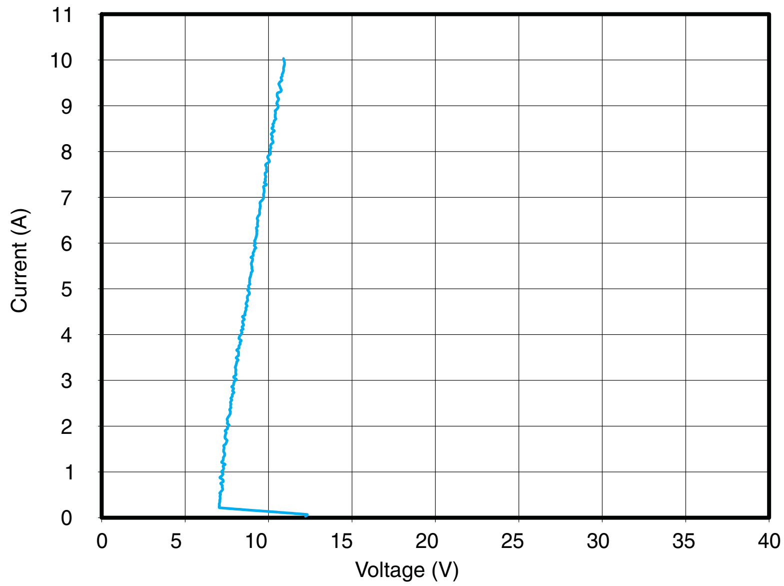


Figure 6. TLP Plot

6.2 *Peak Pulse Waveform*

Similar to the TLP plot, the Peak Pulse Waveform shows the behavior of the ESD protector under ESD stress. The peak pulse plots are taken by exposing the ESD protector to IEC62000-4-2 stress. The important information for the System level Engineer is the voltage stress during the first 25 ns of the pulse. While typically the very first peak can be ignored due to the short nature of the pulse and potential the influence of the measurement setup, the second and third pulses give a realistic picture of the voltage stress during an IEC ESD stress event. The lower and the faster decaying these voltage peaks are, the better the chances are to successfully protect the system components.

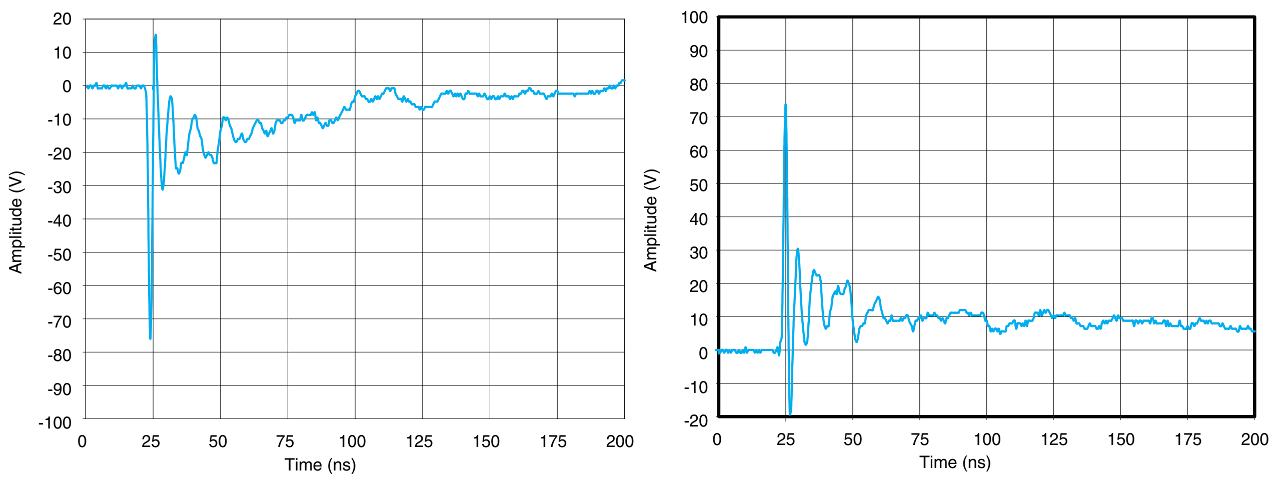


Figure 7. Typical Peak Pulse Plots

6.3 *Eye Diagram*

The eye diagrams provide an overview of how the ESD protector influences high-speed design. Ideally, no noticeable change in the eye pattern should be observed. However, due to the parasitic capacitance, small variations in the jitter (1a vs 1b) can be observed. In case of the TPD2EUSB30, the jitter penalty is negligible.

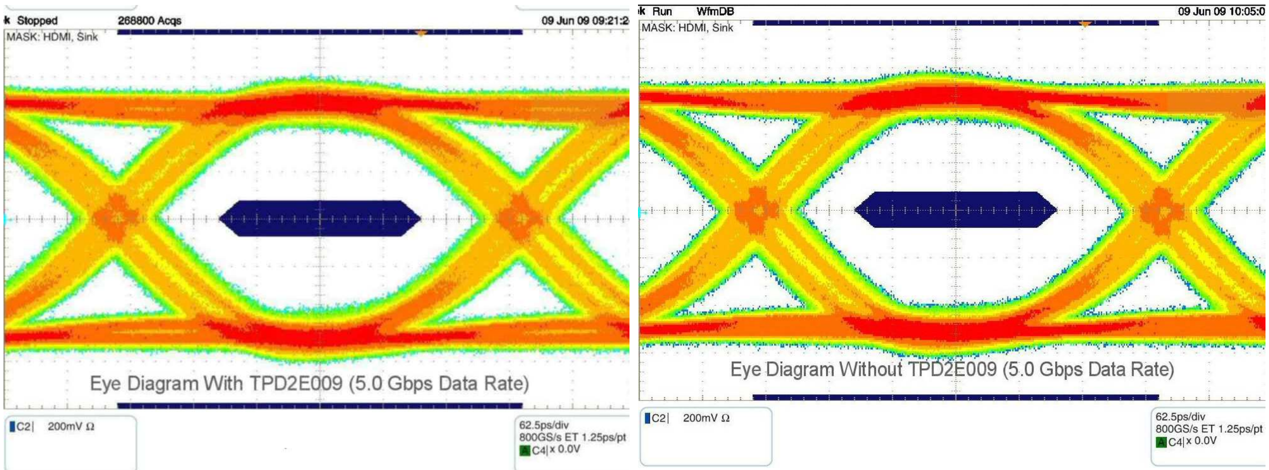


Figure 8. Eye Diagrams

Visit www.ti.com for information and data sheets on Texas Instruments full line of voltage translators.