Application Report
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Selecting a Load Switch to Replace a Discrete Solution

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ABSTRACT

Integrated load switches are a great way to reduce board space and improve switching performance and protection over existing discrete MOSFET solutions. This application note goes into detail on how to identify what features are present in a discrete MOSFET solution as well as the design advantages and simplifications of integrated load switches.

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1 Overview

A simple, active-high discrete MOSFET circuit looks similar to Figure 1. Note that when the switch is ON, there is a constant leakage current from V_{IN} to ground through the resistor. Figure 2 shows that when the switch turns on there is a high inrush current which causes an input voltage drop.

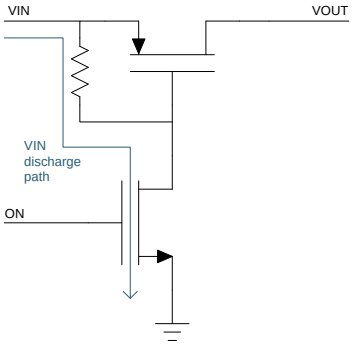

Figure 1. Simple, Active-High Discrete Solution

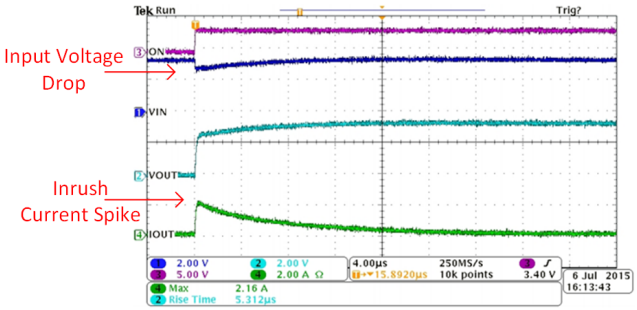

Figure 2. Uncontrolled Inrush Current

A controlled rise time prevents stress on the power supply and reduces input voltage drop during the enabling of the switch. Discrete controlled rise time is shown in Figure 3.

Although the capacitor helps by controlling rise time, it also negatively affects the operation of the rail. When the NMOS turns on and connects the gate of the PMOS to ground, current flows from the input through the resistor to ground. This creates a momentary positive voltage at the gate of the PMOS which generates a negative voltage at the output. This negative voltage spike can be seen in Figure 4.

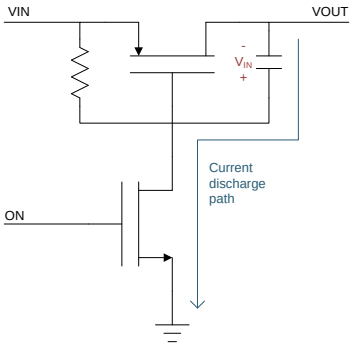

Figure 3. Simple, Active-High Discrete Solution With Controlled Rise Time

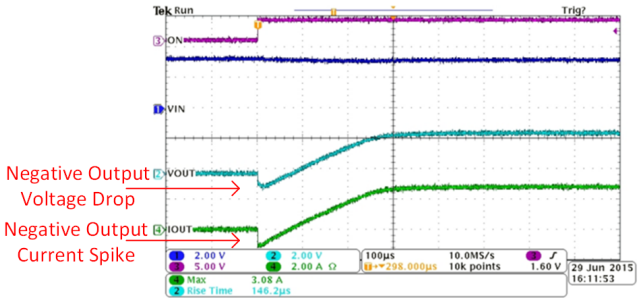

Figure 4. Negative Voltage From Capacitor

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Figure 5 shows a simple 4-pin, active-high load switch with an internally controlled rise time. This solution takes less space than the discrete solution. See Example 1 for a detailed comparison of a simple discrete solution versus a simple integrated load switch.

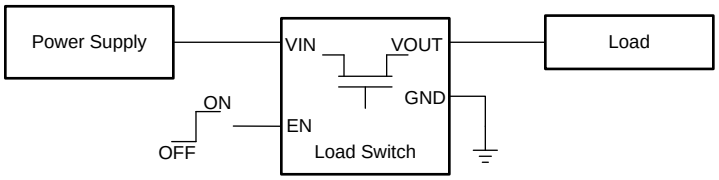

Figure 5. 4-Pin Load Switch

All load switches offer a fixed or adjustable rise time which controls the inrush current and slew rate of the device. A controlled slew rate results in a smooth output voltage ramp without negative voltage spikes or drops in input voltage when the device turns on, as shown in Figure 6.

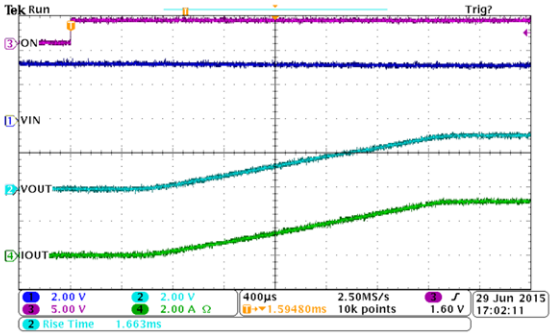

Figure 6. 4-Pin Load Switch Turnon

2 Basic Parameters

The beginning process of selecting an integrated load switch is determining the basic operating parameters for a rail: V_{IN}, I_{OUT}, and the maximum V_{OUT} deviation. These three parameters are all co-dependent on each other; in most situations, V_{IN} and I_{OUT} of the rail are fixed and the V_{OUT} deviation is set based on system tolerances. The V_{OUT} deviation is caused by voltage drop from current passing through the on-resistance, R_{ON}, of the load switch. Inrush current occurs when the load switch turns on and can be controlled with a fixed or adjustable slew rate. For integrated load switches: V_{IN}, I_{OUT}, R_{ON}, and slew rate are all basic parameters that are given for each part.

2.1 On-Resistance

First, verify V_{IN} and I_{OUT} of the part fits the rail requirements and determine what is the maximum V_{OUT} deviation for the rail. Then, solve for the maximum R_{ON} that is within the system tolerance based on the maximum V_{OUT} deviation.

If, for example, a 3.3 V rail that carries 1 A of current is allowed to deviate 0.1 V then the maximum R_{ON} allowed is 100 mΩ, see Equation 1.

$$R_{ON\text{-}MAXIMUM} = \Delta V_{MAXIMUM}/I_{OUT} \quad (1)$$

It is best to keep a safe margin when choosing R_{ON}, given the allowable voltage drop on a rail, because voltage drops can still occur at other stages on the rail.

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2.2 Inrush Current, Slew Rate, and Rise Time

The last basic parameter for a system is how much inrush current can be handled by the downstream components. If inrush current is too high, it can damage downstream components when the switch turns on. If inrush current is too low, the output rail rises too slowly. In order to control inrush current, slew rate must be controlled.

Integrated load switches either have a fixed slew rate, which is handled internally to the part, or an adjustable slew rate which is controlled based on the capacitance set on the CT or dV/dt pin. Each part with adjustable slew rate has an estimate equation in the datasheet for calculating the slew rate based on a given capacitance on the CT or dV/dt pin.

Slew rate controls the rise time of the output and rise time limits the inrush current. Rise time and inrush current are inversely proportional to each other as shown in Equation 2.

$$I_{INRUSH} = C_{OUT} \times dV/dt \quad (2)$$

Where

- C_{OUT} is the output capacitance
- dV is the output voltage
- dt is the rise time

3 Performance Features

There are two additional performance related features that may be present in a discrete solution: *Quick Output Discharge* and *Power Good*. Quick Output Discharge is used to rapidly discharge load capacitance so that the output voltage of a switch is not left floating. Power Good is an output that signifies the output power rail in on.

3.1 Quick Output Discharge

In a discrete solution, Quick Output Discharge, QOD, is implemented using a pull-down FET (or BJT) and pull-down resistor connected from V_{OUT} to ground. When the pass FET turns off, the pull-down FET turns on, and the pull-down resistor in series with the pull-down FET on-resistance are added in parallel to the load resistance. This brings the overall resistance down, as seen by the load capacitance, see Figure 7.

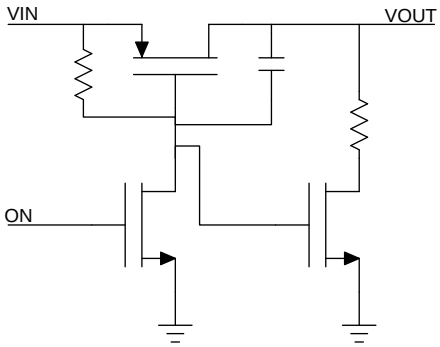

Figure 7. Discrete Quick Output Discharge Feature

In an integrated load switch, QOD is implemented with a bipolar transistor in series with a pull-down resistor. When the load switch turns off, QOD turns on to discharge the load capacitance faster. The way that the load capacitor is discharged depends on the biasing conditions of the transistor. See Figure 8.

- If the transistor is in forward-active mode, it acts as a constant current sink. This pulls current out of the load capacitance at a constant rate regardless of output voltage.
- If the transistor is in saturation mode, it acts as a resistor in series with the pull-down resistor. This pulls current out of the load capacitance based on the output voltage at a given time.
- Once the transistor reaches cutoff mode, the transistor opens the connection from the pull-down resistor to ground. Current only follows through the load resistance now.

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The transistor modes are controlled by the bias voltage conditions of the transistor. As voltage on the load capacitance falls, the transistor moves from forward-active mode into saturation then into cutoff mode.

Integrated load switches with QOD reduce the need for additional external components, reducing area.

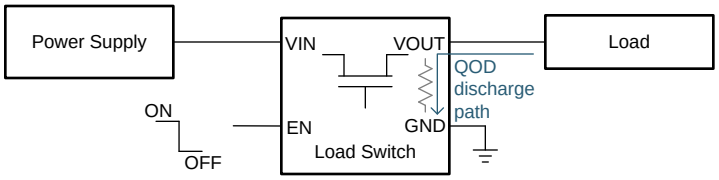

Figure 8. Load Switch With Quick Output Discharge

3.2 Power Good

Power Good, PG, is an output that signifies that the output power rail is up and running. A discrete implementation can look similar to Figure 9. A second rail, V+, is needed for the discrete PG solution otherwise the PG output is left floating at the output rail when the discrete solution is off. PG may also require a third rail depending on the desired voltage of the PG output; Figure 9 assumes that the V_{OUT} voltage is the desired voltage for the PG signal.

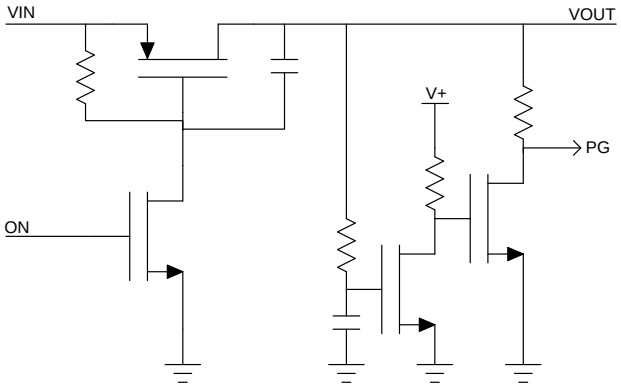

Figure 9. Discrete Power Good Feature

When V_{OUT} is low: the voltage at the gate of the left FET is low, turning it off. This leaves the gate of the right FET pulled up to V+, turning it on and pulling the PG output to ground.

When V_{OUT} is high: the voltage at the gate of the left FET is high, turning it on. This connects the gate of the right FET to ground, turning it off and the PG output is pulled up to V_{OUT}.

An integrated load switch with PG (see Figure 10) provides the above functionality without the need for an additional voltage rail or external MOSFETs, reducing board layout and system level complexity. A single pull-up resistor can be connected from the output rail to the PG pin and the signal can be fed to: downstream components, to let them know their input rail is on; other load switches, for power sequencing operation; or even a micro controller, as a feedback signal that the rail is on.

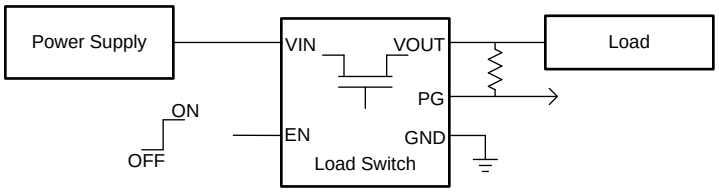

Figure 10. Load Switch With Power Good

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4 Protection Features

The next step to consider is, what protection features are currently in the discrete solution that need to be present in the integrated solution? There are four main protection features that can be implemented in discrete solutions: *Reverse Current Blocking*, *Discrete Undervoltage Lock-Out*, *Undervoltage Lock-Out*, and *Thermal Shutdown*. Reverse Current Blocking prevents current flow from the output to the input. Current limiting prevents the power supply from overloading. Undervoltage Lock-Out prevents a low voltage from being passed to the output. Thermal shutdown is implemented to protect the switch and its downstream components from excessive temperatures.

4.1 Reverse Current Blocking

Reverse Current Blocking, RCB, is implemented in order to protect the power supply on the input side of the switch as well as the switch itself. In a discrete solution, RCB prevents current flow from V_{OUT} to V_{IN} only when the switch is turned off. This is done using back to back FETs, see Figure 11.

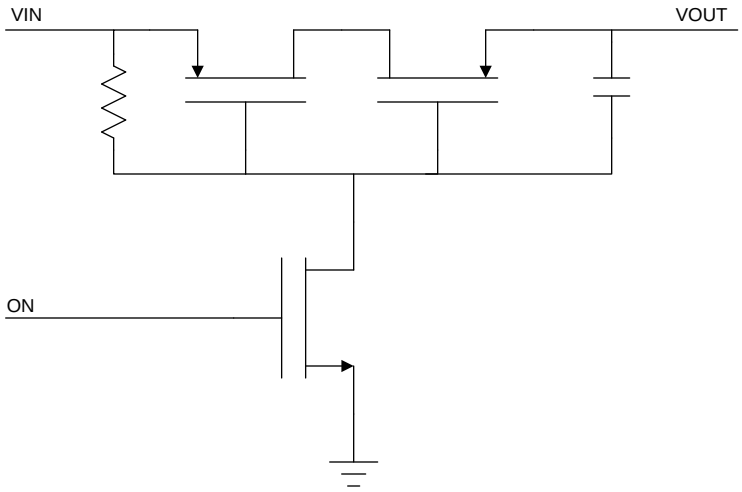

Figure 11. Discrete Reverse Current Blocking Feature

An integrated load switch can implement RCB using an internal comparator which allows for always-on RCB. This means that load switches with RCB prevents current flow from V_{OUT} to V_{IN} when the switch is turned off and in situations where the load switch is on with V_{OUT} greater than V_{IN}. Integrated load switches with always-on RCB allow for a smaller solution size, lower on-resistance, and broader protection over the discrete implementation. See Figure 12.

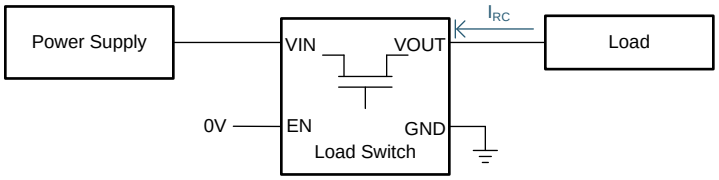

Figure 12. Load Switch With Reverse Current Blocking

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4.2 Current Limiting

Current limiting is implemented to protect the power supply from delivering more current than it is capable of. Overloading the power supply can damage the supply, the system, or the load. Current limiting in a discrete solution can be done using a current sense resistor that feeds into a comparator op-amp. The comparator output is connected to the NMOS which turns the pass FET on or off, as seen in Figure 13. This type of current limiting can cause output voltage oscillations based on the delay between the comparator turning off the NMOS, when there is too much output current, and turning the NMOS back on, once the output current is below the limit. The oscillation can be tapered, but not removed, by adding a resistor and capacitor to the output of the comparator; this also increases on time and off time of the solution.

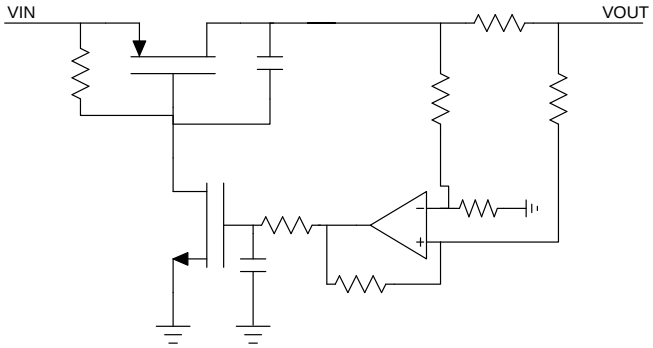

Figure 13. Discrete Current Limiting Feature

Integrated load switches take a similar approach of current limiting without the issue of output voltage oscillations. Integrated load switches heavily reduce the board space required over the discrete implementation, except for a single resistor connected from the current limit pin, I_{LIM}, to ground. The external resistor value can be changed to alter the amperage level of the adjustable current limit. See Figure 14.

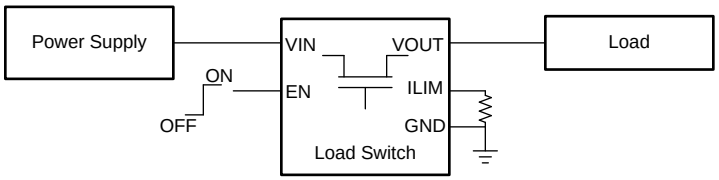

Figure 14. Load Switch With Current Limiting

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4.3 Undervoltage Lock-Out

Undervoltage lock-out, UVLO, is implemented to protect the downstream components on the rail from being damaged when the input voltage drops below a safe or intended level. UVLO, in a discrete solution, is done with a voltage divider branching off from the input voltage which feeds into a comparator op-amp. The reference for the comparator is set to the lowest acceptable voltage that the load switch must pass from input to output. The output of the comparator is connected to the NMOS which turns the pass FET on or off. Figure 15 shows the discrete implementation. When the input voltage, through the voltage divider, goes below the reference voltage of the comparator, the pass FET is turned off and the output is disconnected from the input.

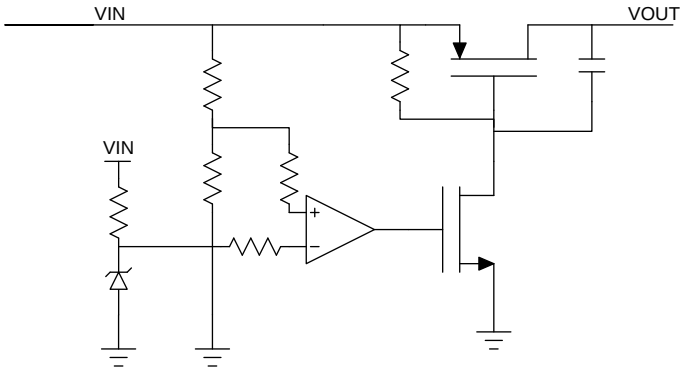

Figure 15. Discrete Undervoltage Lock-Out Feature

Integrated load switches incorporate all of the discrete components internally except for the voltage divider connected to the input. Some integrated load switches have a fixed, internally set UVLO reference voltage as well as an externally adjustable UVLO. When using the fixed UVLO setting, no external resistors are needed, reducing board space and part count even further. See Figure 16.

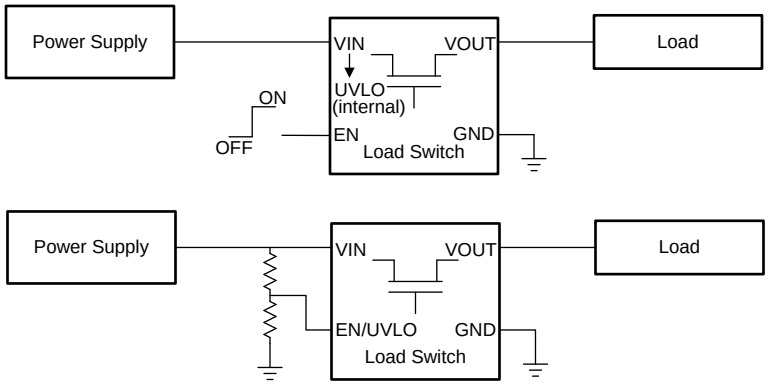

Figure 16. Load Switch with Undervoltage Lock-Out

4.4 Thermal Shutdown

Thermal shutdown, T_{SD}, protects the device from internally or externally generated excessive temperatures. Thermal shutdown can be implemented discretely using an temperature sensor IC or by using a thermistor and a comparator op-amp. Both of these options add board space and cost to the discrete solution.

Integrated load switches can offer thermal shutdown without an increase in size to the solution. When the device temperature triggers T_{SD} the switch is turned off. The switch automatically turns on again if the temperature of the die drops below the T_{SD} threshold; this is called thermal hysteresis. Thermal shutdown on a load switch is not only useful to protect the switch itself but can also be used to protect downstream components which may be facing similar high temperatures. If a device also has a power good output, when thermal shutdown is triggered the PG signal goes low. This can be used to communicate to the system that a fault has occurred.

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5 Example 1

Let's take a simple, discrete PMOS solution with a controlled rise time; no other features are included. The load switch needs to meet the following requirements:

- Input Voltage: 5 V
- Output Current: 4 A
- Max Output Voltage Deviation: 3%
- Rise time: approximately 500 µs

From the above: the maximum V_{OUT} deviation is 150 mV resulting in a maximum on-resistance of 37.5 mΩ, based on Equation 1. This discrete solution requires 1 resistor, 1 capacitor, 1 PMOS FET, and 1 NMOS FET, as shown in Figure 17.

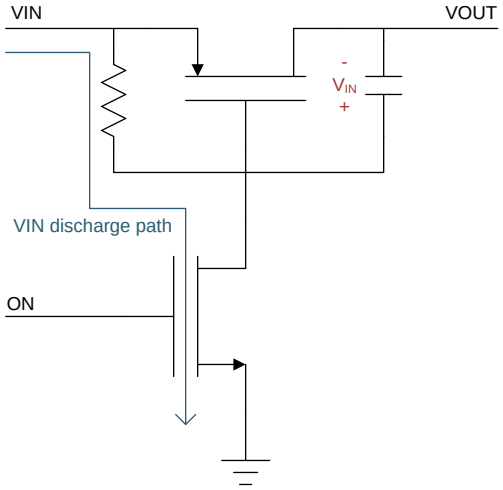

Figure 17. Discrete PMOS Solution Circuit

As the NMOS turns on, there is going to be a momentary positive voltage on the gate which in turn results in a momentary negative voltage on the output. Using typical 6-pin SOT packages for the FETs and 0402 package sizes for the passives, the total solution size comes to 17.24 mm^2.

The TPS22975N can handle the 5 V input, supports up to 6 A of current, has a typical on-resistance of 16 mΩ, and has an adjustable rise time. The rise time can be set at 520 µs with a 220 pF capacitor on the CT pin. The TPS22975N has the same simple functionality as the discrete circuit above while also providing thermal shutdown. The integrated solution requires: 1 TPS22975N and 1 capacitor (520 pF); the total solution size comes to 4.5 mm^2, as much as 26.1% of the size of the discrete solution. The integrated solution is shown in Figure 18.

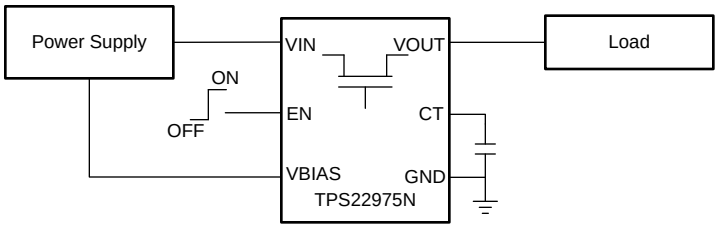

Figure 18. TPS22975N Solution

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6 Example 2

Let's take a feature-full discrete PMOS solution with controlled rise time, reverse current blocking, undervoltage lock-out, and power good. See Figure 19.

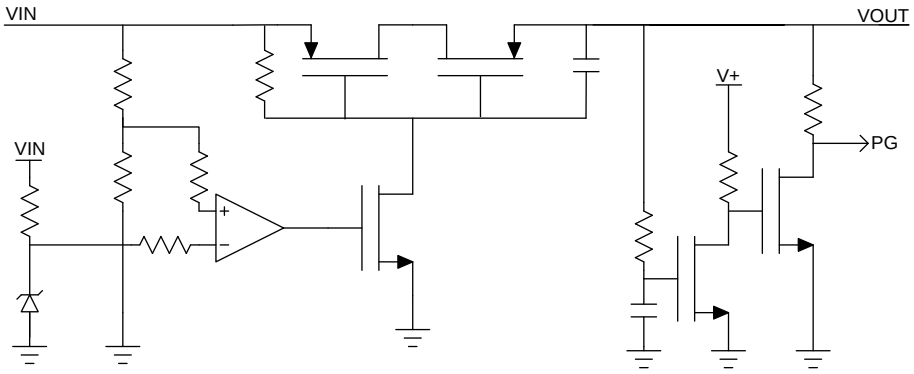

Figure 19. Discrete Feature Full Circuit

This solution requires: 2 PMOS, 3 NMOS, 1 comparator op-amp, 1 zener diode, 2 capacitors, and 9 resistors. The resistor and capacitor packages are assumed to be 0402s. A second rail, V+, is needed for PG. A third rail could be required depending on the desired voltage for the PG output, the above circuit assumes that the output voltage is the desired value for PG. Table 1 lists out each discrete component and their area. The discrete solution comes to 55.64 mm^2 total area.

Table 1. Size of Feature Full Discrete Parts

Device	Package	Size (mm^2)	Quantity	Area (mm^2)
PMOS	6-pin SOT	8.12	2	16.24
NMOS	6-pin SOT	8.12	3	24.36
Comparator Op-Amp	QFN	2.52	1	2.52
Zener Diode	SOD-123	7.02	1	7.02
Capacitor	0402	0.5	2	1
Resistor	0402	0.5	9	4.5
TOTAL				55.64

The TPS22953 offers adjustable controlled rise time, reverse current blocking, undervoltage lockout, and power good as well as thermal shutdown. The integrated solution requires: 1 TPS22953, 5 resistors, and 1 capacitor. It only requires 1 voltage rail, but a second higher voltage V_{BIAS} rail can be used. Table 2 lists out each component and their area.

Table 2. Size of Feature Full Integrated Parts

Device	Package	Size (mm^2)	Quantity	Area (mm^2)
TPS22953	10-pin WSON	6	1	6
Resistor	0402	0.5	5	2.5
Capacitor	0402	0.5	1	0.5
TOTAL				9

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The integrated solution, Figure 20, comes to 9 mm^2 total area, as much as 16% of the size of the discrete solution.

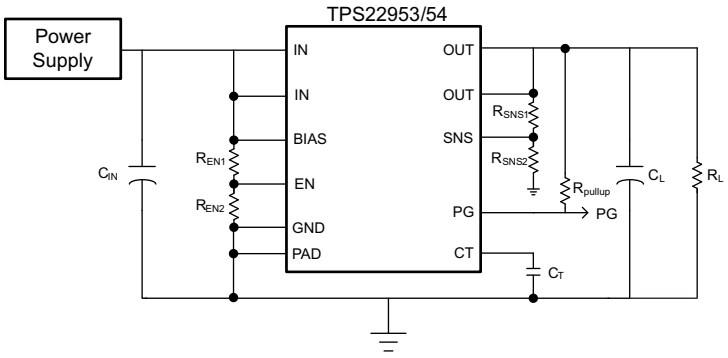

Figure 20. TPS22953 Typical Application

7 Example 3

Let's take a look at a simple power muxing discrete MOSFET solution with controlled rise time and reverse current blocking. See Figure 21.

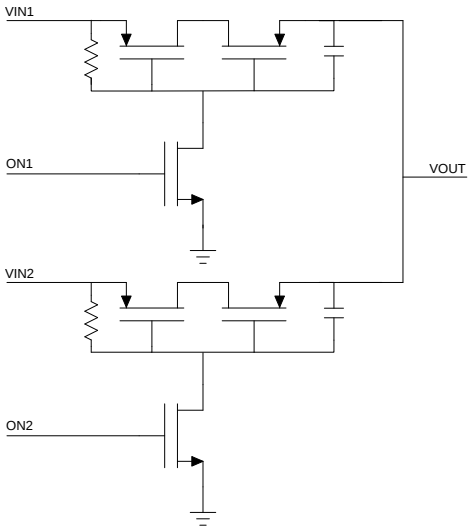

Figure 21. Discrete Power Muxing Circuit

This solution functions as a power mux but it does have 3 major performance and safety faults. This circuit cannot switch both supplies at the same time, turning one off while turning the other on, because the turn off time of the MOSFETs is substantially longer than the turn on time. In order to reduce fall time, the capacitor must be reduced but this increases inrush current which could damage downstream components. Secondly, because the switches cannot be switched at the same time, two enable signals are needed to control the power mux. Lastly, as shown before, a controlled rise time implemented in the circuit above causes a negative voltage spike on the output when the power supply changes.

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This solution requires: 4 PMOS, 2 NMOS, 2 resistors, and 2 capacitors. 6-pin SOT packages are used for the FETs and 0402 packages will be used for the passives. Table 3 lists out each discrete component and their area. The discrete solution comes to 50.72 mm^2 total area.

Table 3. Size of Power Muxing Discrete Parts

Device	Package	Size (mm^2)	Quantity	Area (mm^2)
PMOS	6-pin SOT	8.12	4	32.48
NMOS	6-pin SOT	8.12	2	16.24
Resistor	0402	0.5	2	1
Capacitor	0402	0.5	2	1
TOTAL				50.72

The TPS2115A is a power muxing integrated solution which includes reverse current blocking and controls inrush current though current limiting and a fixed rise time (See Figure 22). This integrated solution allows for automatic or manual switching and can be controlled with zero enable pins (automatically), or by one or two enable pins depending on the level of desired control. In comparison to the circuit above, only one enable pin is needed. Thermal shutdown is also included in this integrated solution as well as a switch status output pin (similar to power good) which is held high when input 1 is being passed to the output and is held low when input 2 is being passed to the output.

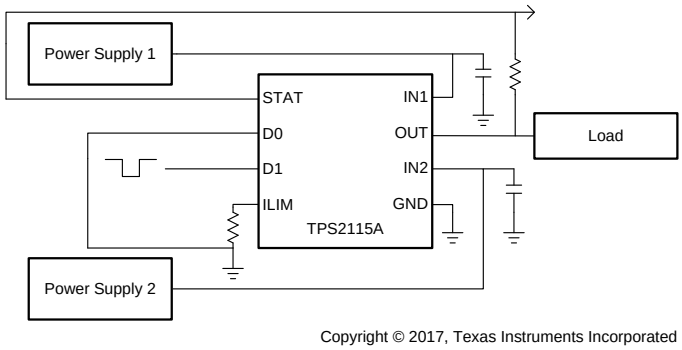

Figure 22. TPS2115A Manual Power Muxing Application

The integrated solution requires: 1 TPS2115A, 2 resistors, and 2 capacitors. The TPS2115A package is an 8-pin SON and the passives uses 0402 packages. The total integrated solution size is 11 mm^2, as much as 21.7% of the discrete solution.

8 Conclusion

All in all, integrated load switches offer space conscious solutions with the options of additional performance and protection features without digging into available board space. Integrated load switches allow current limiting, without the threat of output oscillations, and true always-on reverse current blocking, which protects the load switch and power supply when the load switch is on or off. Integrated load switches allow for cleaner and safer output voltage ramps over simple discrete solutions without the threat of inrush current affecting the downstream components.

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9 References

1. *TPS22975 5.7V, 6A, 16mΩ Load Switch with Adjustable Rise Time & Optional QOD for Cost-Conscious Applications*
2. *TPS22953 5.7V, 5A, 14mΩ Load Switch with Voltage Monitoring and Reverse Current Protection*
3. *TPS2115A Autoswitching Power Mux*

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