TPS2350 –48-V Hot Swap/Supply Selector Evaluation Module

User's Guide

EVM IMPORTANT NOTICE (CATEGORY B)

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It is important to operate this EVM within the maximum input voltage ranges specified in Table 2.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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TPS2350 −48-V Hot Swap/Supply Selector Evaluation Module

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ABSTRACT

This User's Guide describes the use and features of the TPS2350 −48-V Hot Swap/Supply Selector Evaluation Module (EVM). This EVM can be used to learn about the TPS2350 Hot Swap Power Manager (HSPM) Integrated Circuit (IC) from Texas Instruments (TI).

Contents

1 Introduction

The TPS2350 is a negative voltage hot swap controller intended for use in systems needing to hot swap telecom distribution-level voltages. It integrates inrush current control, peak current limiting, electronic circuit breaker, and overvoltage and undervoltage protection. In addition, it monitors and selects from two power supplies the larger magnitude supply, reducing OR-ing losses in redundant supply systems. The EVM is a PCB-based tool featuring the TPS2350 in a hot swap circuit, and can be used to evaluate device operation in simulated live insertion events.

1.1 Features

The following list highlights some of the features of the TPS2350 device.

- Wide input supply range of −12 V to −80 V
- Transient rating to −100 V
- Programmable current limit
- Programmable linear inrush slew rate
- Redundant supply selector function
- Programmable UV/OV thresholds/hysteresis
- Fault timer to eliminate nuisance trips
- Open-drain power good (PG) output
- Open-drain fault output ($\overline{\text{FLT}}$)
- 14-pin TSSOP package

1.2 Description

The TPS2350 integrated circuit is a hot swap power manager optimized for use in nominal −48-V systems. It operates over a supply voltage range of −12 V to −80 V, and is rated to withstand spikes to −100 V. In conjunction with an external N-channel FET and sense resistor, it can be used to enable live insertion of plug-in cards and modules into powered systems. It provides load current slew rate control and peak magnitude limiting. Undervoltage and overvoltage shutdown thresholds are easily programmed via a three-resistor divider network. A power good (PG) output enables downstream converters. The TPS2350 also provides the basic hot swap functions of electrical isolation of faulty cards, filtered protection against nuisance overcurrent trips, and single-line fault reporting.

The TPS2350 also provides a unique feature for redundant-supply systems. The supply selection function can be used to reduce power losses of diode-OR systems. A selection comparator monitors the two input supplies, and selects the supply with the larger magnitude. Internal driver circuits provide the gate drive needed to control two external N-channel FETs, providing a low-loss switch closure for the active supply, while disconnecting the lower voltage supply.

For input capacitor charging and load current faults, the TPS2350 provides an internal fault timer to filter out spurious current glitch events. In the event of a persistent fault which exceeds the programmable timer setting, the TPS2350 turns off the hot swap FET, disconnecting the load. A retry mode periodically tests for continued existence of the fault at a low duty cycle, thus protecting the pass FET from excessive dissipation.

2 The TPS2350 −48-V Hot Swap/Supply Selector EVM Kit

2.1 Module Description

The TPS2350 −48-V hot swap/supply selector EVM kit is a PCB-based platform that enables designers to rapidly learn about the TPS2350 operation, and evaluate its performance during hot swap events. The assembly (TI part number HPA021−001) features a TPS2350 device as it may be connected in the power interface section of a hot swap-capable plug-in card. The assembly also provides additional controls and components to simplify testing and for quick modifications of the circuit characteristics. Input power to the module is connected at three banana jacks located on the left-hand side of the board. A toggle switch is provided to rapidly apply power to and remove it from the circuit.

The hot swap circuit on the EVM board contains the TPS2350 HSPM device, a power MOSFET switch, sense resistor and some configuration capacitors. Two through-hole patterns are provided on the load side for the installation of large-value aluminum electrolytic capacitors. These capacitors simulate the input bulk capacitance that may be found on the target module's back-end supply plane. The EVM is supplied from the factory with a 100-μF capacitor installed in one of the locations. The second pattern, connected in parallel with the first, can be used to increase or otherwise modify the amount of load capacitance. With the TPS2350, both inrush slew rate limiting and a fault time-out period are externally programmable using capacitors. On the EVM board, several options are provided for slew rate limit setting, for quick comparison of the effect of capacitor value on this function. The capacitors can be quickly switched in and out of the circuit via the DIP switch SW1. Fault timing programming is set up in a similar manner; some amount of capacitance is hard-wired into the circuit, with the option of switching in additional capacitance.

N-channel FETs are also provided on-board to exercise or demonstrate the supply selection operation of the TPS2350 when two supplies are connected to the board.

The board also contains the component patterns and connections to exercise the undervoltage (UVLO) and overvoltage (OVLO) lockout functions. A slide switch is also tied into the UV input pin to provide an alternate means of enabling and disabling the output voltage. The powergood output can be monitored directly at the device pin, or through the on-board opto-coupler.

Test points are provided throughout the circuit for easy voltage monitoring via oscilloscope or voltmeter. The test point connections are listed in Table 6.

The pictorial of the TPS2350 −48-V hot swap/supply selector EVM top assembly is shown in Figure 1.

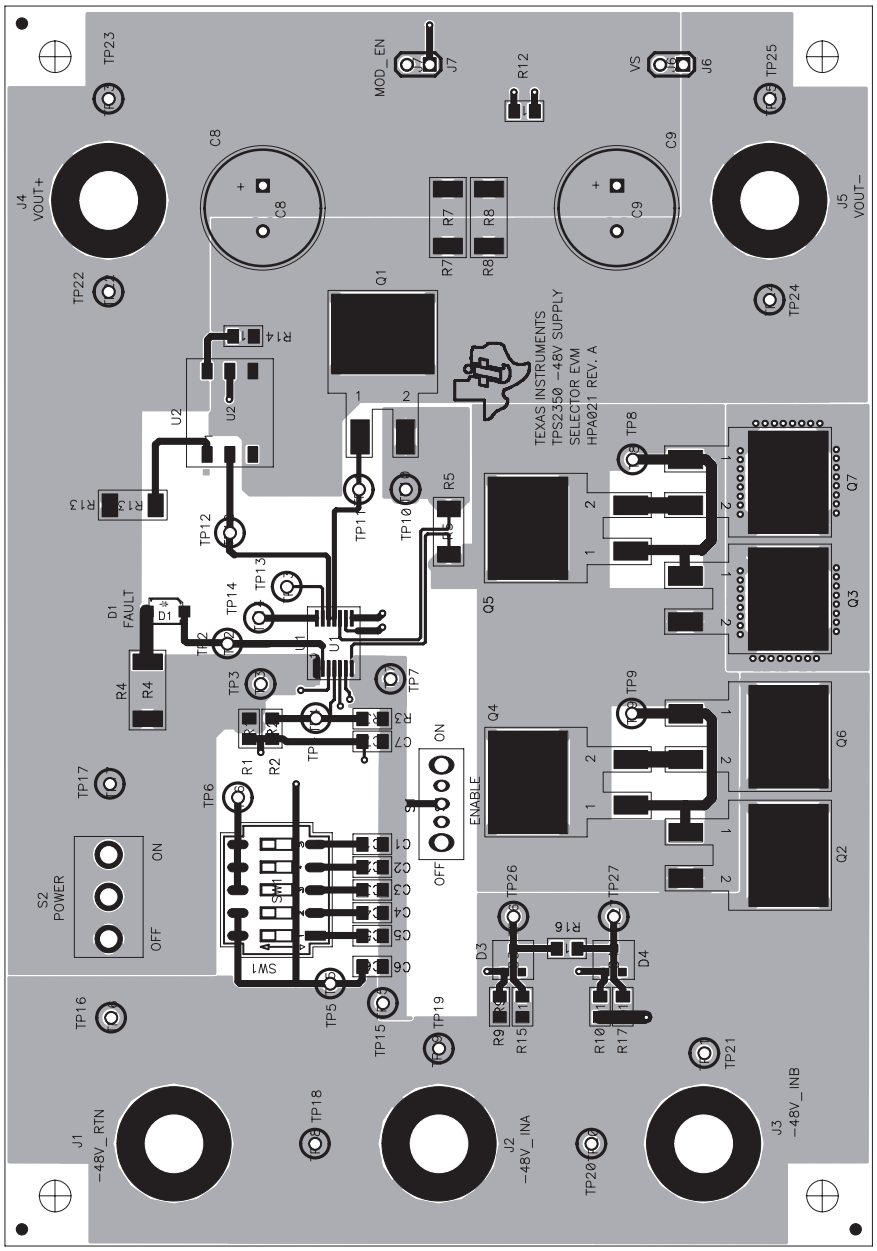

Figure 1. Evaluation Module Top Assembly

2.2 EVM Schematic Diagram and List of Materials

The EVM schematic diagram is shown in Figures 2 and 3.

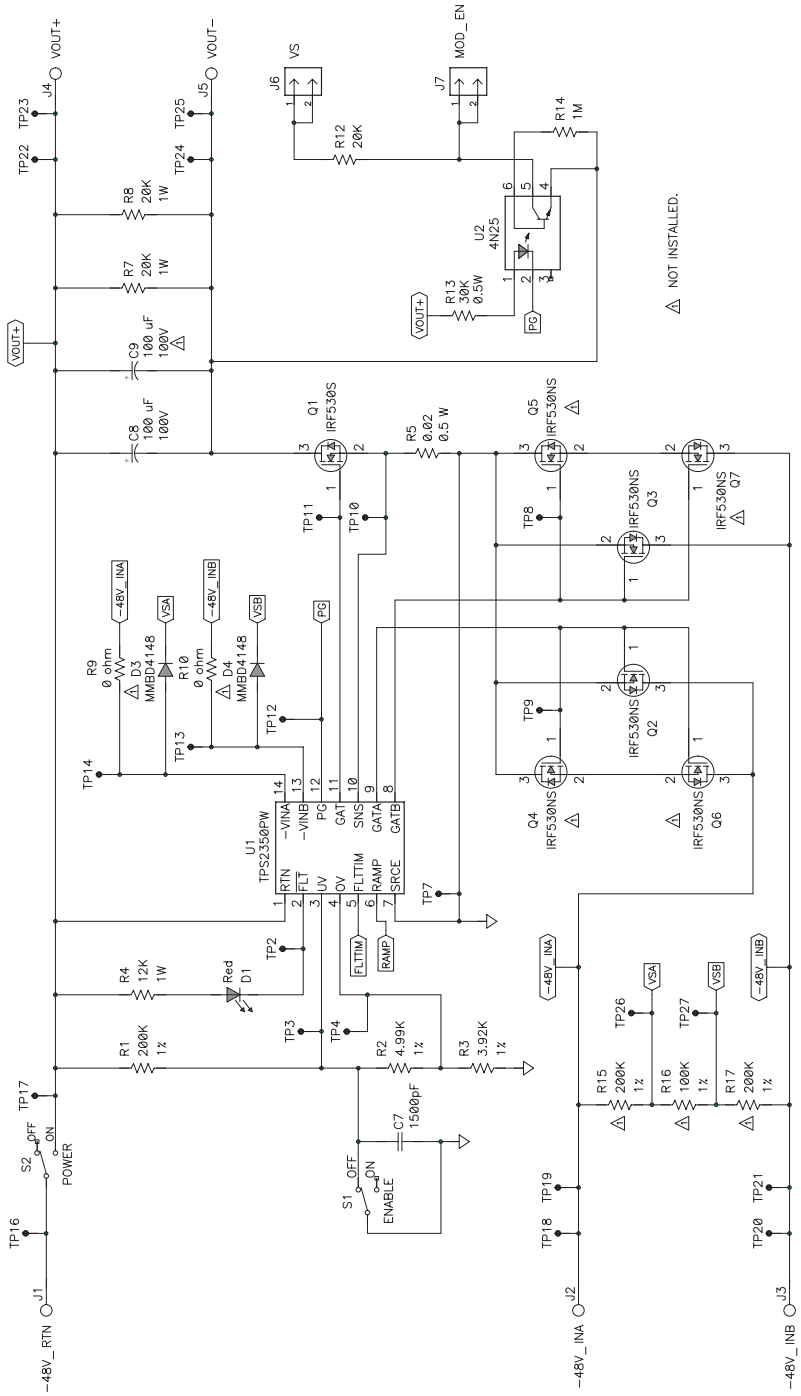

Figure 2. TPS2350 −48-V Hot Swap/Supply Selector EVM Schematic (Sheet 1)

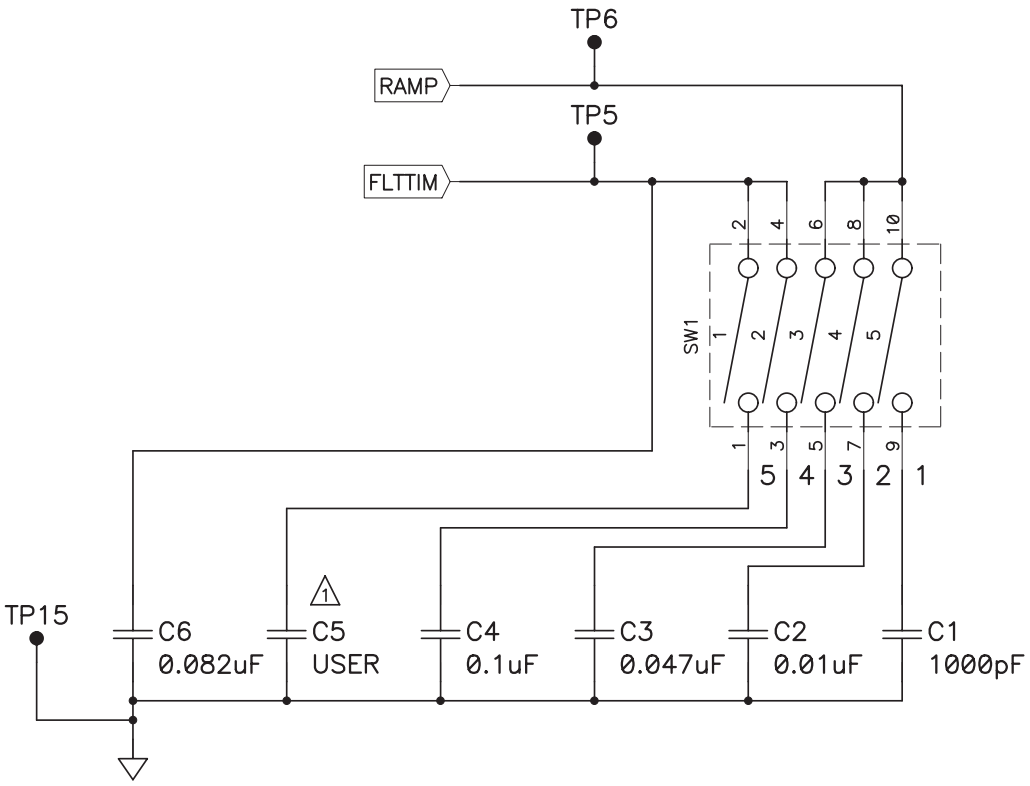

Figure 3. TPS2350 −48-V Hot Swap/Supply Selector EVM Schematic (Sheet 2)

The EVM list of materials is shown in Table 1.

Table 1. Evaluation Module List of Materials (HPA021A)

REFERENCE	QTY	DESCRIPTION	MANUFACTURER	PART NUMBER
C1	1	Capacitor, ceramic, 1000 pF, 25 V, 10%, X7R	Vitramon	VJ0805Y102KXXA
C2	1	Capacitor, ceramic, 0.01 μF, 16 V, 10%, X7R	Vitramon	VJ0805Y103KXJA
C3	1	Capacitor, ceramic, 0.047 μF, 16 V, 10%, X7R	Vitramon	VJ0805Y473KXJA
C4	1	Capacitor, ceramic, 0.1 μF, 16 V, 10%, X7R	Vitramon	VJ0805Y104KXJA
C5	−	Capacitor, ceramic, 0805	Standard	Standard
C6	1	Capacitor, ceramic, 0.082 μF, 16 V, 10%, X7R	Vitramon	VJ0805Y823KXJA
C7	1	Capacitor, ceramic, 1500 pF, 25 V, 20%, X7R	Vitramon	VJ0805Y152MXXA
C8	1	Capacitor, aluminum electrolytic, 100 μF, 100 V, 20%	Vishay	EKA00DE310L00
C9	−	Capacitor, aluminum electrolytic, 100 V, radial	Standard	Standard
D1	1	DIODE, LED, ultra bright red, GW type	Panasonic	LN1261CAL
D3, D4	−	DIODE, Switching, 75 V, 0.35 W, type 4148	Standard	Standard
Q1	1	MOSFET, N-channel, V(BR) > 100 V	Int'l Rectifier	IRF530S
Q2, Q3	2	MOSFET, N-channel, V(BR) > 100 V	Int'l Rectifier	IRF530NS
Q4, Q5, Q6, Q7	−	MOSFET, N-channel, V(BR) > 100 V	Int'l Rectifier	IRF530NS
R1	1	Resistor, 200 kΩ, 0.1 W, 1%	Vishay	CRCW0805−2003F
R2	1	Resistor, 4.99 kΩ, 0.1 W, 1%	Vishay	CRCW0805−4991F
R3	1	Resistor, 3.92 kΩ, 0.1 W, 1%	Vishay	CRCW0805−3921F
R4	1	Resistor, 12 kΩ, 1 W, 5%	Vishay	CRCW2512−123J
R5	1	Resistor, 0.02 Ω, 0.5 W, 1%	Vishay−Dale	WSL−2010 .020<1%
R7, R8	2	Resistor, 20 kΩ, 1 W, 5%	Vishay	CRCW2512−203J
R9, R10	2	Resistor, 0 Ω jumper, 0805	Vishay	CRCW0805−000Z
R12	1	Resistor, 20 kΩ, 0.1 W, 5%	Vishay	CRCW0805−203J
R13	1	Resistor, 30 kΩ, .5 W, 5%	Vishay	CRCW2010−303J
R14	1	Resistor, 1.0 M, 0.1 W, 5%	Vishay	CRCW0805−105J
R15, R16, R17	−	Resistor, 1 W, 1%, 0805	Standard	Standard
S1	1	Switch, slide, SPDT, vertical act., 100 mA	E−Switch	EG1249
S2	1	Switch, toggle, SPDT, PC mount	E−Switch	100SP1T1B1M2QE
SW1	1	Switch, dip, 5 position, SPST	CTS	219−05MS
J1, J2, J3, J4, J5	5	Jack, banana, non-insulated, PC mount	Pomona	3267
J6, J7	2	Header, 2-pin, Single row, 0.10-C, 0.025 square, 0.230 head	Sullins	PTC36SAxN
N/A	4	Spacer, nylon, hex, #6−32, 0.625"	Eagle	14HTSP020
TP7, TP15, TP18 − TP21	6	Jack, test point, black	Farnell	240−333
TP2−TP6, TP8−TP14, TP16, TP17, TP22−TP27	20	Jack, test point, red	Farnell	240−345
N/A	4	Screw, nylon, round head, #6−32, 0.25"	Eagle	010632R025
N/A	1	PCB, FR−4, 2-layer, SMOBC, 5.43" x 3.80", 0.062"	Texas Instruments	HPA021
U1	1	IC, Hot Swap Power Manager for Redundant −48-V Supplies	Texas Instruments	TPS2350PW
U2	1	IC, linear, optocoupler, 30 V, CTR = 0.2 minimum	Fairchild	4N25.S

2.3 TPS2350 −48-V Hot Swap/Supply Selector EVM Operating Specifications

The supply selector EVM is intended to allow some degree of user reconfiguration. This allows designers to set up the circuit to better represent the characteristics of their target application. Potential modifications include changing the current limit threshold, the inrush limiting, the fault timing, and load characteristics. However, under no circumstances should the EVM kit be operated beyond the absolute maximum conditions specified in Table 2.

Table 2. EVM Absolute Maximum Ratings(1)

PARAMETER	MIN	MAX	UNITS
Input voltage range, J2, J3(2)	−100	0.3	V
Input voltage range, J6(3)		30	
Load current, J4		−2.25	A
Load return current, J5		2.25	
Ambient operating temperature range	−40	85	°C

NOTES: (1) Currents are positive into and negative out of the specified terminal.
(2). With respect to the PCB −48V_RTN node at J1.
(3). With respect to the VOUT− node at J5.

As supplied from the factory, the supply selector EVM is configured for operation under the following target conditions, shown in Table 3.

Table 3. EVM Recommended Operating Conditions(1)

PARAMETER	MIN	NOM	MAX	UNITS
Input supply voltage, J2, J3(2)	0	−48	−80	V
Input supply voltage, J6(3)	−1	5	20	
Nominal load current, J4		−1		A
Nominal load return current, J5		1		
Operating temperature range	−40		85	°C

NOTES: (1). Currents are positive into and negative out of the specified terminal.
(2). With respect to the PCB −48V_RTN node at J1.
(3). With respect to the VOUT− node at J5.

3 Getting Started

3.1 Equipment Requirements

The following test equipment is required to use the TPS2350 −48-V hot swap/supply selector EVM .

- Power supply, 80 VDC at 3 A minimum, quantity of two required
- Power supply, 5 VDC
- Oscilloscope
- Digital voltmeter (DVM or DMM)

The individual DIP switches of SW1 are labeled numerically on the PCB silkscreen. Throughout this document, references to the DIP switches (e.g., SW1−1) apply to these screened labels, not to any marking on the switch. However, to determine the ON and OFF positions of the switches, use the labeling on the switch body itself.

3.2 Verifying the EVM Operation

The following procedure steps may be used to verify functional operation of the EVM after receipt.

3.2.1 Equipment Setup

On the EVM, place the POWER and ENABLE switches in the OFF position.

Set the DIP switches 1 through 4 of switch SW1 to the ON position.

Turn on power supply number 1 (PS No. 1) and adjust the output for about 48 V. Turn on power supply number 2 (PS No. 2) and adjust the output for about 44 V. Verify the current limit of supplies 1 and 2 is set to allow sourcing of at least 3 A. Turn off the supplies

Turn on power supply number 3 (PS No. 3), and adjust the output to about 5 V. Turn off the power supply.

Connect the EVM and test equipment as shown in Figure 4.

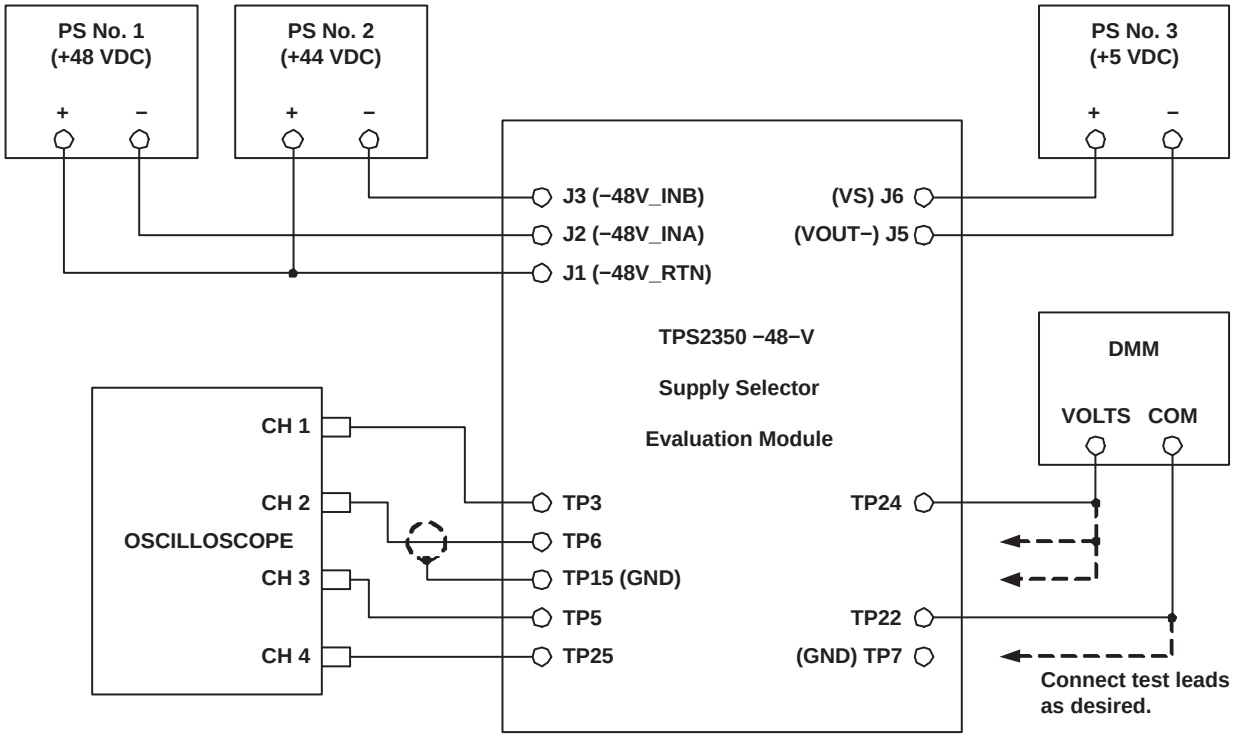

Figure 4. TPS2350 −48-V Supply Selector EVM Equipment Setup

On the oscilloscope, set the channel amplifiers to the following scales:

- CH1: 2 V/div
- CH2: 2 V/div
- CH3: 5 V/div
- CH4: 20 V/div

For easier correlation to the information in this document, the scope trace baselines can be positioned as shown in Figure 5.

Set the scope to trigger on the rising edge of channel 1, at about a 1-V level. Set the scope timebase to 10 ms, and the trigger mode to NORMAL.

3.2.2 Functional Test

Turn on all the power supplies.

On the EVM, place the POWER switch in the ON position. Verify the FAULT LED (D1) remains off. Verify the voltage readings in Table 4 are obtained at the corresponding test points.

Table 4. Test Point Voltages −− Outputs OFF

TEST POINT	REFERENCE	VOLTAGE READING
TP22	TP24/TP25	0 ± 200 mV
J7	TP24/TP25	250 mV max.

Place the ENABLE switch in the ON position. Verify the FAULT LED (D1) remains off. The oscilloscope should have acquired a sweep similar to that shown in Figure 5.

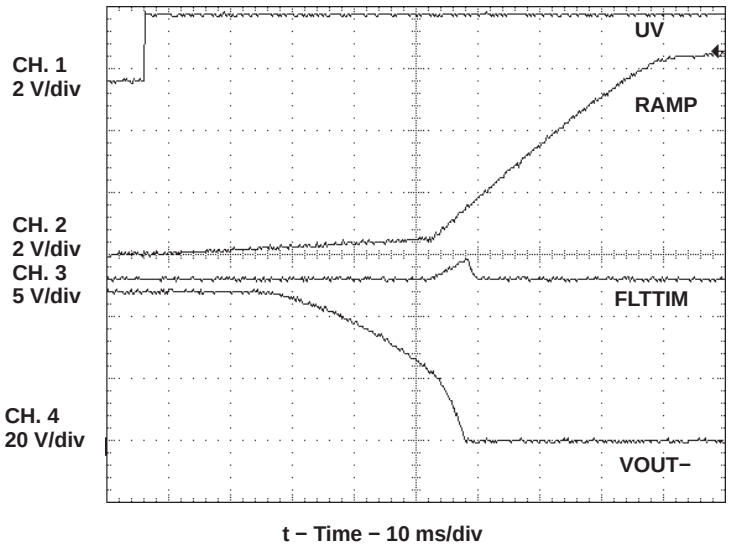

Figure 5. Load Ramp-Up Waveform

The brief fault timing ramp which is shown in Figure 5 (FLTTIM trace) may or may not be present, depending on the actual values of the timing parameters for the particular board being used. If the load voltage ramps to full input potential during the initial reduced rate ramp period, then fault timing does not initiate.

The DMM can now be used to verify that the voltages shown in Table 5 are present at the test points indicated.

Table 5. Test Point Voltages −− Outputs ON

TEST POINT	REFERENCE	VOLTAGE READING
TP22	TP24/TP25	~ Input Supply Voltage
J7	TP24/TP25	4.93 V min.
TP3	TP7	Approx. 2.13 V
TP4	TP7	Approx. 0.94 V

Leave a meter connected across TP22 and TP24/TP25 (i.e., the VOUT terminals). Decrease the voltage of the PS No. 1 supply to be less than 43.5 V. Verify that as the supply is decreased below this voltage, the VOUT voltage remains at the PS No. 2 potential, about 44 V.

Place either the ENABLE or POWER switch (or both) in the OFF position to remove power from the VOUT terminals.

4 Using the EVM Kit to Evaluate the TPS2350

Procedures similar to the steps of Section 3.2.2 for functional test of the EVM can also be used to continue evaluation of the TPS2350 hot swap controller device. Additional details about the EVM features are provided in this section.

4.1 Supply Connections and Test Points

Supply connections to the EVM should be made to the banana jacks as shown in Figure 4. The two backplane, 48-V supplies (PS No. 1 and PS No. 2 in Figure 4) connect between J1 and J2 and J1 and J3, respectively. The polarity of the circuit is such that the HI or (+) outputs of the supplies connect to J1, −48V_RTN. The LO or (−) jacks connect to J2 (−48V_INA) and J3 (−48V_INB). PCB header J6 (VS) is used to connect an external pull-up source when using the MOD_EN output of the EVM. This supply is referenced to the VOUT− node at J5.

The TPS2350 −48-V hot swap/supply selector EVM contains numerous test points located throughout the circuit for waveform monitoring. A list of the EVM test points and their associated signals is given in Table 6.

Table 6. TPS2350 −48-V Hot Swap/Supply Selector EVM Test Points

TEST POINT	SIGNAL NAME	DESCRIPTION
TP2	$\overline{\text{FLT}}$	Load fault output of the TPS2350. On the EVM, this signal drives the red LED.
TP3	UV	Sense input for supply undervoltage detection.
TP4	OV	Sense input for supply overvoltage detection.
TP5	FLTTIM	Fault timing waveform of the TPS2350.
TP6	RAMP	Current ramp control output waveform.
TP7	SOURCE	Common source node of the selection FETs, and reference pin for the TPS2350.
TP8	GATB	Gate drive for the *B* supply selection FET.
TP9	GATA	Gate drive for the *A* supply selection FET.
TP10	SNS	Current sense input for the hot swap controller.
TP11	GAT	Gate drive for the hot swap or pass FET Q1.
TP12	PG	Open-drain, active-high indication of a load power-good condition.
TP13	−VINB	Selection comparator voltage sense input for the *B*−designated supply. On the EVM, this is connected to the −48V_INB jack.
TP14	−VINA	Selection comparator voltage sense input for the *A*−designated supply. On the EVM, this is connected to the −48V_INA jack.
TP15	SOURCE	Secondary test point on the TPS2350 reference node (located near the timing capacitors).
TP16	−48V_RTN	Backplane side of the high side of input power to the board. This node is common to both supplies.
TP17	VOUT+	Additional supply high side test point on the plug-in side of the POWER switch (S2). This is also the input supply to the TPS2350 and the high-side of the load
TP18	−48V_INA	Low side input of the *A*−designated power supply.
TP19		
TP20	−48V_INB	Low side input of the *B*−designated power supply.
TP21		
TP22	VOUT+	High side of switched (load) output power.
TP23		
TP24	VOUT−	Low side of switched (load) output power.
TP25		

4.2 Load Capacitors

Capacitor patterns C8 and C9 are available on the EVM for installation of components to represent the module input bulk capacitance; i.e., the load capacitance seen by the hot swap interface circuit. As supplied from the factory, the EVM contains a 100-μF aluminum electrolytic installed at C8. Further customization to approximate the user's application can be done using either C8 or C9. When installing capacitors in these mounting locations, care should be taken to observe the polarity marking on the PCB silkscreen, and to use appropriately rated capacitors for voltage withstanding. Generally, telecom applications should use 100-V minimum rated capacitors.

Banana jacks J4 (VOUT+) and J5 (VOUT−) are also connected across the output terminals, in parallel with C8 and C9. These jacks can be used to connect additional loads to the EVM board.

4.3 Supply Selector

The TPS2350 device monitors the input supply voltages at −48V_INA and −48V_INB. Using two external N-channel MOSFETs, it selects the supply of larger magnitude for applying power to the back-end plane (the load). Because of this capability, a TPS2350 circuit can be a lower-loss alternative to diodes in traditional diode-OR telecom applications. On the EVM, the selection FETs are Q2 (for supply A) and Q3 (for supply B).

Hysteresis of the supply comparison is set internally to a nominal 400 mV. In order for the TPS2350 to switch over to the deselected supply, its potential must become 400 mV more negative than the supply currently being used.

The selection function can be exercised under various conditions. The voltage levels of the two supplies can be adjusted relative to each other to generate switching events. The supplies can be turned off and back on using their power switches, or they can even be plugged into and removed from their respective jacks J2 and J3. The selection action can easily be viewed at the gates of the selection FETs, TP9 for the *A* supply, and TP8 for the *B* supply. Also, by applying a steady-state load at the output terminals, current probes can be used on the bench supply leads to monitor which supply is delivering power as input conditions are varied. And of course, the load voltage should reflect the magnitude of the selected supply. The scope plot of Figure 6 shows an example of what can be observed using the EVM.

NOTE:

The FET PCB patterns Q4, Q5, Q6, Q7, and certain associated components, are not used on this EVM.

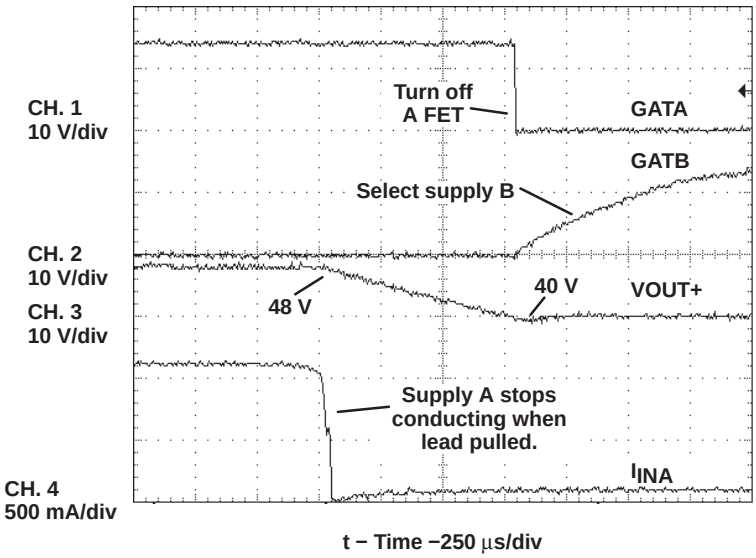

Figure 6. Switching From −48V_INA to −48V_INB Supply

In the Figure 6 plot, the TPS2350 is switchng from the *A* supply to the *B* supply when the initially higher-potential *A* supply lead is rapidly pulled from the input jack. At the time the lead is disconnected, current from that source is interrupted. The bulk capacitor holds up the sense node voltage momentarily (seen here on the VOUT+ trace); however, the 1-A load eventually causes it to decay below the magnitude of the *B* supply, which was 40 V. At this time, the A-channel FET gate is rapidly pulled low, and the B-channel is turned on.

4.4 Changing the Current Limit Threshold

During power-up of a plug-in card, the TPS2350 limits the peak inrush current drawn by the discharged bulk capacitance. The LCA senses load current as the drop across an external sense resistor. Current is regulated by slewing the gate of the pass FET to maintain the voltage drop at an internally set level, nominally 42 mV. Therefore, the peak current level can be established by selecting the appropriate sense resistor value. On the EVM, this resistor is R5. The default value of R5 is 20 mΩ. To modify the current limit threshold, a new sense resistor value can be determined from Equation 1.

$$R5 = \frac{V_{MAX}}{I_{MAX}} \quad (1)$$

where:

- VMAX is the sense voltage limit, and
- IMAX is the desired current limit threshold.

Using the device minimum value of 34 mV for VMAX along with the required minimum load current will ensure that minimum amount of current can always be supplied to the load. For example, a particular line card is expected to draw a maximum of 2.5 A, when the power bus is at its operating minimum level of −33 V, once the card is powered up and operating normally. For this load characteristic, a sense resistor value less than 34 mV/2.5 A, or 13 mΩ, would be selected. A 10-mΩ resistor is generally the closest standard value readily available; smaller values also work, but with a corresponding increase in the maximum current limit.

4.5 Changing the Inrush Slew Rate

The TPS2350 also features slew rate limiting as current is ramped to charge the load capacitance. The slew rate is easily programmed, once the sense resistor is determined, with a small-value capacitor connected between the RAMP and SOURCE pins. The EVM comes equipped with three preset capacitor values, selectable either individually or in combination by closing the appropriate DIP switches of SW1. The default values of the capacitors, and the corresponding nominal slew rates, are given in Table 7.

Table 7. Supply Selector EVM Default Slew Rates

SW1 DIP	REF DES	INSTALLED VALUE	SLEW RATE (A/s)
1	C1	1000 pF	5000
2	C2	0.01 µF	500
3	C3	0.047 µF	106

The EVM can be used to get an illustration of the relationship between current limit, inrush slew rate, load values, and the circuit's fault timing requirements. With DIP switch SW1−1 only closed, the fastest of the preset slew rates is selected, and only the hard-wired timing capacitor C6 is connected to the TPS2350 controller. However, this is sufficient to allow the bulk capacitor C8 to fully charge, from 0 V, across the full range of input supply voltages, down to −80 V. This can be observed by connecting input power as shown in Figure 4, displaying the VOUT− node on an oscilloscope, and enabling the device.

To observe the controller response to a load that does not charge up as expected (a shorted or otherwise excessive load), set switches SW1−1, SW1−2, and SW1−3 to the ON position. This greatly reduces the inrush (load charging) current slew rate at turn-on, with a corresponding increase in the amount of time needed to successfully charge the intended load. Increase the supply level to about 60 V to 72 V, and again enable the device. In this case, the voltage ramp time is excessively long relative to the programmed fault timer; the controller times out and turns off the load.(1) This can be seen from the illumination of the red LED. (The LED may only flash briefly then turn off, indicating load charging ultimately completed on a successive retry.) If this combination represented the parameters of the target plug-in module, then the timing capacitance of C6 and C4 (SW1−4 closed) would be more appropriate. The intended load, in this case, the 100-μF capacitor, can again be charged up on the first attempt, for supply values across the input voltage range.

NOTE: (1)

Due to tolerances of various EVM parameters, some units may not fault out under these conditions. Generally, this is due to the fact that the amount of voltage ramping during the reduced-rate turn-on period will vary from device to device. Some units may be able to charge the load almost completely during this period, when fault timing is inhibited. A more severe load fault is needed to view the fault response. Additional capacitance, or even a resistor, can be connected across the VOUT terminals, J4(+) and J5(−) or at C9. If the user is confident the module is operating correctly, the load can also be shorted out to do this demonstration.

The inrush slew rate can be changed, to better match the application requirement, by replacing any capacitor C1, C2 or C3. The PCB patterns are sized for 0805 ceramic chip capacitors. Use equation 2 to calculate the new ramp capacitor, C_{RAMP}, value in microfarads.

$$C_{RAMP} = \frac{11.3}{100 \times R5 \times (di/dt)_{MAX}} \quad (2)$$

where:

- R5 is the selected sense resistor value, in ohms, and
- $(di/dt)_{MAX}$ is the desired maximum slew rate, in amps/second.

4.6 Fault Timing with the TPS2350

Whenever the hot swap controller is limiting current to the load, an on-chip timer is monitoring this operation against an established time limit. The timeout period is generated by the constant-current charging of a capacitor at the FLTTIM pin. If current regulation ceases prior to expiration of the timer, the capacitor is discharged, and normal steady-state operation of the load either starts or resumes. However, if the timer expires, then the pass FET is turned off, disabling power to the load, and the $\overline{\text{FAULT}}$ output is asserted.

On the TPS2350 −48-V hot swap/supply selector EVM, several capacitor patterns are provided for adding to or otherwise modifying the timeout period. Capacitor C6 is hard-wired to the device FLTTIM pin, and provides a minimum fault timer for the default load. C4 and C5 can be switched into the circuit via DIP switches SW1−4 and SW1−5, respectively. The EVM ships from the factory with a 0.1-µF capacitor installed at C4; C5 is not populated for easier subsequent user modification as required.

If the target application requires fault timing other than provided by the default EVM setup, a new value of timing capacitor can be calculated from equation 3. When selecting from the readily available capacitor values for the equation 3 result, default to a slightly larger, rather than smaller, capacitor.

$$C_{FLT} = \frac{54 \times t_{FLT}}{3.75} \quad (3)$$

where:

- C_{FLT} is the calculated value in microfarads, and
- t_{FLT} is the desired timeout period in seconds

4.7 Programming the UVLO and OVLO Thresholds and Hysteresis

The UV and OV pins can be used to set the circuit undervoltage and overvoltage thresholds (V_{UV} and V_{OV}, respectively). When the input supply is below V_{UV} or above V_{OV}, the GAT pin is held low, disconnecting power from the load, and the PG output is deasserted. When input voltage is within the UV/OV window, the GAT drive is enabled, assuming all other input conditions are valid for turn-on.

Threshold hysteresis is also externally programmable. Internal current sources are switched to the UV and OV pins whenever the corresponding input voltage exceeds the nominal 1.4-V reference.

On the EVM, the V_{UV} and V_{OV} thresholds are individually programmed via the three-resistor divider R1, R2, and R3 (refer to Figure 2). The factory-installed resistor values result in the following nominal voltage thresholds.

Table 8. Nominal UVLO and OVLO settings.

PARAMETER	DESCRIPTION	VALUE (V)
V_{UV_L}	UVLO threshold, supply low ($V_{IN} < V_{UV}$)	32.8
V_{UV_H}	UVLO threshold, supply high ($V_{IN} > V_{UV}$)	30.8
V_{OV_L}	OVLO threshold, supply low ($V_{IN} < V_{OV}$)	72.6
V_{OV_H}	OVLO threshold, supply high ($V_{IN} > V_{OV}$)	70.5

The thresholds are easily modified by changing the resistor values. When the desired trip voltages and the UV hysteresis have been established for the protected load, new values are determined as follows. Generally, the process is simplest by first selecting the top leg of the divider (R1) needed to obtain the desired hysteresis. This value is calculated from equation 4.

$$R1 = \frac{V_{HYS\_UV}}{10\ \mu A} \tag{4}$$

where V_{HYS_UV} is the desired amount of undervoltage hysteresis.

Once a value for R1 is selected, it is used to calculate R2 and R3 using equations 5 and 6.

$$R2 = \frac{1.4 \times R1}{\left(V_{UV\_L} - 1.4\right)} \times \left[1 - \frac{V_{UV\_L}}{\left(V_{OV\_L} + 10^{-5} \times R1\right.}\right] \tag{5}$$

$$R3 = \frac{1.4 \times R1}{\left(V_{UV\_L} - 1.4\right)} \times \left[\frac{V_{UV\_L}}{\left(V_{OV\_L} + 10^{-5} \times R1\right.}\right] \tag{6}$$

where:

- V_{UV_L} is the UVLO threshold when the input supply is low; i.e., less than V_{UV}, and
- V_{OV_L} is the OVLO threshold when the input supply is low; i.e., less than V_{OV}

4.8 TPS2350 Powergood Output (PG)

The supply selector EVM features two nodes to access the powergood status generated by the TPS2350. For simply monitoring, for example with a scope probe, the actual output signal itself is available at test point TP12.

The MOD_EN output at J7 demonstrates an isolated signal interface using an opto device. An example application of such a signal is to drive the enable input of downstream converters. As such, this output is referenced to the VOUT− node, as this would be the low side of input power to the brick. The EVM schematic shows the circuit details. The MOD_EN assertion level is active-high. The use of this signal requires a pull-up source at the VS input, J6. See Tables 2 and 3 for the requirements of the VS supply.

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