Application Report
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Protecting Radio, Baseband and Active Antenna Systems with TPS2352x Hot Swaps

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ABSTRACT

Technological advancements in radio units and antenna systems have pushed the semiconductor industry to develop improved power management solutions to support these higher power systems. One of these power management solutions, the hot swap controller, is a critical component that provides fault protection for the rest of the system. This application note will highlight some common challenges with current hot swap design and provide solutions to these challenges with the TPS2352x family.

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Trademarks

1 Introduction

Every generation of mobile telecommunications has introduced new improvements and features. 1G created the first mobile phones, 2G introduced SMS text messages, 3G enabled wireless internet access, and 4G LTE increased data rates five-fold. In the future, increasing user demand for higher bandwidths and capacity will continue to drive advancements in active antenna systems, radio units and other telecommunication systems.

However, these upgrades are not without cost. To implement many of these features, systems would need to consume higher amounts of power which makes optimization and efficiency crucial. In addition, the need for continuous connectivity in harsh operating environments puts challenging requirements on these systems to avoid resets during transient events. The hot swap protection circuit, in particular, is an area that is challenging to design due to these requirements.

In remote radio units (RRU), baseband units (BBU) and active antenna systems (AAS), hot swap controllers are almost universally placed at the –48 V input of the power subsystem. The purpose of this application note is to explain three traditional hot swap design challenges and how TI's TPS2352x family of –48 V hot swap controllers addresses these issues. These issues are: inefficient paralleled MOSFET design, oversizing MOSFETs due to poor safe operating area (SOA) utilization and slow transient recovery.

2 Optimizing Paralleled Power MOSFET Design

The biggest challenge in any hot swap design is ensuring that the power MOSFETs remain in their safe operating area (SOA) in all scenarios. As power levels have increased over time, large power MOSFETs with strong SOAs have been configured in parallel to support higher currents. Figure 1 shows a general schematic with two MOSFETs placed in parallel for simplicity. However, when more MOSFETs are placed in parallel, the total on resistance (R_{DSON}) and total thermal dissipation decrease proportionately. In this common architecture, the gates of all the MOSFETs would be connected to a single gate drive on the hot swap controller.

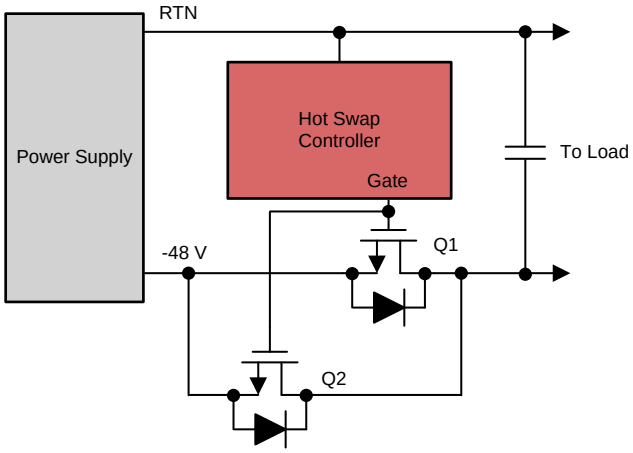

Figure 1. Hot Swap Controller with Two Power MOSFETs in Parallel

Often times, this creates an issue. During start-up, the gate drive will attempt to power up the MOSFETs simultaneously but due to parasitic gate threshold differences between MOSFETs (which can be greater than 2V), there is no guarantee that they will begin conducting at the same time. On top of that, the MOSFETs will draw more current at high temperature when operated at a low V_{GS}. As a result, the MOSFET that initially draws more current will get hotter and draw even more current leading to a greater imbalance in current sharing between the MOSFETs. This will continue until both MOSFETs are fully turned on. (For more information, please read "Robust Hot Swap Design").

While this may not seem like an issue, the stress exerted on these MOSFETs during startup can be significant. Since it's difficult to determine which MOSFET will be taking the bulk of the stress due to the variable gate thresholds, every MOSFET in parallel must have a strong enough SOA to survive the event as if it were the only MOSFET handling the power. On a similar note, fault events such as short circuits on the output also exert large amounts of stress on the MOSFETs, so designers need to ensure that the MOSFETs remain in their SOA during this condition as well.

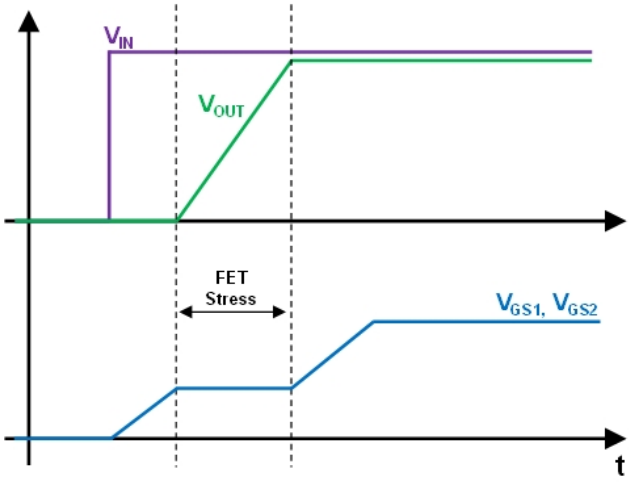

Figure 2. Start Up

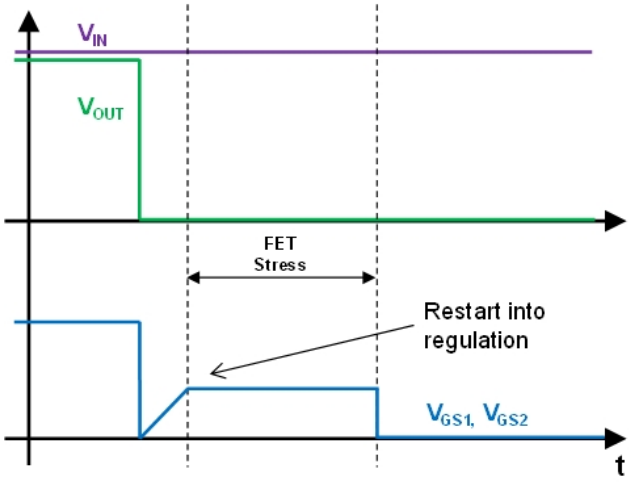

Figure 3. Hot Short

In our basic two MOSFET example, Figure 2 and Figure 3 depict the MOSFET stress during start up and during a hot short circuit event. To survive these events, both MOSFETs require strong SOA which usually means larger packages and higher costs. With more MOSFETs in parallel, this cost and size can quickly compound.

2.1 Dual Hot Swap Gate Drive

The TPS23521 and TPS23523 hot swap controllers address this issue by adding an independent, second gate drive shown in Figure 4. The addition of GATE2 allows the second MOSFET (Q2) and any other paralleled MOSFETs to power up after the MOSFET on GATE (Q1) is fully on. This ensures that only the Q1 MOSFET is exposed to stresses during power up, hot short and other stressful events.

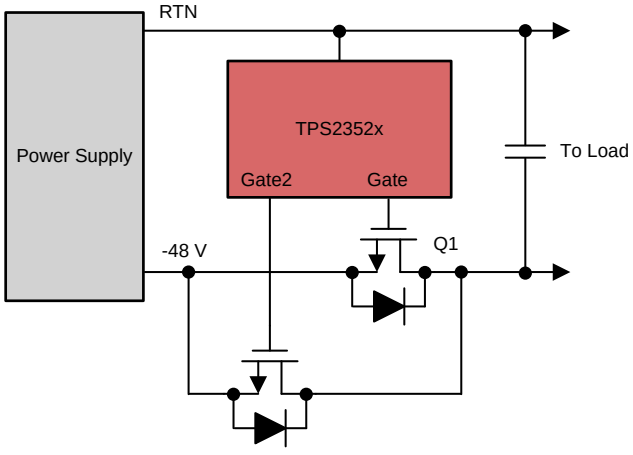

Figure 4. Dual Gate Drive with Two Power MOSFETs in Parallel

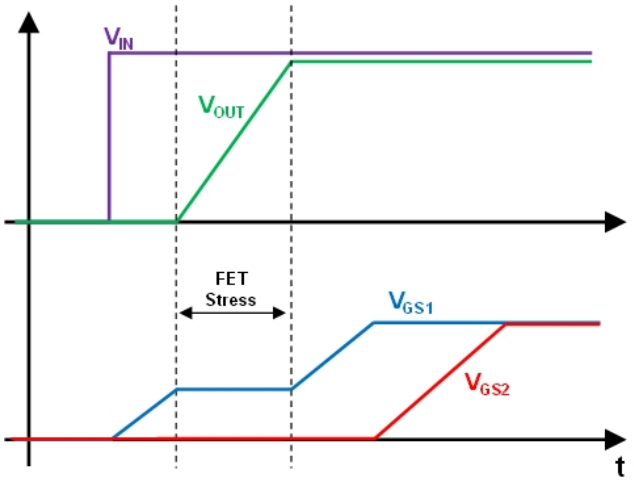

Figure 5. TPS2352x Start Up

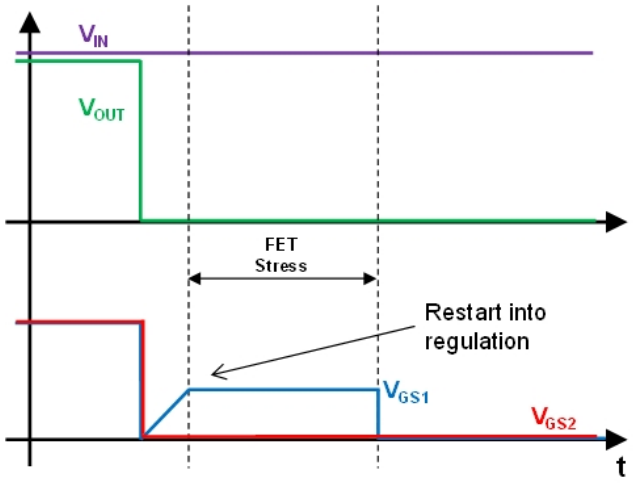

Figure 6. TPS2352x Hot Short

For example, during start up in Figure 5, Q1 would begin to turn on and conduct current while Q2 is fully off. Once Q1 conduction begins, current begins to flow and Q1 begins to take on stress as output voltage ramps. After Vout ramps to the maximum level, Q1 continues to increase its gate-source voltage until it reaches a threshold of 7.25 V (typical). It is only after this point that Q2 and all the additional MOSFETs turn on.

When a hot short circuit occurs, all MOSFETs turn off within 300 ns. Immediately after, the Q1 MOSFET slowly turns back on to determine if the short is still present. If the short circuit remains, the hot swap will enter regulation mode for a configurable fault time and then the Q1 MOSFET will turn off. Q2 does not turn back on until the fault is removed and startup stress has passed.

In summary, with the dual gate drive feature, only one MOSFET needs to have strong SOA since only one MOSFET will be exposed to harsh stresses. All additional MOSFETs can be connected to the second gate drive which would only power up after the first MOSFET is enhanced. Since the additional MOSFETs do not require strong SOA, designers can choose these MOSFETs to optimize R_{DSON}, cost and space.

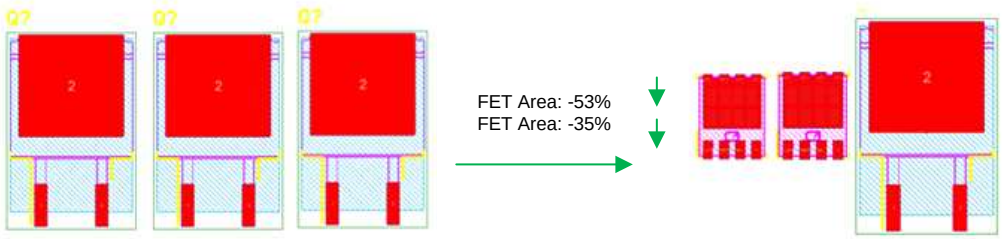

Figure 7. Dual Gate Drive Saves Space and Cost by Using Smaller MOSFETs. Instead of Three D2PAK MOSFETS, Only One is Required.

Table 1. Comparison of MOSFETS. For a single gate drive, all MOSFETs would need strong SOA (PSMN4R8). With dual gate drive, Only one MOSFET requires strong SOA.

	PSMN4R8-100BSEJ	CSD19532Q5B
V_{DS} Rating (V)	100 V	100 V
R_{DSON}, max (mΩ)	4.8	4.9
R_{DSON}, max at 125°C	9.6	8.82
10 ms, 70 V SOA (W)	260	70
10 ms, 10 V SOA (W)	800	200
Package	D2PAK	SON

Table 1. Comparison of MOSFETS. For a single gate drive, all MOSFETs would need strong SOA (PSMN4R8). With dual gate drive, Only one MOSFET requires strong SOA. (continued)

	PSMN4R8-100BSEJ	CSD19532Q5B
Size	15 mm × 10 mm	5 mm × 6 mm
Price (1ku)	$1.90	$0.89

3 Maximizing Power Efficiency and MOSFET SOA

One of the most important features in any hot swap protection circuit is limiting the current to safe levels. If the current limit is not properly managed, the power MOSFET, sensitive integrated circuits and other components can be damaged during unwanted overcurrent conditions. Many hot swap controllers allow the user to set a current limit threshold. Once the MOSFET current exceeds this threshold, the hot swap will either decrease the gate voltage of the MOSFET to regulate the current back to the threshold, or open the MOSFET completely and stop all current from flowing.

3.1 Single Current Limit

While this current limit threshold is usually adjustable, it does not allow for full utilization of a power MOSFETs SOA.

Let's take a look an example with a PSMN4R8-100BSE MOSFET. Our example system has a $V_{IN,\ MAX}$ of 72 V and the fault timer of our hot swap controller is set to be 10 ms. Below is the PSMN4R8-100BSE power MOSFET SOA curve at 25°C.

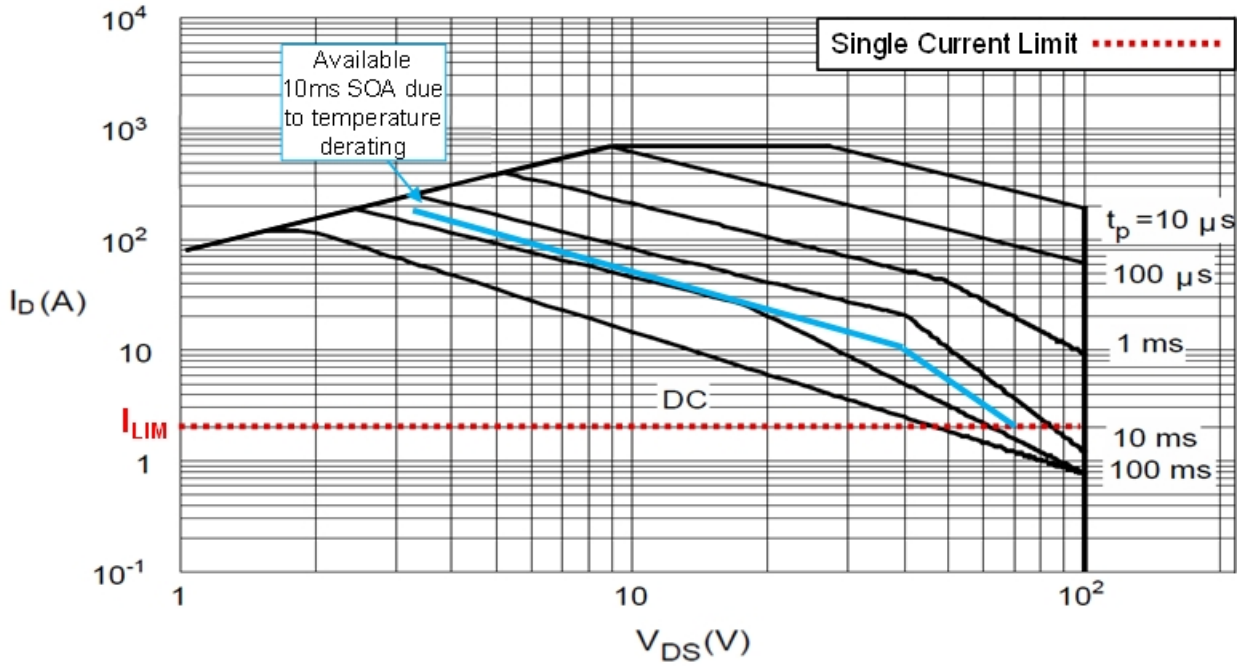

Figure 8. PSMN4R8-100BSE SOA with Single Current Limit

Since the fault timer has been set at 10 ms, the SOA of interest is the one for a 10 ms pulse (third curve from the bottom). Since this curve is taken at 25°C, we must decrease the SOA by 50% to account for temperature derating. The resulting "Available 10 ms SOA" is approximated by the blue curve. As we can see from this plot, the current should not exceed 2 A at 72 V or it would violate the SOA and damage the MOSFET. Therefore, current limit should be set at 2 A (dotted red line).

While a single current limit of 2 A would enure that the MOSFET stays in its SOA for a $V_{IN,\ MAX}$ of 72 V, it does not make good use of the MOSFETs SOA at lower V_{DS}. For example, when the MOSFET is fully enhanced , the R_{DSON} and V_{DS} will both be low. In this range, the MOSFET can safely pass more current. However, the actual current would be capped by the current limit (in this case, 2 A) even if the entire system can handle higher power. Therefore, having just a single current limit is an inefficient solution.

3.2 Power Limit

A better solution to the single current limit issue is a feature called power limit. Power limit measures the V_{DS} and current through the MOSFET to ensure that the total power does not exceed a given pre-programmed threshold. Power limit also includes a single current limit that is active at low V_{DS}. At higher V_{DS}, power across the MOSFET increases and power limit ensures that the $V_{DS} \times I_{DS}$ doesn't exceed its pre-programmed threshold.

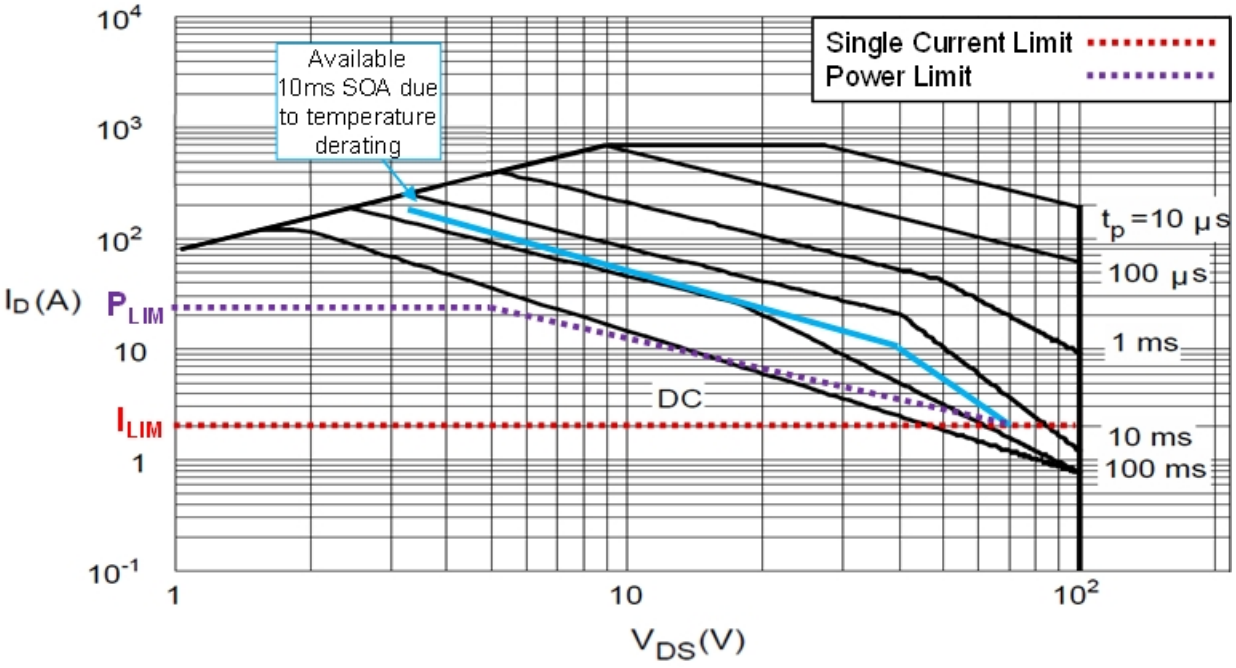

Figure 9. PSMN4R8-100BSE SOA with Power Limit

The purple curve above shows the current limit to be set at 25 A with the power limit (P_{LIM}) at 130 W. This solution makes significantly better use of the MOSFET's SOA compared to the single current limit while still maintaining proper protection for the MOSFET. In this example, the power limit solution allows the MOSFET to pass approximation 5 V_{DS} at 25 A before regulating. However, if there were a larger V_{IN} step such that V_{DS} exceeds 6 V, the Hot Swap would begin to regulate the MOSFET. There are two scenarios where this would be an issue.

During normal operation, an intentional V_{IN} step from –48 V to –60 V would create a transient drop of 12 V_{DS} shown in Figure 10. If the load was drawing 20 A of current, the power across the MOSFET would reach 12 × 20 A = 260 W which exceeds the power limit threshold. Although this does not exceed the SOA of the MOSFET, the Hot Swap will begin to power limit and potentially shut off the device.

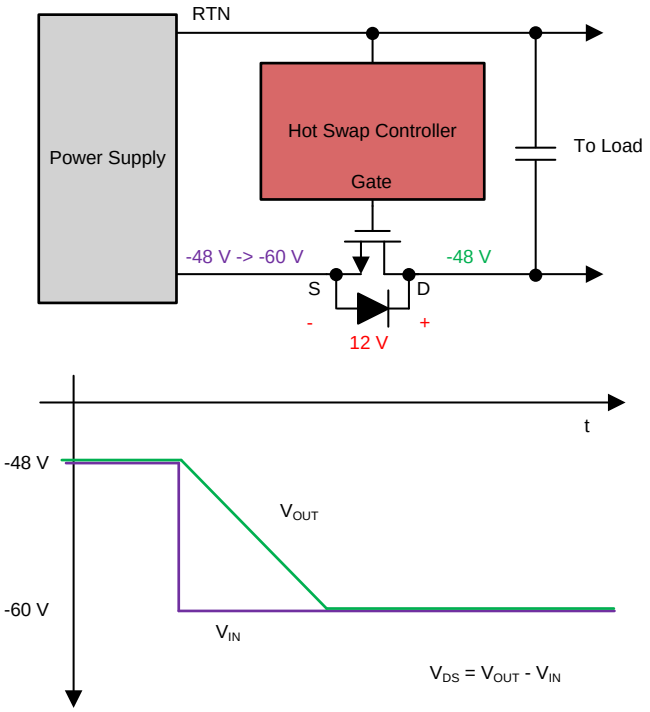

Figure 10. V_{IN} Step Causes Large V_{DS}

Another scenario would be during brownouts. During brownout faults, the input voltage would drop suddenly to zero and restart back to the original voltage level in a short period of time. During the dead time when input voltage is 0 V, the output would decay based on I = C*dV/dt. Once the input voltage returns, there will be a large transient V_{DS} drop across the MOSFET similar to the input voltage step scenario.

In these scenarios, the SOA of the MOSFET is not violated so it would be beneficial for the Hot Swap to pass this transient instead of regulating.

3.3 Dual Current Limit

The TPS2352x family addresses the shortcomings of single current limit and power limit by implementing a dual current limit feature. Dual current limit allows the user to program two current limit thresholds (one at higher V_{DS} and one at lower V_{DS}) along with the voltage threshold where the switch occurs.

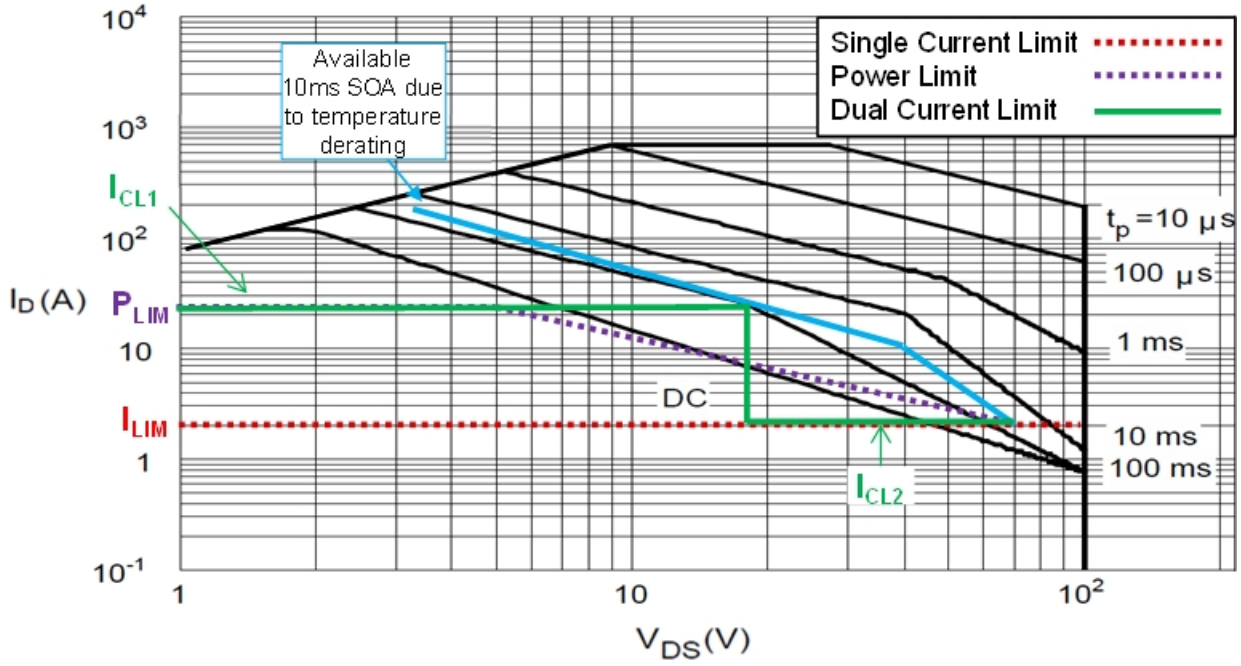

Figure 11. PSMN4R8-100BSE SOA with Dual Current Limit

By setting a higher current limit (I_{CL1}) at lower V_{DS}, the MOSFET's SOA utilization is maximized to pass higher current and higher power during full enhancement. Dual current limit also has better transient performance than power limit during brownouts and VIN steps since it maintains I_{CL1} to a higher V_{DS} voltage. As a result, the MOSFET will not regulate unncessarily when SOA boundaries are not violated. When higher voltages are dropped across the MOSFET, it cannot be exposed to the same current levels at lower V_{DS}. To address this, a programmable switchover threshold ($V_{DS,\ SW}$) will implement the lower current limit (I_{CL2}) at high V_{DS} to ensure the power remains within the MOSFETs SOA.

These dual current limits (I_{CL1}, I_{CL2}) and switchover threshold ($V_{DS,SW}$) can be configured by selecting the appropriate R_{SNS} and R_D resistors.

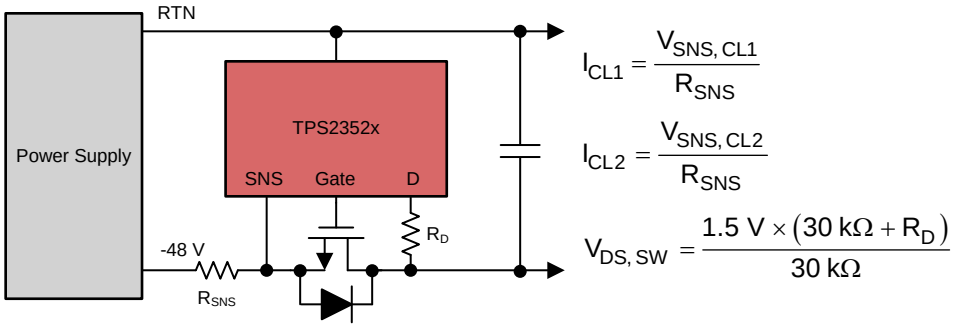

Figure 12. Dual Current Limit on TPS2352x

4 Hot Swap Transient Recovery

In harsh operating environments, lightning strikes, inductive coupling and other events can cause transients surges at any time. While a hot swap must first and foremost protect the system against these events, how it recovers after the transient passes is also crucial. For example, if lightning strikes a radio unit, the hot swap must be able to disconnect and shield the system from this event with minimal delay. However, if the hot swap does not reconnect right after the transient has passed, the system could shut off due to lack of power.

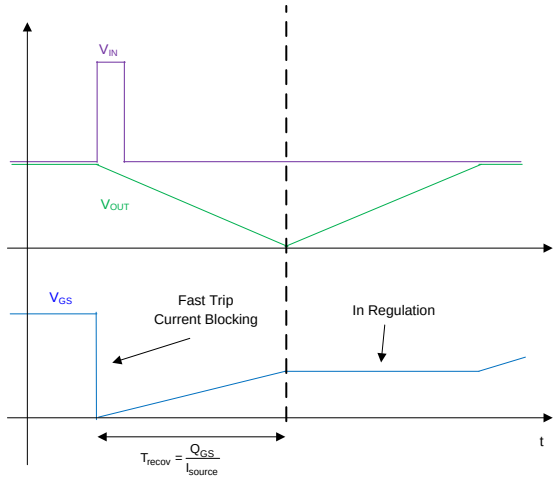

Figure 13. V_{OUT} Droop Due to Transient Recovery Time

When a transient exceeds a fault threshold in typical hot swap applications, the hot swap will immediately pull down the MOSFET gate voltage to prevent the transient from reaching the system. Since power is also disconnected from the system, V_{OUT} will begin to discharge. During this time period, the hot swap will begin sourcing current to the MOSFET gate to bring V_{GS} back up to the V_{GS} threshold required to turn on the MOSFET. If the transient has passed, the MOSFET will turn back on and V_{OUT} will rise back to its pre-transient level. During this recovery period, it is critical that V_{OUT} does not droop past a certain level or the system could shut down due to lack of power. Since V_{OUT} droop is directly correlated to the time it takes for the MOSFET to turn back on, T_{RECOV} should be minimized.

There are two ways to minimize the recovery time (T_{RECOV}) which is given by the equation below:

$$T_{RECOV} = \frac{Q_{GS}}{I_{SOURCE}} \quad (1)$$

One way to minimize the recovery time is to increase the gate sourcing current (I_{SOURCE}). The stronger the gate sourcing current, the faster the MOSFET will restart after a transient and minimize drooping on V_{OUT}.

The second way is to decrease Q_{GS} which is the gate charge required to turn on the MOSFET. Many hot swaps today have large capacitors on the gate to provide soft starting capabilities to manage inrush current and output voltage rise time (shown in Figure 14). These gate capacitors are important because they provide a controlled output rise time and limit inrush current as to not exceed the MOSFET SOA or damage downstream circuitry. However, after start up, these capacitors also increase the Q_{GS} which in turn proportionately increases the transient recovery time.

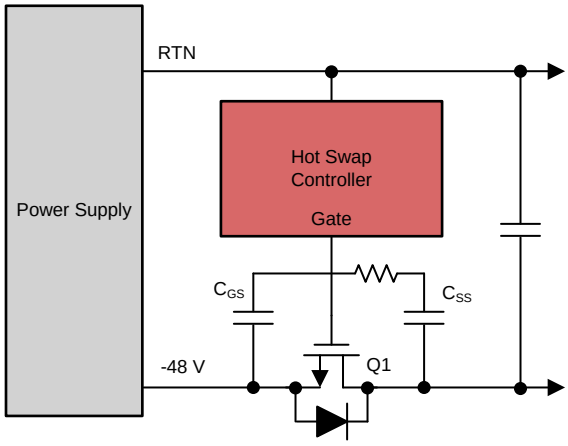

Figure 14. Soft Start Capacitors on MOSFET Gate

4.1 Gate Sourcing Current

The TPS2352x family optimizes transient recovery by increasing I_{SOURCE} and decreasing Q_{GS}.

During regular start up state, the TPS2352x sources 20 µA of current to the MOSFET gate to assist with soft start. After the MOSFET turns on, the hot swap enters the “normal operation” state and the gate sourcing current increases to 400 µA shown in Figure 15. When transient fault occurs, the MOSFET will turn off but the hot swap remains in the normal operation state for a deglitch time. During this time, the source current remains at 400 µA to charge the gate voltage quickly. Compared to a typical hot swap sourcing current of 40-50 µA, the strong sourcing current of the TPS2352x reduces recovery time and output voltage droop tenfold.

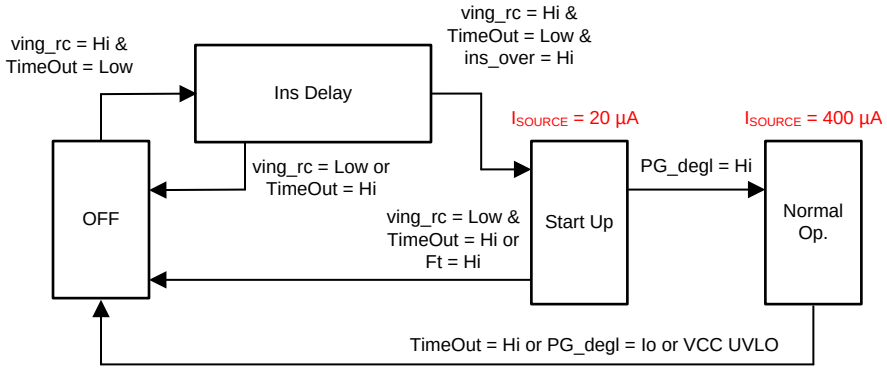

Figure 15. TPS2352x State Diagram

4.2 Soft Start Disconnect

As mentioned earlier, soft start capacitors on the gate are typically used to control output voltage rise time and manage inrush current. However, these capacitors deteriorate transient recovery by slowing down the time it takes for the MOSFET to turn off (since the capacitors need to be discharged) and slowing down the time it takes the MOSFET to turn back on after the fault (since the capacitors need to be recharged).

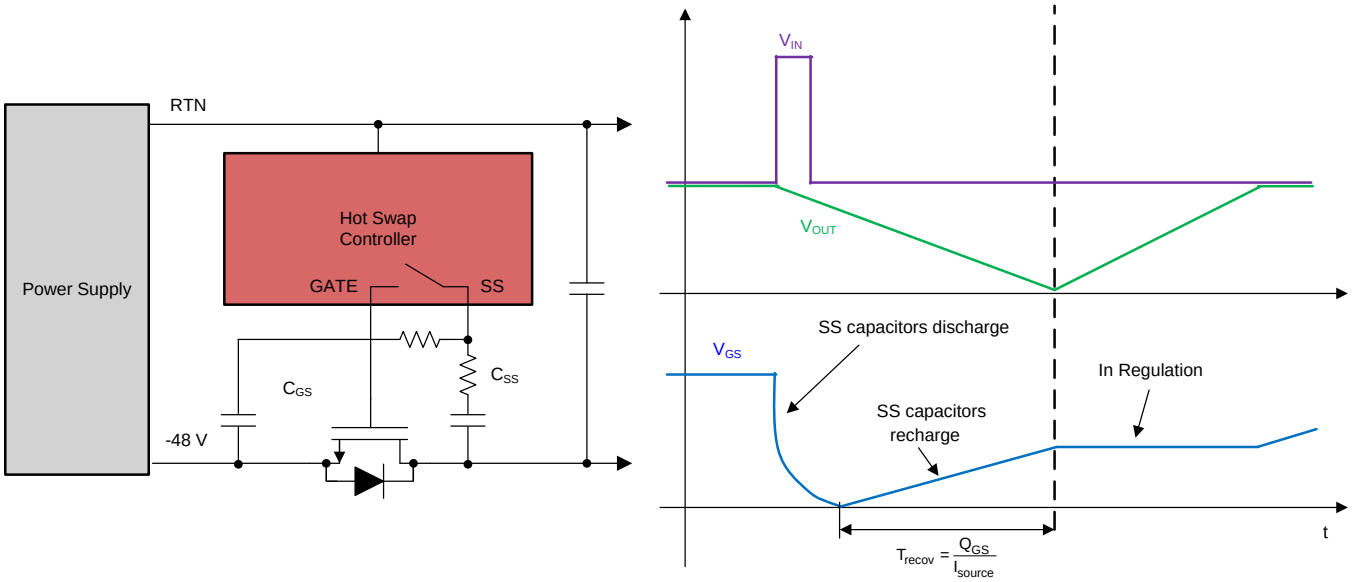

Figure 16. Soft Start Capacitor Effects on Transient Performance

In the TPS2352x, the soft start capacitors are initially connected to the gate during startup but are disconnected in normal operation. This “soft start disconnect” feature combines the protection and inrush management benefits of traditional soft start circuitry with improved transient response during a fault. Since the capacitors are no longer connected when transients occur, the Q_{GS} decreases and transient recovery time improves.

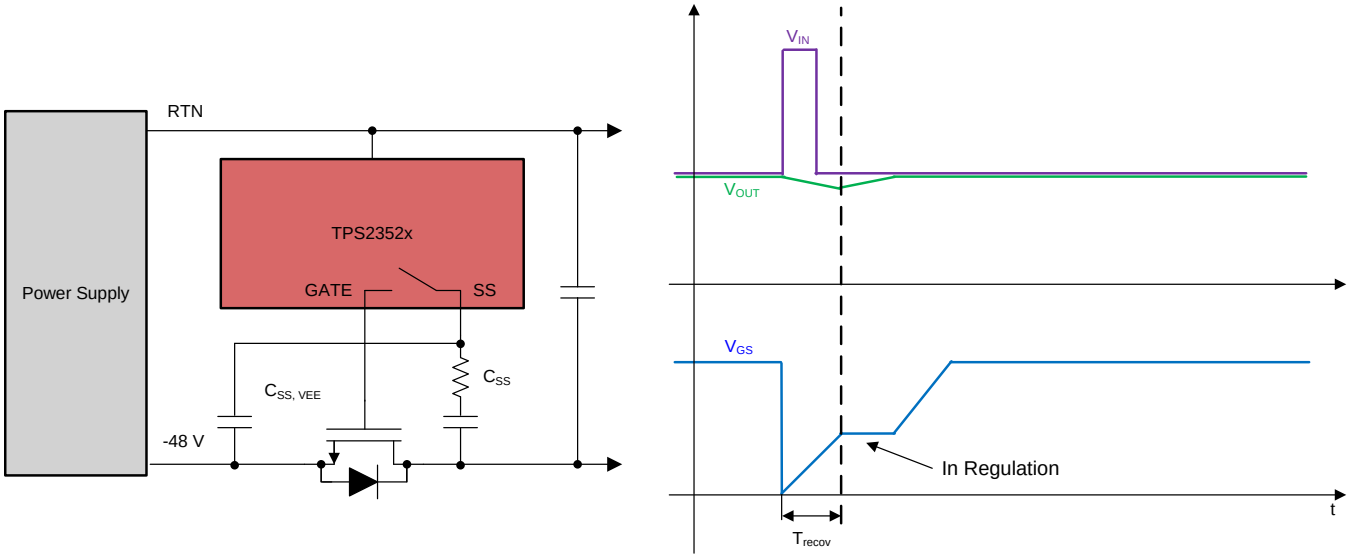

Figure 17. Improved Transient Response with Soft Start Disconnect

By incorporating a strong sourcing current of 400 uA along with soft start disconnect, the TPS2352x optimizes transient recovery to minimize output voltage droop.

5 LM5067 vs TPS2352x Performance Comparison

This section compares the performance of the LM5067, a popular –48 V hot swap controller with the TPS2352x.

The test conditions are given below:

LM5067

- C_{OUT}= 550 µF
- I_{LIM}= 12.5 A
- P_{LIM}= 75 W
- Timer = 27.52 ms (2x typical start time)

TPS2352x

- C_{OUT}=550 µF
- I_{LIM}=12.5 A
- C_{SS}=33 nF (Output dV/dt=0.6 V/ms)
- $C_{SS,VEE}$=100 nF

5.1 Start Up

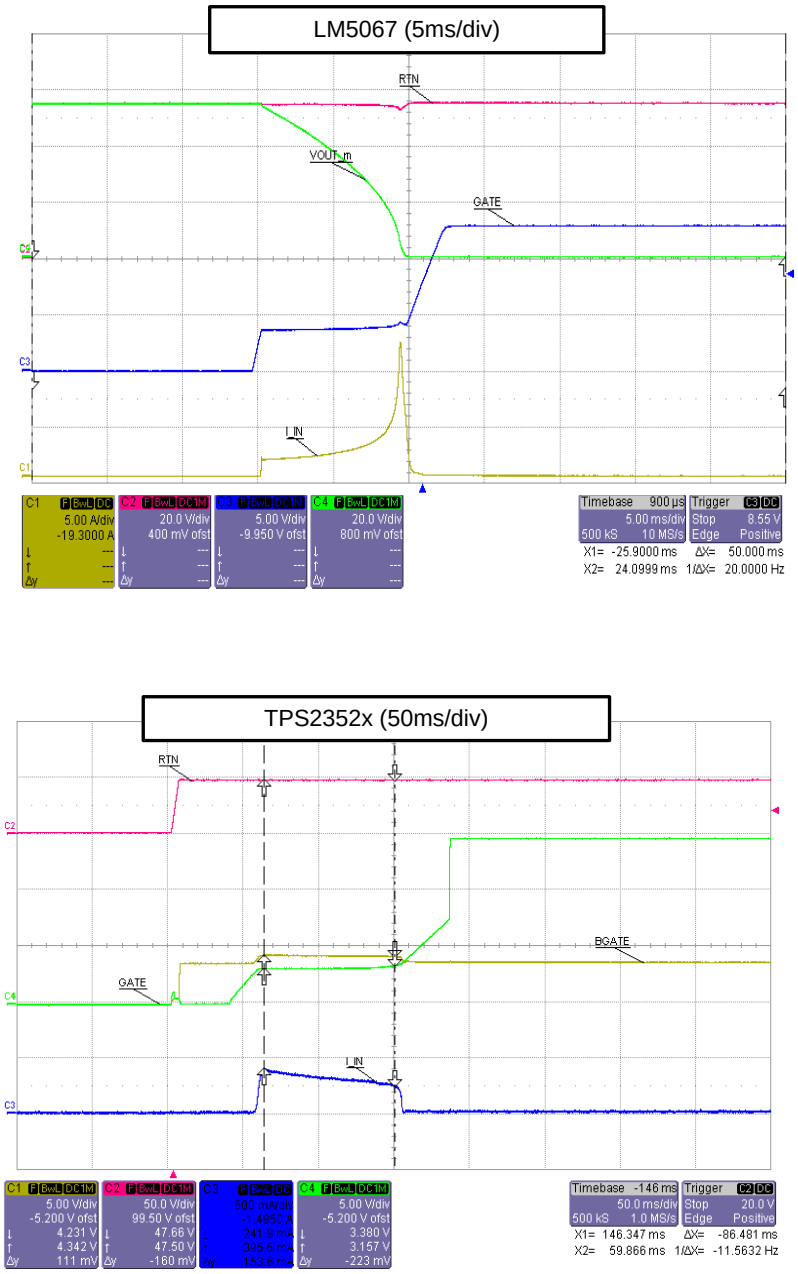

Figure 18. Start Up

On start up, approximately 1.5 A of input current flows through the LM5067 MOSFETs while only 0.4 A flows through the TPS2352x MOSFETs.

5.2 Start Up into Short

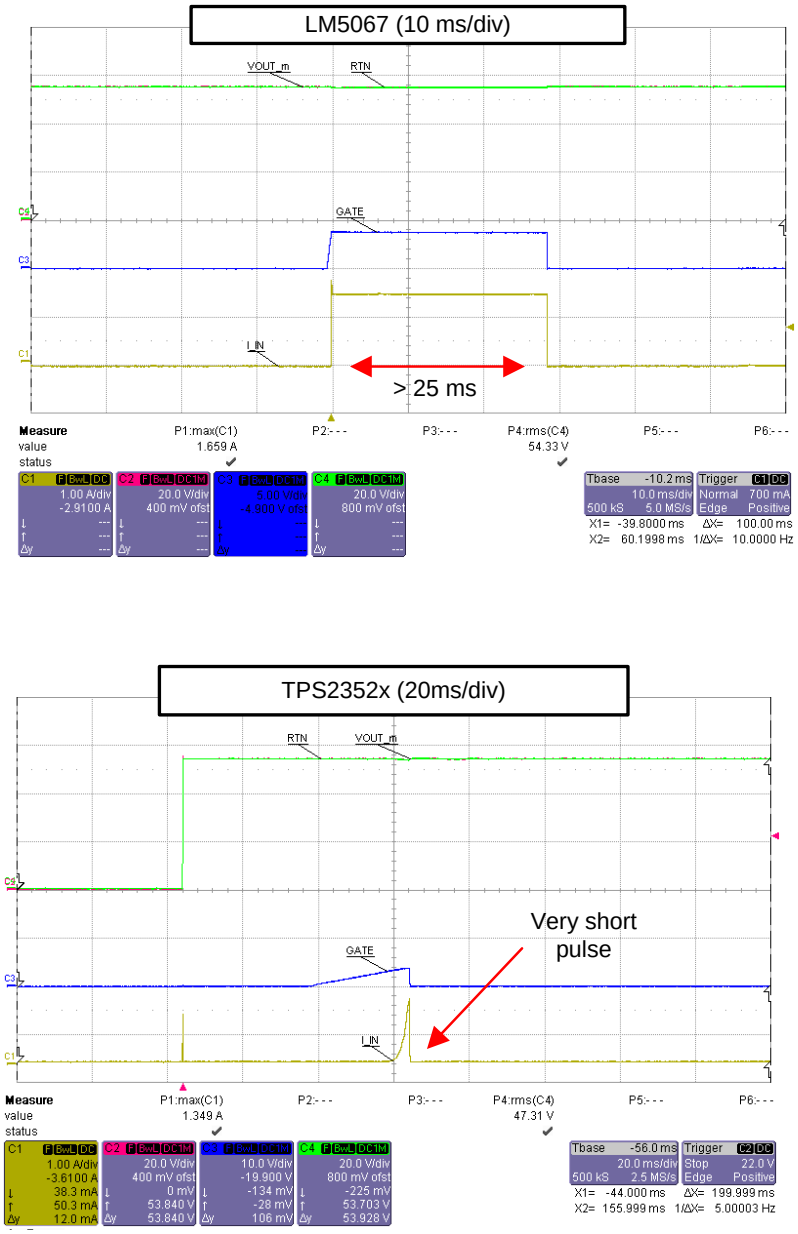

Figure 19. Start Up into Short

The TPS2352x's dual current limit feature allows the current limit to be set to 1.5 A. This allows the hot swap to have a short timer and as a result, the MOSFET is less stressed during a start up into a short circuit. In contrast, the LM5067 MOSFET is exposed to 1.5 A for 25 ms since the timer must be set for 2x the typical start time for margin.

5.3 Hot Short

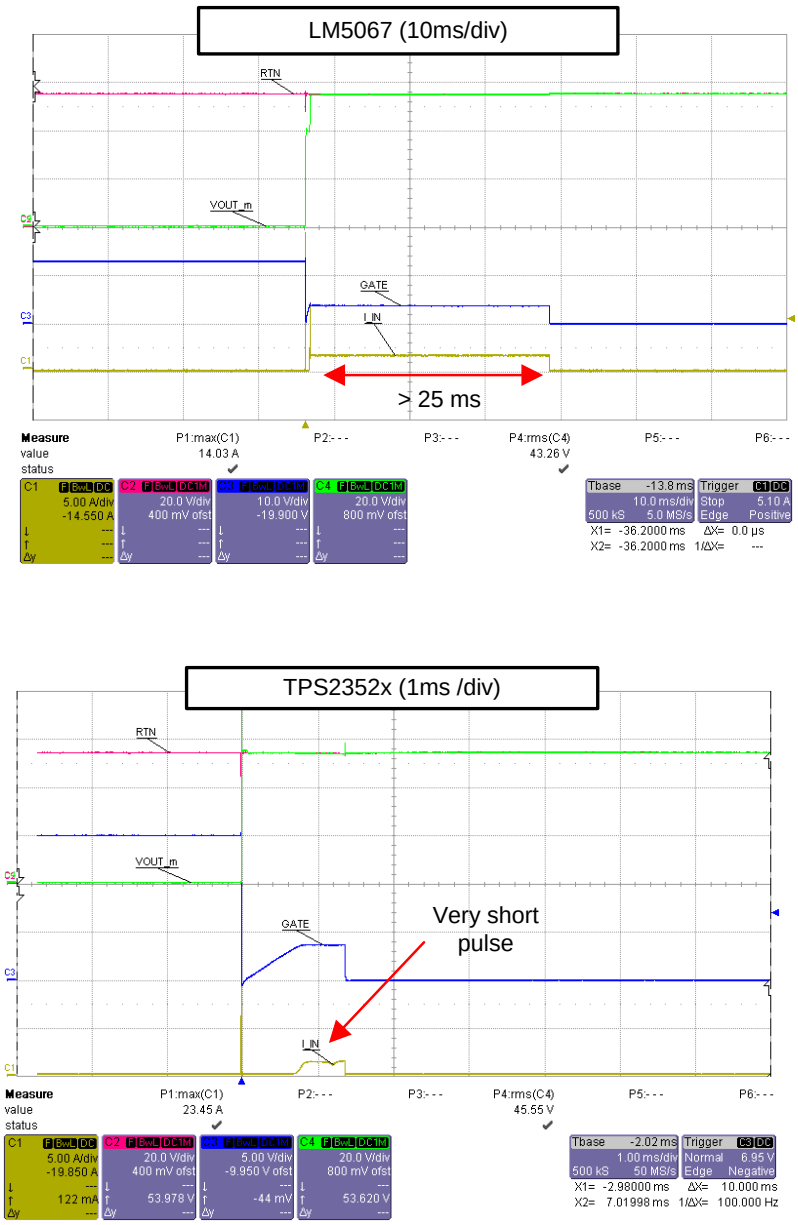

Figure 20. Hot Short

When a hot short occurs in normal operation, the TPS2352x MOSFETs are again exposed to significantly less power than the LM5067 MOSFETs.

5.4 V_{IN} Step and Transient Response

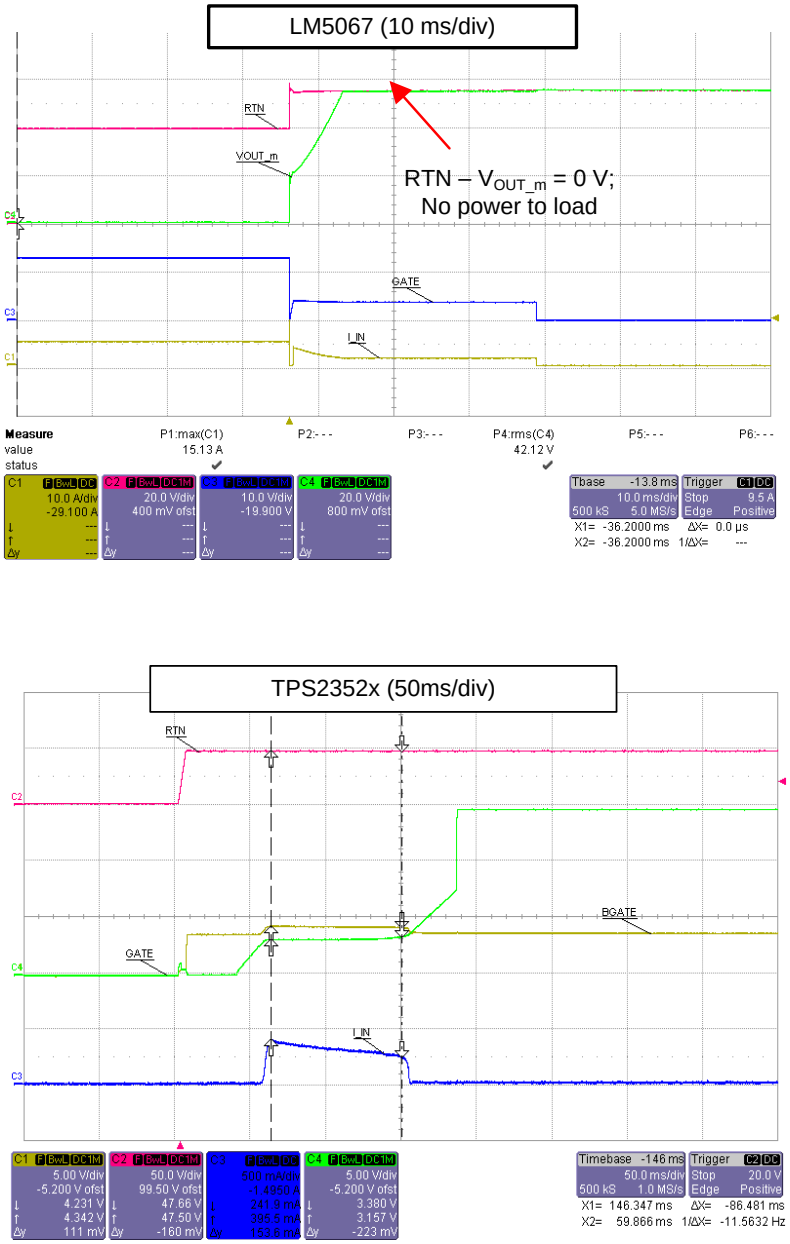

Figure 21. V_{IN} Step and Transient Response

When V_{IN} steps from –40 V to –55 V, the system shuts down with the LM5067 since the hot swap was unable to reconnect power back to the system before V_{OUT} drooped below a critical level. In contrast, the strong sourcing current, soft start disconnect and dual I_{LIM} of the TPS2352x minimize output voltage droop and keeps the system on during transients.

6 References

- *Robust Hot Swap Design* (SLVA673A)
- TPS23521 Datasheet, December 2017
- TPS23523 Datasheet, December 2017
- TPS23525 Datasheet, December 2017
- PSMN4R8-100BSE Datasheet, NXP Semiconductors, 4/12/2013

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