Practical Guidelines to Designing an EMI Compliant PoE Powered Device with Non-Isolated DC/DC

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DC/DC converters used in Powered Device (PD) applications can be sources of conducted and radiated emissions. The PD should employ design techniques to mitigate or eliminate potential emissions associated with its DC/DC converter. This application report presents some practical guidelines that can be followed to obtain an EMI compliant PD. These guidelines are illustrated by working through an actual design example of a non-isolated buck converter employing the Texas Instruments TPS23750. The TPS23750 includes an IEEE 802.3-2005 compliant PD front-end and a DC/DC controller. Refer to datasheet SLVS590 and user's guide SLVU136 for more information on using the TPS23750.

1.1 Introduction

Power over Ethernet (PoE), as defined in the IEEE 802.3-2005 (clause 33) standard, provides both data and power over unshielded twisted-pair copper wiring, such as Category 5 (CAT-5) cable. Power is supplied to the cable by Power Sourcing Equipment (PSE) that may be located at the Ethernet router/hub or between the router/hub and the Powered Device (PD). The PSE applies a nominal 48 VDC to the CAT-5 cable after a process that confirms a PD is connected. The PD typically includes a DC/DC converter that converts the 48 VDC to voltages required by the PD circuitry.

The PD must comply with EMC standards, such as that defined by EN 55022 / CISPR 22, in order to be sold in many markets. The EN 55022 / CISPR 22 standard establishes limits for both conducted emissions and radiated emissions. The limits are defined for Class A (commercial) and Class B (residential) equipment, with Class B being the more stringent. The conducted emissions generated by a PD, which is considered to be a telecommunication port, are measured as common-mode disturbances on the CAT-5 cable. The radiated emissions associated with a PD can be in the form of emissions radiating from the CAT-5 cable as a result of the PD's conducted common-mode noise (i.e. antenna mode disturbances), or emissions that radiate directly from the PD itself.

1.2 PD Design Example Schematic

Figure 1-1 shows a schematic of the circuit used to demonstrate the EMI guidelines presented in this application report. The circuit uses the TPS23750 in a non-isolated buck converter topology to produce a 5-V at 2-A output. The IEEE 802.3-2005 standard requires that circuits connected to the 10/100Base-T Ethernet port be isolated from all external electrical connections that can be touched by users or connected to other equipment. PDs without these connections may use non-isolated converters for their simplicity, while isolated converter topologies are used to otherwise meet the standard or for their added layer of safety to users.

Figure 1-1 is divided into three separate sections (input, intermediate, and power) to facilitate discussion of the EMI guidelines. The input section on the left side of the schematic is considered to be the "quiet side" of the circuit, while the power section on the right side of the schematic is considered to be the "noisy side" of the circuit. It's desirable to maintain both physical and electrical (filtering) separation between these two sides of the circuit in order to prevent conducted and radiated noise from entering the input-related circuitry (which connects to the CAT-5 cable).

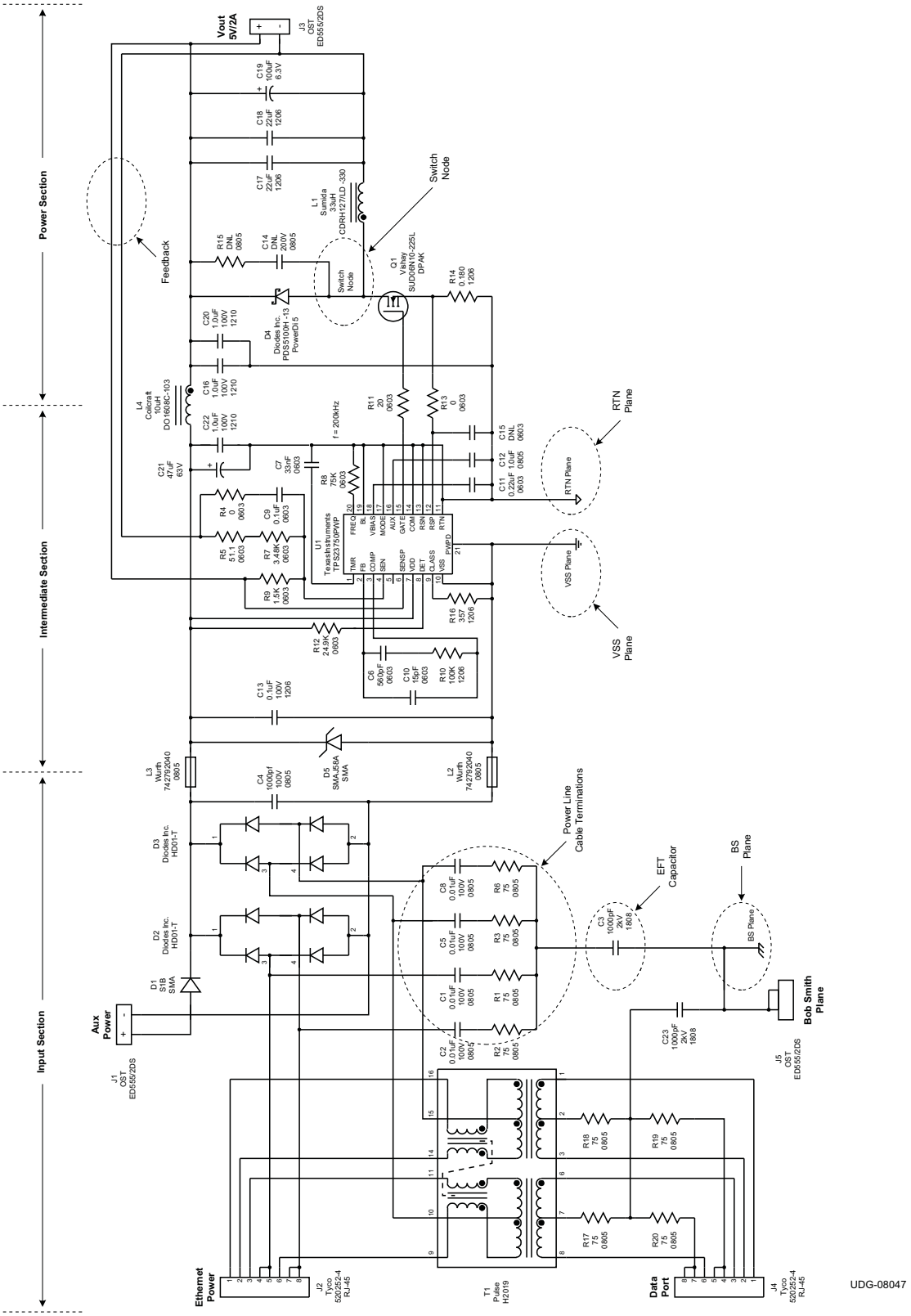

Figure 1-1. TPS23750 Non-Isolated Buck Converter Schematic

1.3 PD Design Example Circuit Board Layout

Figure 1-2 through Figure 1-4 show the board layout used for the circuit of Figure 1-1. The board measures 2" x 4" and consists of two layers of 2 oz. copper on a FR-406 substrate with an overall thickness of 0.062".

A photo of the actual circuit board assembly is shown in Figure A-1 in Appendix A.

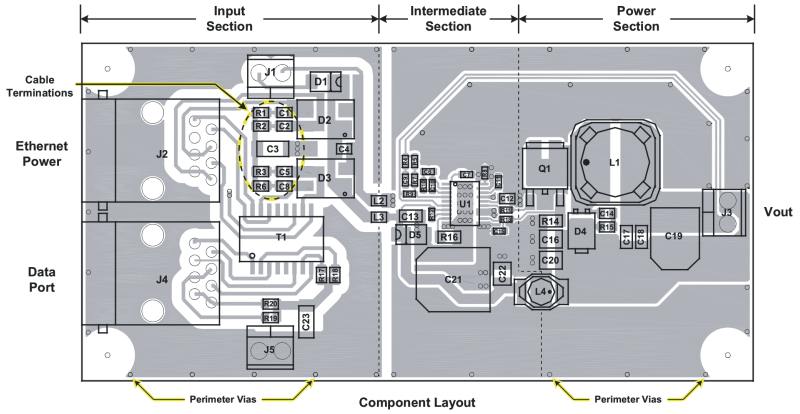

Figure 1-2. TPS23750 Non-Isolated Buck Converter Circuit Board Component Layout

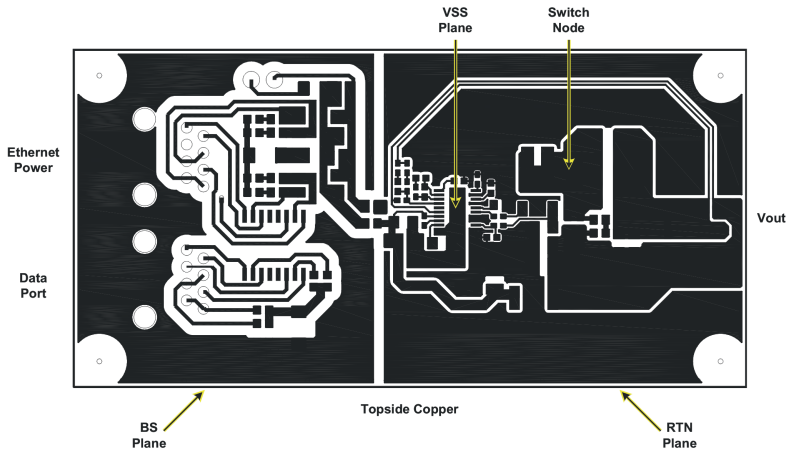

Figure 1-3. TPS23750 Non-Isolated Buck Converter Circuit Board Top Layer

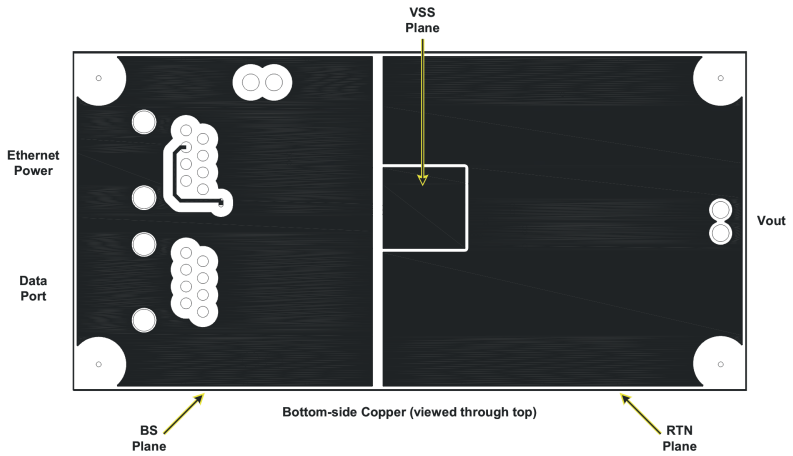

Figure 1-4. TPS23750 Non-Isolated Buck Converter Circuit Board Bottom Layer

1.4 Input Section

Referring to Figure 1-1 through Figure 1-4, the input section is shown to comprise components that are typically used for the front-end of PD applications. For EMI considerations, the guidelines below were followed for this section of the circuit:

- Congregate the input-related components toward the RJ-45 input connectors.
- Include the 75-Ω, 0.01-μF, Bob Smith cable terminations on the input power lines as shown.
- Include the 1000-pF, 2-kV bypass capacitor (C3) to tie the Bob Smith cable terminations to a copper plane (shield) which is commonly referred to as the Bob Smith plane (BS plane). Connect C3 to the BS plane using dedicated vias located directly at the capacitor termination.
- Treat the BS plane as a phantom or literal earth connection and use it to create a top and bottom layer ground plane that surrounds the input-related circuitry. Maintain a 0.060” high voltage spacing between the BS plane and all other circuitry.
- Use a number of perimeter vias to stitch the top and bottom layers of the BS plane together.
- Include the PoE transformer (T1) with internal common-mode chokes (most common topology available from magnetics suppliers).
- To minimize the possibility of radiated and magnetic coupling into the input section (from the power section), do not oversize the copper traces interconnecting the input-related components. Size the traces so that they meet current handling and thermal requirements without being excessive.
- Include provisions for inserting ferrite beads (L2/L3) to separate the input and intermediate sections of the circuit. Along with acting as high-frequency filters, the beads also serve to isolate the lower input impedance of the PD from the Bob Smith termination impedance. If not needed, the beads could always be replaced by 0-Ω resistors.
- Include provisions for a ceramic capacitor (C4) at the output of the diode bridges (D2/D3) to form a filter with the ferrite beads. C4 would typically have a value of approximately 1000 pF. The combined value of C4 and C13 (intermediate section) should not exceed 0.12 μF to be IEEE 802.3-2005 compliant.

The 75-Ω impedance matching resistors are routinely used for cable terminations in Ethernet applications to minimize EMI and reduce susceptibility (see Section 1.13, Reference 5). The 0.01-μF capacitors used for the cable terminations are required for PoE applications in order to AC couple the 75-Ω resistors (since DC is present in a PoE system). Although the 1000-pF, 2-kV bypass capacitor has historically been used to reduce susceptibility in PD applications, it seems reasonable that it would also have the reciprocal affect of suppressing EMI. A closer look at the schematic reveals that the combination of this bypass capacitor and the cable terminations appears to resemble a “Y-capacitor” type of circuit which is commonly used to suppress common-mode noise in mains port applications. The return end of a Y-capacitor circuit is typically connected to earth or chassis ground. The above-mentioned BS plane was introduced in the design example to emulate such a connection. For some earthed applications, the BS plane might actually be physically connected to earth. For unearthed applications, the BS plane is intended to present itself as a phantom earth connection. For either instance, the BS plane might also be connected to a shielded enclosure (chassis ground).

1.5 Intermediate Section

Referring to Figure 1-1 through Figure 1-4, the intermediate section of the circuit is shown to include the PoE interface and DC/DC controller circuitry. For EMI considerations, the guidelines below were followed for this section of the circuit:

- Include the 0.1-µF filter capacitor (C13) which is also required to be IEEE 802.3-2005 compliant.
- Include the LC filter (L4/C21/C22) to separate the intermediate and power sections of the circuit. The filter attenuates the input ripple generated by the DC/DC converter located in the power section. The *winding start* of L4 should be connected to the input side of the DC/DC converter in order to keep the relatively noisy end of the winding embedded within the innermost section of L4. The inductor manufacturer's datasheet should be consulted to determine the location of the winding start and its relationship to any markings on the inductor. The proper orientation of the inductor should be specified in production to ensure consistent EMI performance.
- Orient the TPS23750 IC (U1) so that pins 1-10 (input-related) are toward the input side of the board and pins 11-20 (output-related) are toward the output side of the board.
- Locate the peripheral components associated with U1 in close proximity to the device, making short and direct connections to the device pins to eliminate any possibility of erratic or unstable operation.
- Locate the AUX bypass capacitor (C12) so as to create a short compact path between the AUX pin of U1 and the return side of the current sense resistor (R14). The AUX pin of U1 is the supply for the internal gate driver and C12 provides the high-frequency energy for the gate drive pulses to the MOSFET (Q1). Gate drive paths are often overlooked sources of EMI.
- Include provisions for a gate resistor (R11) to connect the gate output of U1 to the gate of Q1. The resistor provides a level of control over EMI by adjusting the slew rate of Q1. It can play a role in controlling both conducted and radiated emissions. The resistor value, typically between 10 Ω and 75 Ω, can be optimized to balance efficiency and EMI margins.
- Create a topside and bottom-side ground island (VSS plane) for the VSS connections associated with pin 10 of U1. Size the VSS plane to make direct connections to the VSS-related components and to provide heat-sinking for the power pad of U1 without being excessive.
- Create a topside and bottom-side ground plane (RTN plane) for the RTN connections associated with pin 11 of the U1. Use the RTN plane as the main ground plane associated with the intermediate and power sections of the board. Ideally, the bottom side of the RTN plane should be as uninterrupted as possible, with the exception of flowing around the above-mentioned VSS plane. Allow the topside of the RTN plane to flood into unused areas and surround the intermediate and power circuitry, creating a return shield for any stray radiated noise.
- Use multiple perimeter vias to stitch the top and bottom layers of the RTN plane together.
- To eliminate any possibility of erratic or unstable operation, the output feedback connections should be routed away from the power section components and shielded by the RTN plane. For noise immunity, the feedback-related components should be located near U1, so that the longer exposed feedback traces are tied directly to the low-impedance presented by V_{OUT}. For multi-layer circuit boards, the feedback traces can be further shielded by placing them on an inner layer between two RTN plane layers.
- Use dedicated vias to connect the return end of each bypass/decoupling capacitor to its respective ground plane. Locate the vias directly at the capacitor termination to create a low-impedance return path. Use multiple vias for gate drive and power related capacitors such as C12 and C22.

1.6 Power Section

Referring to Figure 1-1 through Figure 1-4, the power section of the circuit is shown to comprise the DC/DC converter which can be a main source of EMI due to its inherently high dv/dt and di/dt operation. For EMI considerations, the guidelines below were followed for this section of the circuit:

- Include the high-frequency ceramic capacitors (C16/C20) on the right side of L4. These capacitors provide the high-frequency pulsating current for the DC/DC converter. The magnitude of the peak-to-peak AC ripple voltage developed across these capacitors, which can contribute to EMI, is inversely proportional to the capacitance and proportional to the ESR of the capacitors. The capacitors should be physically located to create a compact, low-inductive path between the RTN side of R14 (i.e. Q1 return path) and the cathode of the schottky diode (D4). This minimizes any EMI-generating voltage spikes that can be caused by the high di/dt operation associated with these circuit paths.

- Use multiple vias to connect the RTN side of C16/C20 to the RTN plane in order to create a low-impedance return path for any stray radiated noise picked up by the above-mentioned RTN plane.
- Use compact, low-inductive paths for all connections to the power-related components to minimize any EMI-generating voltage spikes and any possible higher frequency ringing that can be related to circuit board and component parasitics. The main power paths to consider are the Q1 path (when Q1 is on and D4 is off) and the D4 path (when D4 is on and Q1 is off). The component flows associated with the two paths are summarized as follows:
  - Q1 path: C16/C20 → C17/C18/C19 → L1 → Q1 → R14 → C16/C20
  - D4 path: L1 → D4 → C17/C18/C19 → L1
- The connection between Q1, L1, and D4 is commonly referred to as the *switch node* of a buck converter. The voltage on this node switches from 0 V to VIN (48 V nominal) in typically 20 ns to 50 ns. Due to this high dv/dt operation, the switch node can potentially be a large contributor to EMI. The circuit board copper connected to the switch node presents itself as a radiating surface capable of radiating significant EMI. This problem is usually complicated by the fact that this copper is also used to provide heat-sinking for the switch node components. The amount of copper used for the switch node should be optimized to minimize the size of the EMI radiating surface, while maintaining adequate heat-sinking. An effective technique for reducing the radiating surface area is to hide a portion of the switch node copper under shielded magnetics, such as the output inductor (L1).
- Connect the *winding start* of L1 to the switch node in order to keep the noisy end of the winding embedded within the innermost section of L1. The outermost section of the winding is then connected to the DC output return, providing some level of shielding. The inductor manufacturer's datasheet should be consulted to determine the location of the winding start and its relationship to any markings on the inductor. The proper orientation of the inductor should be specified in production to ensure consistent EMI performance.
- Provide heat-sinking for the *quiet end* of power components where possible. This is related to the switch node discussion above. In an effort to minimize the EMI radiating surface presented by the switch node copper, additional heat-sinking of components such as L1 and D4 can be provided by placing copper at the relatively quiet end of the component. In the design example, a significant portion of the heat-sinking for L1 is provided by the copper located from the output side of L1 to the output connector. The majority of heat-sinking for D4 is provided by the copper connected from the cathode of D4 to the output connector.
- Include provisions for a possible RC snubber (R15/C14) across D4. The snubber might be used to dampen any higher frequency ringing that may be present on the switch node due to circuit board and component parasitics. It can play a role in controlling both conducted and radiated emissions. Note that the snubber components were not loaded in the design example, after confirming with an oscilloscope that no higher frequency ringing was present on the switch node waveform when using the selected components and this particular board layout.
- Centrally locate the power circuitry so that it is surrounded by the RTN plane copper to create a shield for any stray radiated noise (as previously mentioned in Section 1.5).

1.7 Conducted Emissions Pre-Compliance Test Setup

Figure 1-5 shows the block diagram and Figure 1-6 shows a photo of the pre-compliance test setup that was used to measure the conducted emissions of the design example. The test setup was constructed per EN 55022:1998 - Figure 4. An Impedance Stabilization Network (ISN) specifically designed to perform conducted emissions tests on balanced pair telecommunication lines was used. The EMC Analyzer was programmed with the proper correction factors to account for the attenuation characteristics of the ISN, the coax cable, and the Transient Limiter.

The conducted emissions test was performed under full power conditions by connecting a 10-W resistive load to the output of the buck converter. In order to simulate a worst case scenario, the test was performed with no reliance on a shielded enclosure as shown in the photo. The emissions were measured against the more stringent Class B requirement of the EN 55022/CISPR 22 standard.

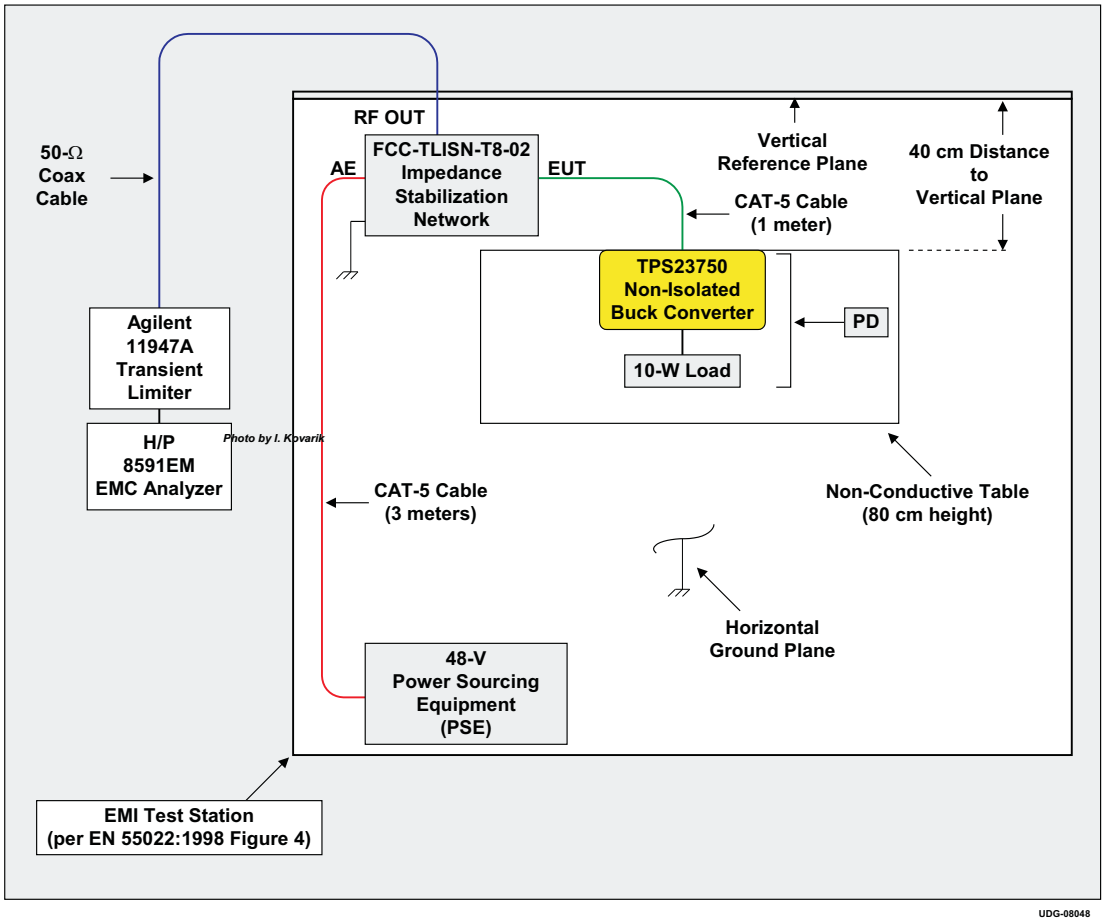

Figure 1-5. Conducted Emissions Pre-Compliance Test Setup Block Diagram

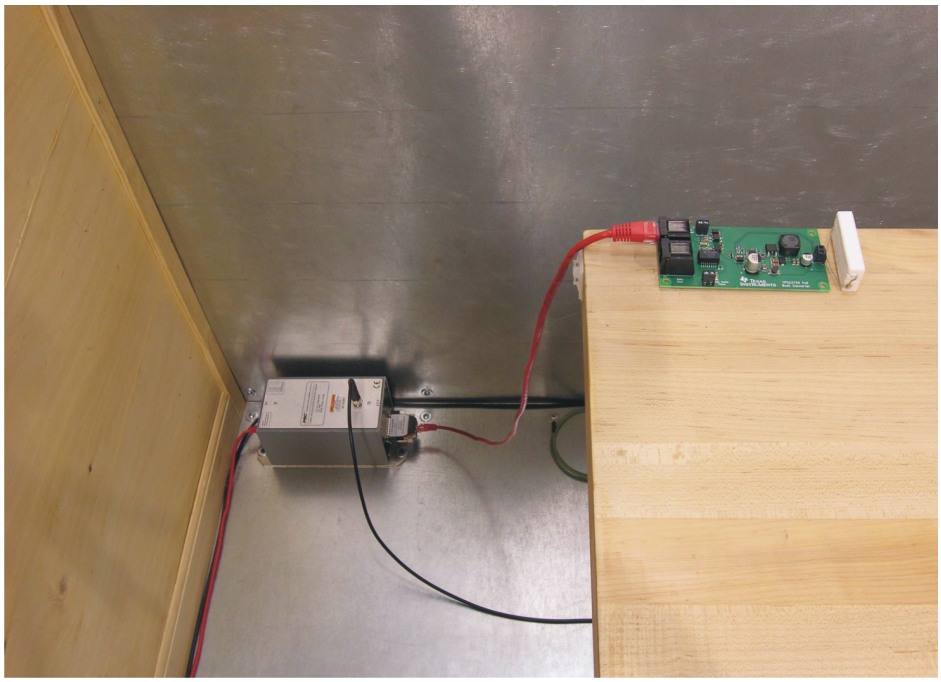

Figure 1-6. Conducted Emissions Pre-Compliance Test Setup Photo

1.8 Conducted Emissions Results

The results of the pre-compliance conducted emissions test for the design example are shown in Figure 1-7. The peak detector mode of the H/P 8591EM EMC analyzer was used to be conservative. The peak measurements are seen to be approximately 30 dB below the Class B quasi-peak limit and approximately 20 dB below the Class B average limit. These margins comfortably meet the 6-dB to 10-dB minimums that are typically used by the industry. The added margin at 30 MHz is a reasonable indicator that radiated emissions will also be low.

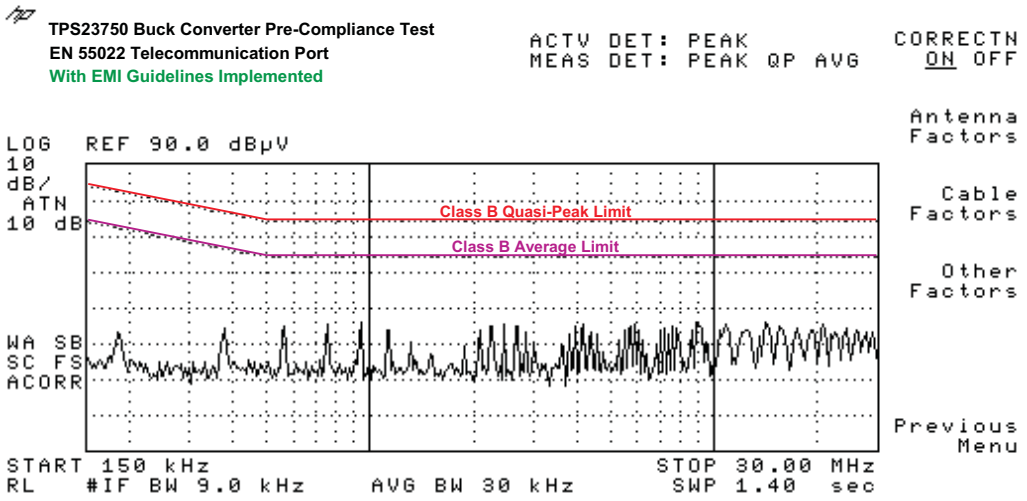

Figure 1-7. TPS23750 Buck Converter Conducted Emissions Results

In comparison, Figure 1-8 shows the conducted emissions results of a previous iteration of the circuit board, prior to implementing the guidelines described in this application report. It can be seen that an improvement of approximately 10 dB was realized after implementing the described methods.

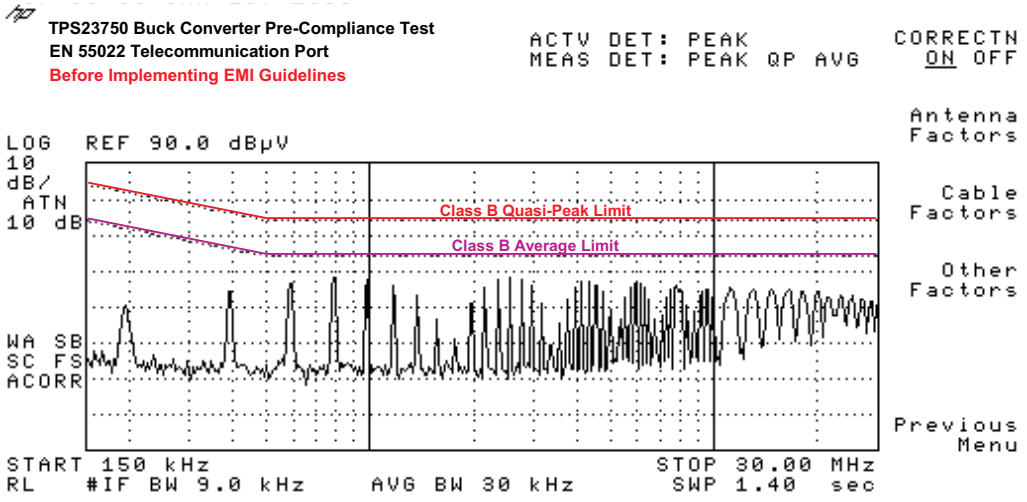

Figure 1-8. Conducted Emissions Before Implementing EMI Guidelines

1.9 Efficiency and Thermal Operation Results

Some of the guidelines for the design example make reference to optimizing items such as slew rate and copper sizes to balance EMI noise margin with efficiency and thermal performance (heat-sinking). The efficiency graph shown in Figure 1-9 indicates that the conducted emissions results of Figure 1-7 were obtained while maintaining a targeted DC/DC efficiency of 85% and an overall end-to-end efficiency of 80%. The safe operating area graph in Figure 1-10 shows no thermal derating at 85°C and natural convection.

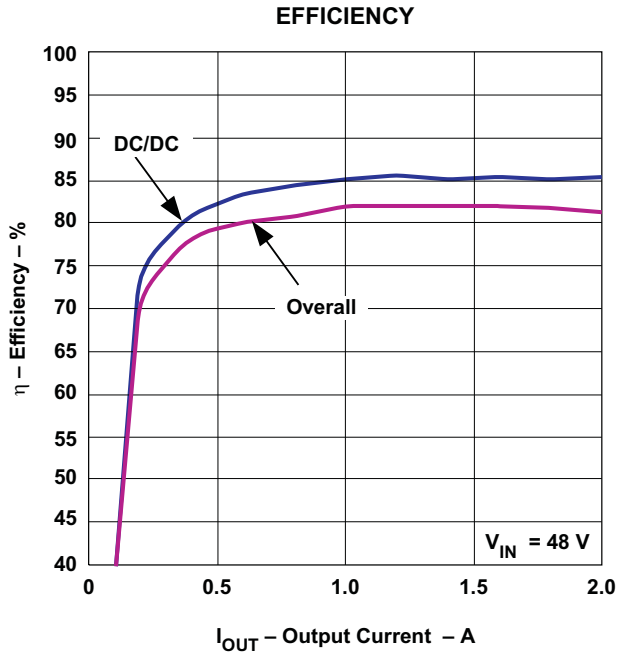

Figure 1-9.

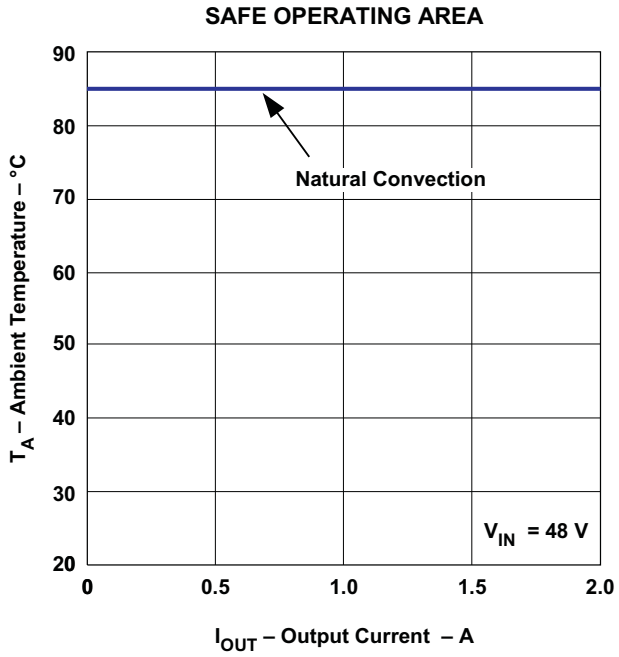

Figure 1-10.

1.10 Radiated Emissions

Radiated emissions associated with a PD can be in the form of antenna-mode disturbances from the CAT-5 cable or emissions that radiate directly from the PD itself. The antenna mode disturbances should be addressed by meeting the common-mode conducted emissions requirements of the EN 55022 / CISPR 22 standard. As mentioned in Section 1.8, having a significant amount of margin at the 30-MHz upper end of the conducted emissions span is a reasonable indicator that emissions radiated directly from the PD will also be low. The following guidelines can be considered if further adjustments to radiated emissions are required.

- Use an oscilloscope to determine if any higher-frequency ringing exists on any of the switching waveforms. This ringing could be related to circuit board and component parasitics. If any ringing is present, determine if it can be reduced or eliminated by an improvement in board layout, by the slowing of slew rates (increasing R11 in the design example), or by the use of damping circuits such as an RC snubber (using R15/C14 in the design example).
- The slew rate of a DC/DC converter switch node can also present an inherent EMI signature within the radiated range. The magnitude of this signature can be lowered by slowing the slew rate of the switch node (increasing R11 in the design example or using an RC snubber), at some cost in efficiency.
- Further improvements in EMI performance may be realized in PD applications that make use of a shielded enclosure, especially in the case of radiated emissions. For these applications, the shield of the enclosure would most likely be connected to an internal circuit board plane, such as the BS plane introduced in Section 1.4.

1.11 Considerations

Another objective of the design example was to obtain the desired EMI performance while using components that are commonly used for PoE and DC/DC circuits. Other PD applications might consider the use of components such as shielded RJ-45 jacks that integrate the PoE transformer and cable termination components discussed in Section 1.4. Depending on power levels and grounding configurations, some PD applications might benefit from the use of common-mode chokes and possible Y-capacitors.

1.12 Summary

Practical guidelines to designing an EMI compliant PoE PD have been presented in this application report. The guidelines were implemented into an actual design example of a non-isolated buck converter using the TPS23750 which includes an IEEE 802.3-2005 compliant PD front-end and a DC/DC controller. The design example was subjected to pre-compliance conducted emissions testing according to the telecommunication ports requirement of the EN 55022 / CISPR 22 standard. The peak emissions of the design example were found to be approximately 30 dB below the Class B quasi-peak limit and approximately 20 dB below the Class B average limit defined by the standard. These comfortable EMI margins were obtained while still meeting efficiency and thermal performance objectives.

1.13 References

1. EN 55022:1998 CISPR 22:1997
2. *TPS23750: Integrated 100-V IEEE 802.3af PD and DC/DC Controller*, Datasheet SLVS590A, Texas Instruments, August 2005 Revision
3. *TPS23750 Buck-Converter Evaluation Board – HPA107*, User's Guide SLVU136, Texas Instruments, July 2005 Revision
4. *Electrical Transient Immunity for Power-Over-Ethernet*, Jean Picard, Application Report SLVA233A, Texas Instruments, August 2006 Revision
5. *Method to Enhance the Performance of Category 5 Cable in the Electromagnetic Environment*, Bob Smith, SynOptics, January 25th 1993

1.14 Acknowledgements

The author would like to thank the following individuals for their contribution to this application report:

1. Martin Patoka - overall guidance
2. Larry Pruyn - circuit board layout
3. Illya Kovarik - photography
4. Tony Merfeldas - EMI test setup construction

Appendix A

A.1 Design Example Photo

Figure A-1 shows the TPS23750 Non-Isolated Buck Converter Design Example

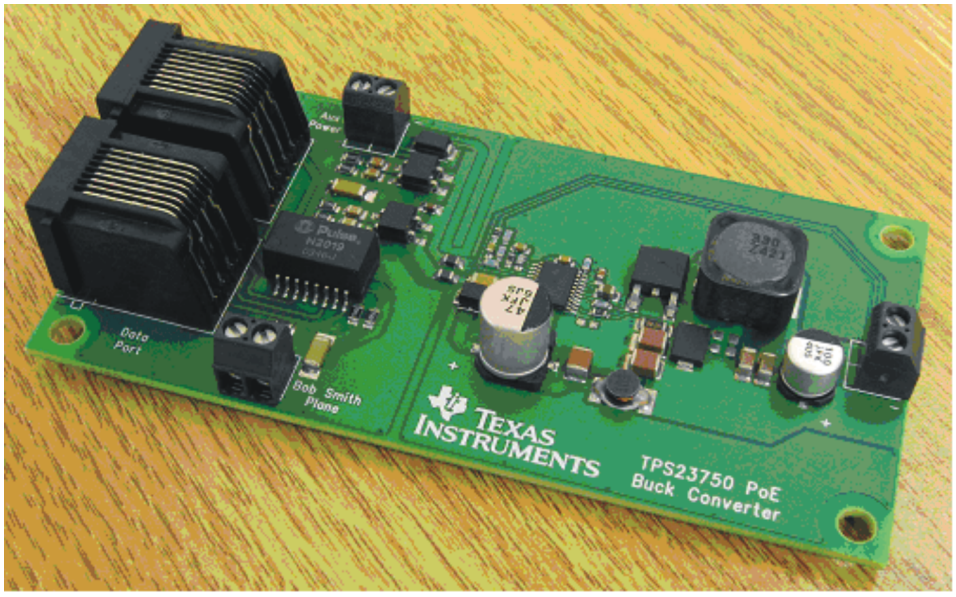

Figure A-1. TPS23750 Non-Isolated Buck Converter Design Example

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