Application Report
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Opto-Isolator Selection Guidelines: TPS2384 I²C Interface

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ABSTRACT

The TPS2384 is a quad-port power sourcing equipment power manager (PSEPM) which is compliant to the Power-over-Ethernet (PoE) IEEE 802.3af standard. When ground isolation is required between the micro-controller and Ethernet ports, opto-isolators can be placed between the TPS2384 I²C interface and micro-controller. This document provides design guideline specifics for selection of the opto-isolator devices.

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1 Introduction

In some applications, electrical ground isolation between the 48V referenced TPS2384 circuitry and master controller (MC) may be required. While other isolator configurations are possible, an optical-isolator implementation is discussed in this report.

Two significant isolator design issues are considered:

- Impact on TPS2384 digital I²C timing when inserting opto-isolators in the control path.
- Opto-isolator power consumption from the TPS2384 digital supply (V3.3 — pin 24).

Figure 1 illustrates a typical opto-isolator connection between the MC and the TPS2384.

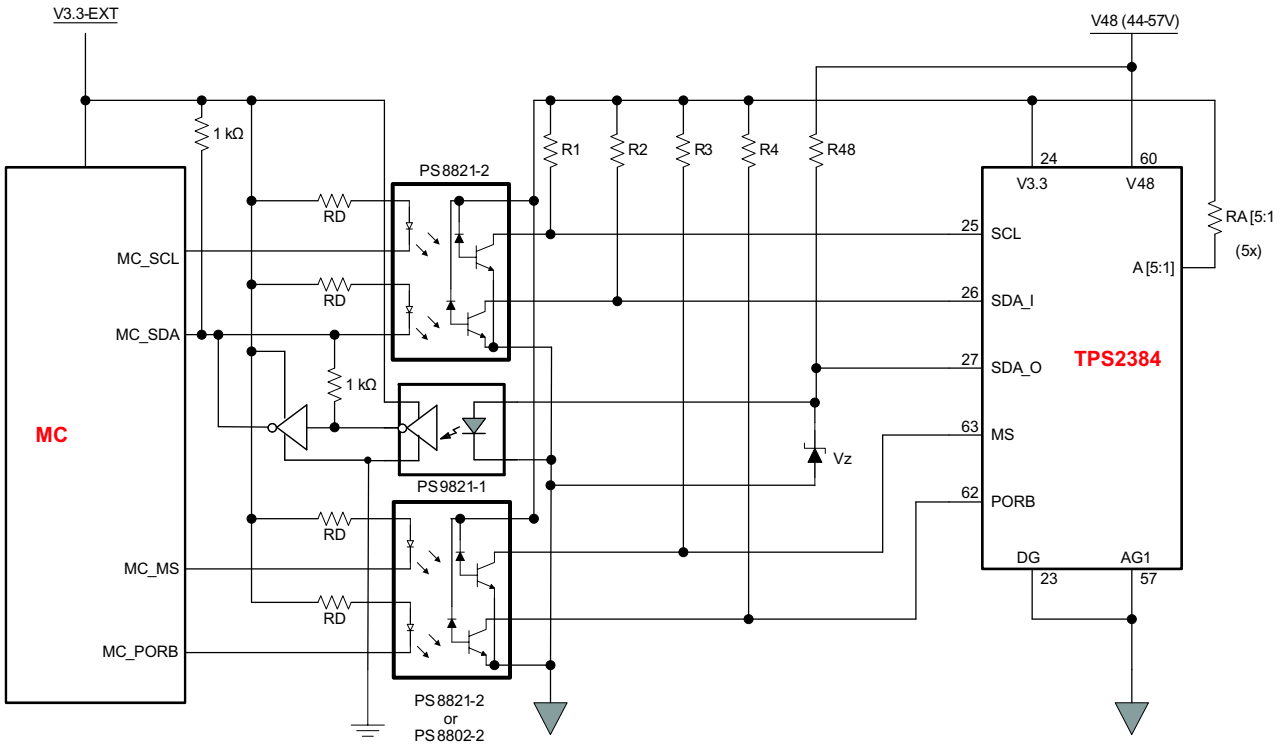

Figure 1. Basic Interface Diagram

2 First Pass Timing

The TPS2384 data sheet digital I^{2}C timing requirements are summarized in Table 1. These timing requirements mirror the requirements for fast mode (F/S) devices outlined in the Phillips I^{2}C specification. The opto-isolator propagation delay characteristics can constrain and possibly necessitate alteration of the MC output timing requirements.

Table 1. Digital I^{2}C Timing Requirements

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
SCL clock frequency		0		400	kHz
Pulse duration	SCL high	0.6			µs
	SCL low	1.3			
Rise time, SCL to SDA				0.3	µs
Fall time, SCL to SDA				0.3	µs
Setup time, SDA to SCL		0.25			µs
Hold time, SCL to SDA		0.3		0.9	µs
Bus free time between start and stop		1.3			µs
Setup time, SCL to start condition		0.6			µs
Hold time, start condition to SCL		0.6			µs
Setup time, SCL to stop condition		0.6			µs
Delay time, SCL to SCL_{INT}, $t_{d(SCL)}$			0.5 (1)	0.9 (1)	µs

(1) $t_{d(SCL)}$ is the TPS2384 internal clock delay.

Selection of the opto-isolator type should also consider end to end signal polarity and MC output drive type. The circuit in Figure 1 implements *inverting* opto-isolators for the SCL and SDA_I inputs but since the MC drives the LED cathode; no net polarity inversion takes place.

Also of note in Figure 1 is the SDA_O signal drive implementation. To minimize V3.3 loading, the SDA_O signal derives its LED anode drive current from V48. Since this drive implementation induces a polarity change, an inverter is required between the opto-isolator output and the MC. This inverter must be an open drain type to be compatible with the I^2C specification and have minimal impact on timing. The zener diode Vz (5.6V), adds a layer of voltage protection to the opto-isolator LED and SDA_O. R48 should be chosen with power dissipation (1/2W) and LED bias current in mind.

2.1 SCL/SDA_I Setup and Hold Considerations

The I^2C standard states that SDA_I must be stable during the SCL logic high time (including SDA_I setup and hold times), or in other words SDA_I can only change state when SCL is a valid low. t_{trans} is the allowable SDA_I state transition time window (during SCL low) and bounds the rising and falling edge propagation delay requirements of the opto-isolators. Table 2 shows t_{trans} for minimum and maximum hold times, t_h.

$$t_{trans} = t_{low} - t_{su(min)} - t_h$$

Table 2. Acceptable SDA Transition Time Window

t_{trans} (µs)	t_{low} (µs)	t_{su} (µs)	t_h (µs)
0.75	1.3	0.25	0.3
0.15	1.3	0.25	0.9

In general, if the rising and falling edge propagation delays of the SCL and SDA_I opto-isolators track each other, are sufficiently small, and the MC meets the requirements of the I^2C standard, then input signal timing can be met. Similarly, start, restart, and stop conditions have setup and hold requirements of $t_{stop/start}$ = 0.6 µs which should also be considered.

2.2 SDA_O Timing Considerations

The TPS2384 internal SCL delay, $t_{d(SCL)}$ should be considered for device reads. SDA_O transition timing occurs on the falling edge of the TPS2384 internal SCL signal as illustrated in Figure 2. The SDA_O opto-isolator is restricted to faster devices so that data arrives at the MC within the required setup and hold times. $t_{d(SCL)}$, $t_{PLH(SCL)}$, $t_{PHL(SCL)}$, and $t_{su(MC)}$ delays bound opto-isolator propagation delays on the SDA_O signal. Also note that the SDA_O opto-isolator (and inverter) are powered by V3.3-EXT and do not impact V3.3 loading.

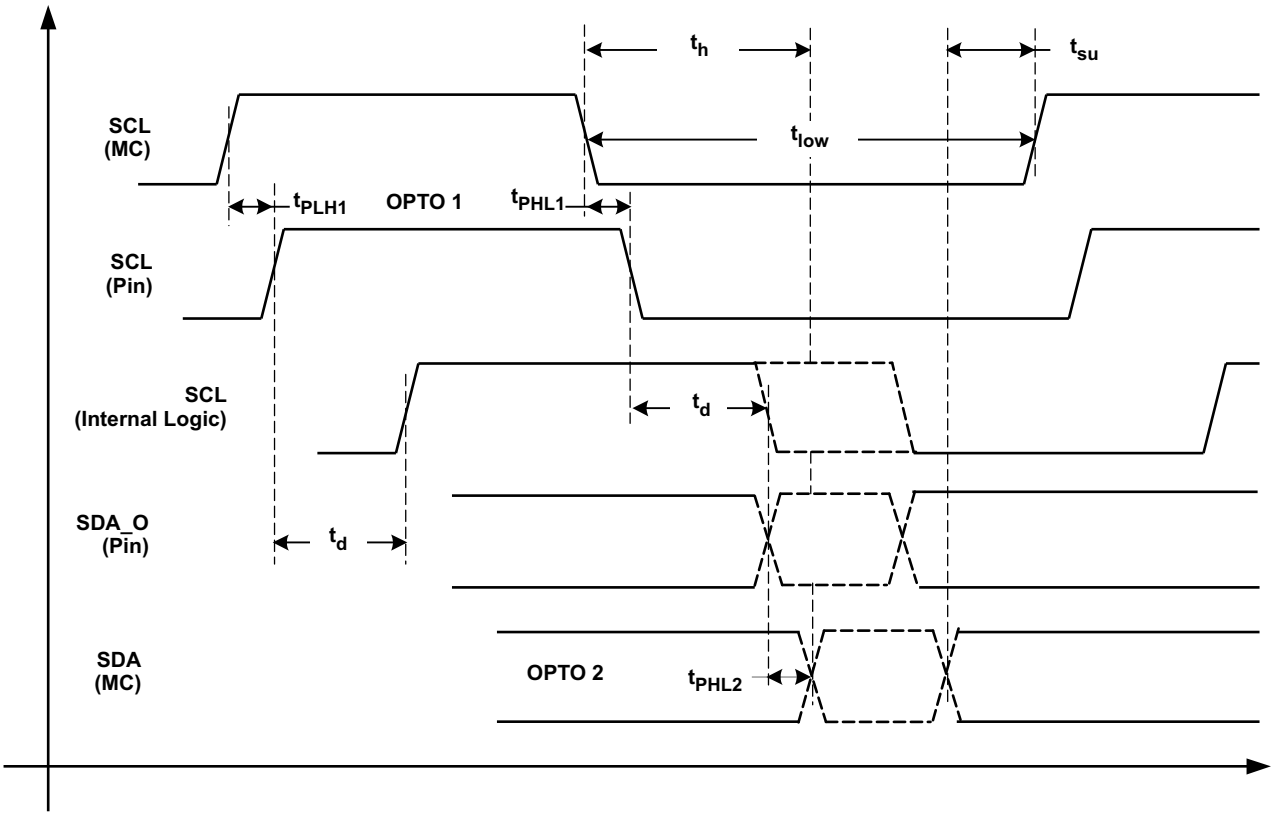

Figure 2. TPS2384 Internal SCL Delay

Table 3 shows target t_{PHL} (total sum for SCL and SDA_O opto-isolators) values that can be derived from the following equations.

$t_{h(min)} < t_{PHL} + t_{d(SCL)} < t_{h(max)}$

$t_{h(min)} - t_{d(SCL)} < t_{PHL} < t_{h(max)} - t_{d(SCL)}$

and

$t_{PHL} + t_{d(SCL)} < t_{low} - t_{su}$

$t_{PHL} < t_{low} - t_{su} - t_{d(SCL)}$

Table 3. Opto-Isolator t_{PHL} Values

CONSIDERING SDA_O HOLD REQUIREMENTS			CONSIDERING SDA_O SETUP REQUIREMENTS		
t_{PHL} (µs)	t_h (µs)	$t_{d(SCL)}$ (µs)	t_{PHL} (µs)	t_{su} (µs)	$t_{d(SCL)}$ (µs)
> –0.2	0.3	0.5	< 0.55	0.25	0.50
> –0.6	0.3	0.9	< 0.15	0.25	0.90
< 0.4	0.9	0.5			
< 0.0	0.9	0.9			

3 Opto-Isolator Selection

For the SCL and SDA_I signals, a medium-fast, low power, dual opto-isolator configuration is desired. For the SDA_O signal, a fast, medium power, single opto-isolator is desired, and for the low speed MS and PORB signals, a slow, low power, dual opto-isolator configuration is desired. Three NEC Electronics photo couplers were selected and the relevant details are summarized in Table 4.

Table 4. Photo-Coupler Parameters

NEC Electronics Device Number	Configuration	$I_{CCL(typ)}$	$t_{PLH(min)}$ (1)	$t_{PLH(typ)}$	$t_{PLH(max)}$	$t_{PLH(min)}$ (1)	$t_{PHL(typ)}$	$t_{PHL(max)}$
PS8802-2	Dual (MS, PORB)	200 µA	0.1 µs	0.6 µs	1.2 µs	0.1 µs	0.3 µs	0.8 µs
PS8821-2	Dual (SCL, SDA_I)	200 µA	0.1 µs	0.5 µs	0.9 µs	0.1 µs	0.3 µs	0.6 µs
PS9821-1 (2)	Single (SDA_O)	7 mA		50 ns	100 ns		45 ns	100 ns

(1) $t_{PLH(min)}$ and $t_{PHL(min)}$ are estimates for this report and are not data sheet specified.
(2) PS9121 is an acceptable substitute for the PS9821.

It might be noted that the propagation delay times are a bit high for the SCL/SDA_I device. The impact of these values are evaluated in the final timing analysis.

4 Power Consumption

The I^2C interface support circuitry for the TPS2384 can be powered from the V3.3 pin if limited to less than 3mA peak. Exceeding the peak output current can cause internal digital circuit malfunction due to short circuit limiting of the V3.3 output. Excessively high DC currents should be evaluated with respect to power dissipation.

The V3.3 pin load current paths are highlighted in Figure 3. Included is loading by the 5 address lines, 4 opto-isolator output pullup resistors, and the 4 opto-isolator output amplifiers.

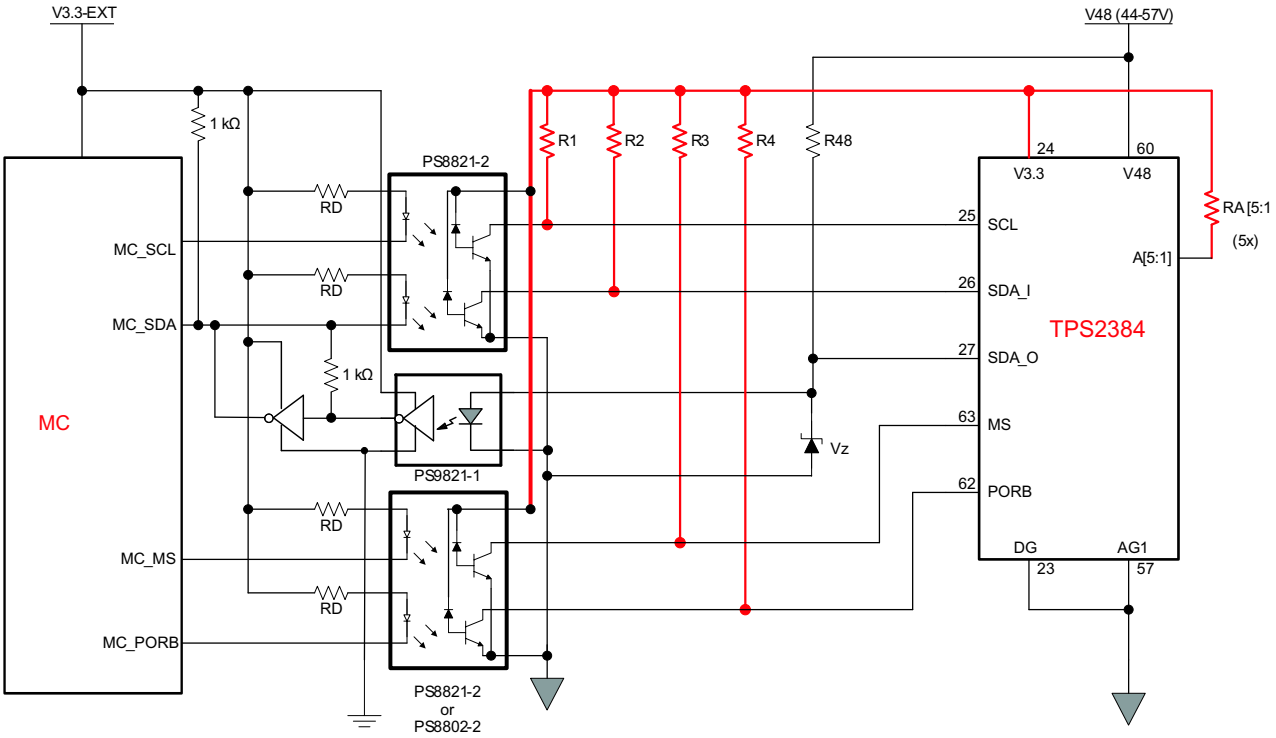

Figure 3. V3.3 Load Current Paths

4.1 DC Considerations

R3/R4: Select a value for these resistors based on MS/PORB threshold of 1.5V (and 150mV hysteresis) and the MS/PORB internal 50-kΩ resistor pull-down (R_{INT}).

$$V_{3.3(max)} \times \frac{R_{INT}/N}{R_{INT}/N + R3} > V_{TH(max)} = V_{TH(nom)} + V_{HYST}$$

Let : $R_{INT} = 0.8 \times R_{INT(nom)} = 40\ k\Omega$, N = Number of TPS2384 Devices

$$R3 < \frac{R_{INT}}{N} \times \left[\frac{V_{3.3(min)}}{V_{TH(max)}} - 1 \right] \text{ For } N = 2,\ R3 < \left(\frac{40k}{2}\right) \times \left(\frac{3}{1.65} - 1\right) = 16.4\ k\Omega$$

R1/R2: Select R1/R2 for simultaneous SCL/SDA_I low (for V3.3 output current) and minimize R1/R2 for rise time signal considerations.

$$I_{3.3(max)}(R1\ \&\ R2) = 3\ mA - I_{opto} - I_{addr} - I_{R3/R4}$$

$$I_{3.3(max)}(R1\ \&\ R2) = 3\ mA - 400\ \mu A - 50\ \mu A - 404\ \mu A = 2.1\ mA$$

$$R1/R2 > \frac{V3.3}{0.5 \times I_{3.3(max)}(R1\ \&\ R2)} = \frac{3.3}{0.5 \times 2.1\ mA} = 3.1\ k\Omega$$

$$\text{For } V3.3_{(max)} = 3.7\ V,\ R1/R2 > 3.5\ k\Omega$$

Table 5 summarizes the DC load requirement targets.

Table 5. DC Load Current Summary

	V3.3 = 3.3V	
Load	**Target I_{LD}**	**Target R_{PU}**
Address	50 µA	
PS8821-2	200 µA	
PS8802-2	200 µA	
R1	1.05 mA	3.1 kΩ
R2	1.05 mA	3.1 kΩ
R3	202 µA	16.4 kΩ
R4	202 µA	16.4 kΩ
	I_{SUM} = 3.0 mA	

4.2 AC Considerations

Bulk energy storage capacitance: Determine beneficial effects of V3.3 capacitance which sources current peaks during simultaneous *logic low* conditions. Considering V3.3 (V_S) with series source impedance R_S, minimum R_L (R1 || R2) can be determined so that V3.3 does not fall below 1.65V (V_{TH} + V_{HYST}) during simultaneous logic low (with I_S = 2.1mA). Figure 4 shows the circuit model.

$R_L = R_S = 1.65\ V/0.0021 = 786\ \Omega$

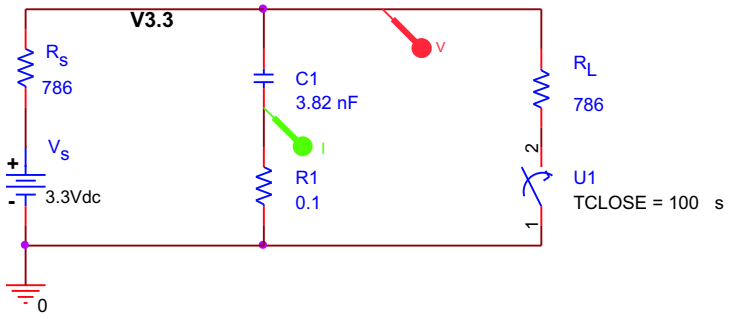

Figure 4. AC Load Model for V3.3

Target C1 value required to keep V3.3 above 1.65 V during U1 on time:

For I^2C bus speed = 100 kHz, $t_{low(max)}$ = 6 µs (very fast rise/fall times)

Target 4 × τ (98% droop) = $t_{low(max)}$

$$t_{low(max)} = 4 \times R \times C1 : R = R_L \left\| R_S = \frac{R_L}{2} \right.$$

$$t_{low(max)} = 2 \times R_L \times C1$$

$$C1(min) = \frac{t_{low(max)}}{2 \times R_L} = \frac{6\ \mu s}{2 \times 786} = 3.82\ nF$$

$$R_L = R1 \left\| R2;\ R1(min) = R2(min) = 2 \times R_L = 2 \times 786 = 1572\ \Omega \right.$$

This shows that a significantly small C1 is adequate to support V3.3 during relatively slow I^2C bus access. A reasonable bypass capacitor value of 0.1µF located at the V3.3 pin of the TPS2384 and at each pin of the dual opto-isolators provides good AC voltage stability. Assuming C1 = 0.3µF and R1 = R2 = 1572 Ω, yields $t_{low(max)}$ = 472 µs. This equates to a minimum I^2C bus access speed of 1.27 kHz. So, targeting R1 and R2 values between the minimum AC value (1572 Ω) and the minimum DC value (3.1 kΩ) provides good AC and DC performance.

The designer must keep in mind that the timing parameters detailed in Table 4 and used in Section 5 are based on I_F (set by RD in Figure 1 and Figure 3) and R_L (R1, R2, R3, R4 in Figure 1 and Figure 3) values specified in the opto-isolator manufacturers data sheet. Deviation from these values will have an impact on timing and must be evaluated.

5 Final Timing Analysis

MC writes must meet the TPS2384 setup and hold times by synchronizing data transitions to occur within the acceptable data transition window outlined in Section 2.1. MC reads from the TPS2384 must meet the MC setup and hold times as outlined in Section 2.2. The following equations define the acceptable data transition window times (during SCL low) for reads and writes.

Read Access (400 kHz SCL, t_0 at SCL rising edge):

$t_{accept1} = t_{high} + t_{h(max)}$

$t_{accept2} = t_{period} - t_{su(MC\text{-}min)}$

Write Access (400 kHz SCL, t_0 at SCL rising edge):

$t_{accept1} = t_{high} + t_{h(max)}$

$t_{accept2} = t_{period} - t_{su(2384\text{-}min)}$

NOTE: Rise and fall times are ignored here but must be considered by the designer.

Table 6 illustrates the impact of timing parameter variations during reads and writes. t_{MC} represents the delay variability that must be accounted for when designing SCL/SDA timing. Designers should target the data transitions to occur within the acceptable time windows, $t_{accept1}$ and $t_{accept2}$ for each condition.

Table 6. Timing Budget Summary

Reads								
Min	0.1	0.6	0.1	0.5		t_h =	0.9	
Max	0.9	1.2	0.6	0.9				
t_o	t_{PLH}	t_{high}	t_{PHL}	t_d	$t_{p\text{-}opto2}$	t_{mc}	$t_{accept1}$	$t_{accept2}$
0	0.1	0.6	0.1	0.5	0.1	1.4	1.5	2.4
0	0.1	0.6	0.1	0.9	0.1	1.8	1.5	2.4
0	0.1	0.6	0.6	0.5	0.1	1.9	1.5	2.4
0	0.1	0.6	0.6	0.9	0.1	2.3	1.5	2.4
0	0.1	1.2	0.1	0.5	0.1	2	2.1	2.4
0	0.1	1.2	0.1	0.9	0.1	2.4	2.1	2.4
0	0.1	1.2	0.6	0.5	0.1	2.5	2.1	2.4
0	0.1	1.2	0.6	0.9	0.1	2.9	2.1	2.4
0	0.9	0.6	0.1	0.5	0.1	2.2	1.5	2.4
0	0.9	0.6	0.1	0.9	0.1	2.6	1.5	2.4
0	0.9	0.6	0.6	0.5	0.1	2.7	1.5	2.4
0	0.9	0.6	0.6	0.9	0.1	3.1	1.5	2.4
0	0.9	1.2	0.1	0.5	0.1	2.8	2.1	2.4
0	0.9	1.2	0.1	0.9	0.1	3.2	2.1	2.4
0	0.9	1.2	0.6	0.5	0.1	3.3	2.1	2.4
0	0.9	1.2	0.6	0.9	0.1	3.7	2.1	2.4
Writes								
Min	0.1	0.6	0.1	t_h =	0.9			
Max	0.9	1.2	0.6					
t_o	t_{PLH}	t_{high}	t_{PHL}	t_{mc}	$t_{accept1}$	$t_{accept2}$		
0	0.1	0.6	0.1	0.8	1.5	2.25		
0	0.1	0.6	0.6	1.3	1.5	2.25		
0	0.1	1.2	0.1	1.4	2.1	2.25		
0	0.1	1.2	0.6	1.9	2.1	2.25		
0	0.9	0.6	0.1	1.6	1.5	2.25		
0	0.9	0.6	0.6	2.1	1.5	2.25		
0	0.9	1.2	0.1	2.2	2.1	2.25		
0	0.9	1.2	0.6	2.7	2.1	2.25		

6 Conclusion

This application of opto-isolator interface to the TPS2384 has been implemented for use with the MSP430 micro-controller. In all cases, the MC operating characteristics should be studied carefully and in some cases tailored to meet I^2C bus timing requirements. This may require SCL duty cycle adjustment and/or SDA transition time adjustment with respect to SCL. In some cases, this can be accomplished by slowing the I^2C bus speed to less than 400 kHz; however, this bus speed slowdown may limit the total number of controllable ports in larger systems.

7 References

1. *TPS2384, Quad Integrated Power Sourcing Equipment Power Manager* (SLUS634)
2. *TPS2384, Users Guide* (SLVU126B)
3. *I^2C Bus Specification*

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