Application Report
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Beyond BT High-Power PoE Solution using the TPS23880 and TPS2372-4

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ABSTRACT

The IEEE 802.3bt (Draft) standard defines maximum power of 90 W with a 4-pair configuration for a Power over Ethernet (PoE) system. But some specialized applications like daisy-chain PoE in a small cell may require more than 150 W of power. This application report presents a non-standard PoE system that can deliver 200 W of preprocessed power to the load. The non-standard Power Sourcing Equipment (PSE) interface is built around the BT (Draft) compliant TPS23880. The Powered Device (PD) interface is based on the BT (Draft) compliant high-power TPS2372-4. The total solution presents a good example for beyond BT high-power PoE applications.

Contents

1 Introduction 2
2 Beyond BT High-Power PoE System Overview 2
3 System Design Considerations 3
4 Experimental Results 6
5 Conclusion 10
6 References 10

List of Figures

1 Beyond BT High-Power PoE System 2
2 High-Power PSE Configuration 3
3 New ILIM Protection Curve of the TPS23880 4
4 High-Power PD Configuration 5
5 Detection and Classification Waveform 7
6 Power On Waveform 7
7 PSE Overload Protection 8
8 PSE Overload Protection 9
9 PD Over Load Protection 10

List of Tables

1 High-Power PoE System Parameters 3
2 New Class Resistor for TPS23880 with 110 mΩ Sense Resistor 6
3 PSE-CAT5e-PD System Performance Summary 6

Trademarks

1 Introduction

A system that complies with the IEEE 802.bt (draft) PoE standard can supply up to 90 W of power on the PSE side, which is insufficient for some specialized applications like daisy-chain PoE solution. A non-standard PoE system can be designed to meet the power requirements and retain the PoE benefits such as protection of non-PoE devices and fault tolerance. Such a solution does not comply with the IEEE802.3bt (draft) standard and must be designed and operated as a stand-alone system.

Higher power is achieved by providing power over all four pairs and increasing the current flow through each pair. To ensure proper operation, several design considerations must be taken into account. First, the current limit of both the PD and the PSE must be increased. Second, current-carrying components such as the diode bridges, power transistors, and sense resistors must be scaled up. Finally, the Ethernet data isolation transformers must be capable of carrying the worst-case current without data corruption. It may also be desirable for a high-power PSE or PD to reject its standard compliant counterpart to prevent potential failures.

A 200-W system is designed as an example and can serve as a guide for building systems with higher power requirements. The TPS23880EVM-008 and the TPS2372-4EVM-006 evaluation modules (EVM) are used to build and validate the design. Experimental results are presented and conclusions are drawn.

2 Beyond BT High-Power PoE System Overview

Figure 1 shows a block diagram of the PoE system. It is implemented as a standard 4-pair BT PSE configuration with two single signature PDs in parallel after the rectifier diodes. In order to maximize the output power and reduce power loss on the cable, 57 V power supply is chosen. The 57 V power supply is fed through the pair 1,2 and pair 4,5 in parallel, and the pair 3,6 and pair 7,8 are separated as two channels through two PSE's N-type MOSFETs. Two PDs are in parallel by VDD, VSS, and RTN pins to conduct the high current and share power. The IEEE 802.3bt (draft) standard requires the PSE output to be current limited to protect against overloads. The PD also implements current limiting to prevent transients and overloads from damaging the power switch inside. The PD's input diode bridges (or FET bridge in high power applications) allow input voltage of either polarity as permitted by the IEEE 802.3 standard. Finally, the output of the PDs supplies the downstream load such as an isolated dc/dc converter or other load.

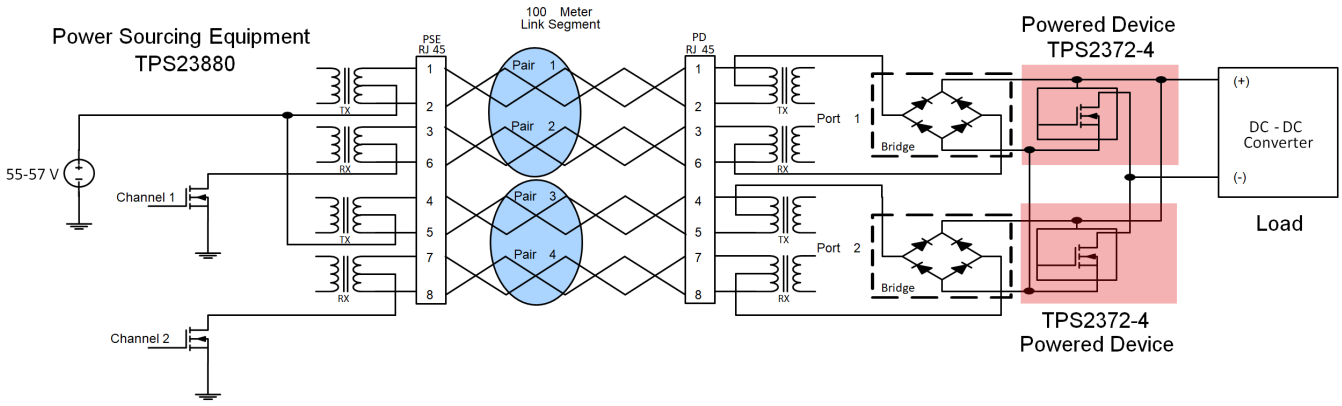

Figure 1. Beyond BT High-Power PoE System

The beyond BT high power PoE system operates as follows:

1. The PSE continuously performs detection by sinking 160 µA and 270 µA.
2. The two PDs connect their detection resistance of 50 kΩ (rather than 25 kΩ) between the input lines, telling the PSE that a valid PD is connected.
3. The PSE measures the two voltages, and if the incremental resistance is 25 kΩ, the PSE proceeds to classification.
4. The PSE performs classification by outputting a voltage between 15.5 V and 20.5 V and measuring the current. The current is decoded into a hardware class by the PSE (Class 0 through Class 8). Here Class 8 is set to implement beyond BT solution.

5. After this handshake is complete, the PSE turns on the port and applies power.
6. The PD charges its output capacitor and then turns on the dc/dc converter.

3 System Design Considerations

In order to realize the beyond BT high-power PoE system, there are several things that should be considered on both PSE and PD sides.

3.1 Calculating the Current Requirement of the System

The first step in designing a PoE system is to calculate the input current. This is necessary to set the current limits on both the PSE and PD sides and to specify the different components.

Table 1 shows the parameters of a high-power PoE system.

Table 1. High-Power PoE System Parameters

Parameter	Specifications
PSE Input Voltage	55 V - 57 V
PSE Maximum Power	200 W
Maximum PSE Current	3.64 A
PSE-Cable-PD Efficiency	>90%

3.2 High-Power PSE Design Considerations

Figure 2 shows a diagram of a BT PSE power section using the TPS23880. Changes from a standard implementation include: reducing sense resistors RSENSEx and enlarging PSE FETs Qx.

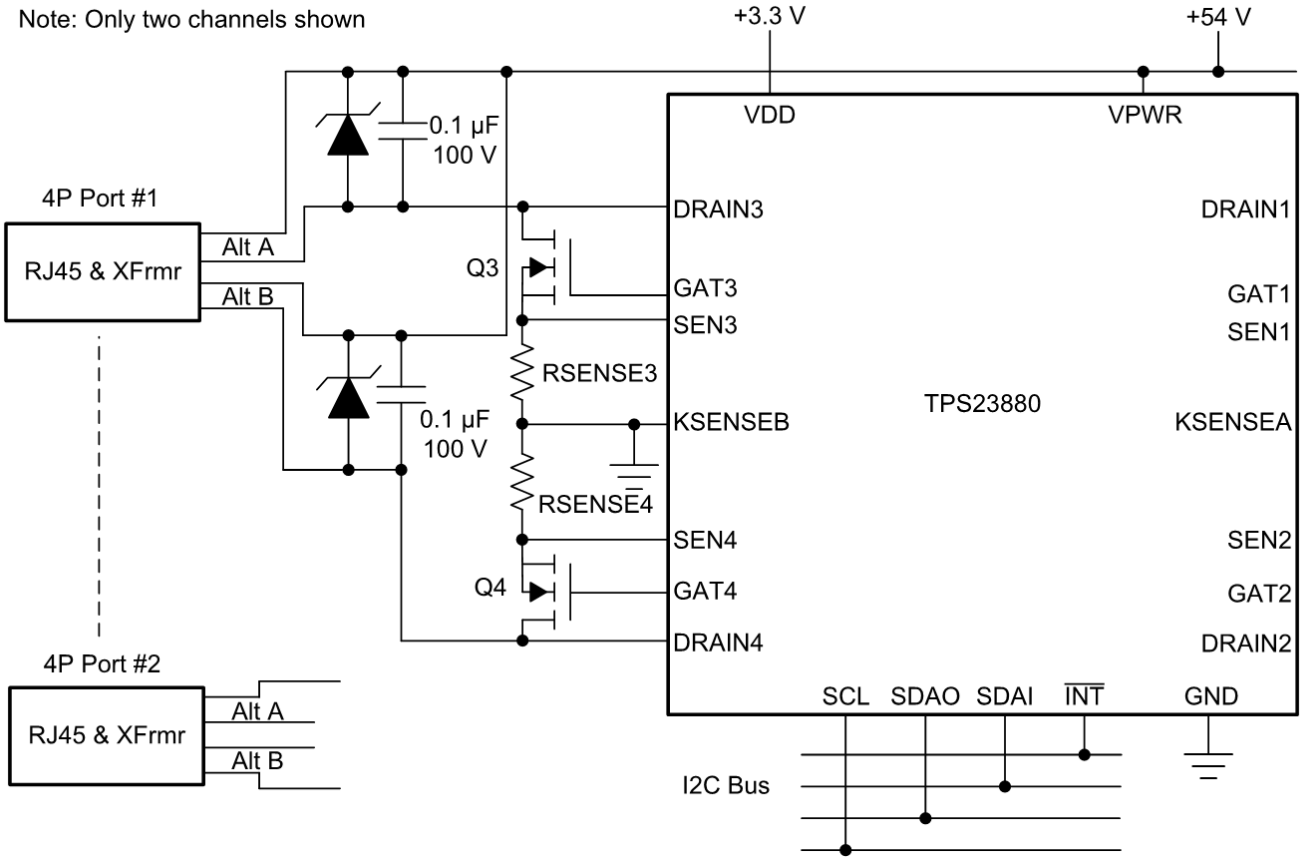

Figure 2. High-Power PSE Configuration

3.2.1 Select Sense Resistors RSENSEx

TPS23880 can do both 2-pair and 4-pair power monitoring. The PSE monitors and controls output current by sensing the voltage across RSENSE. In 4-pair power monitoring it will start a timed overload algorithm when the power of the two channels is above a threshold level 4-pair PUT (Power Policing) by sensing VSENSE and calculating the power. The PSE shuts off once the timer has reached its limit. As TPS23880 sets the PCUT to 90W automatically at the moment of turning on, it is needed to adjust the PCUT manually after power up in order to implement high power. The maximum 4-pair PCUT value of the TPS23880 is 127.5 W with the 2Ah and 2Bh registers set to FFh. In order to get the power of 200 W, RSENSE is supposed to be low enough to make the TPS23880 implement 4-pair PCUT protection until the power of the port reaches a little bit higher than 200 W. The default sense resistor of the TPS23880 is 255 mΩ. The maximum sense resistor can be calculated through Equation 1. Here the 110-mΩ sense resistor is chosen in order to withstand higher than 200-W power.

$$Rsense \leq \frac{127.5W \times 255m\Omega}{200W} = 162.5m\Omega \quad (1)$$

The current can be conducted by two PSE channels, the power rating of the sense resistor for each channel can be calculated by Equation 2. Here two 220-mΩ 0805 resistors in parallel are selected.

$$Psense \geq \left(\frac{200W}{2 \times 55V}\right)^2 \times 110m\Omega = 363.7mW \quad (2)$$

3.2.2 Select PSE FETs Qx

The PSE FETs must have low R_{dson} for high efficiency and enough SOA (Safe Operating Area) to survive during overload or short circuit conditions. The TPS23880 will monitor the current through voltage on the sense resistor and control the port voltage and current through adjusting gate voltage to make sure the V-I curve does not exceed the limitation of its own. Since the sense resistor has been changed to a lower value, the ILIM V-I curve of the PSE should be enlarged to protect higher current according to the coefficient *k* in Equation 3.

$$k = \frac{255m\Omega}{110m\Omega} = 2.3182 \quad (3)$$

The new V-I curve of the TPS23880 is shown in Figure 3.

The FETs should be selected based on the SOA which are supposed to be bigger than *2x New Option* curve as shown in Figure 3. The duration of the power surge can be set by TLIM in the 16 h register with four options - 58 ms, 15 ms, 10 ms, and 6 ms. The longer the duration lasts, the more robust FETs are needed.

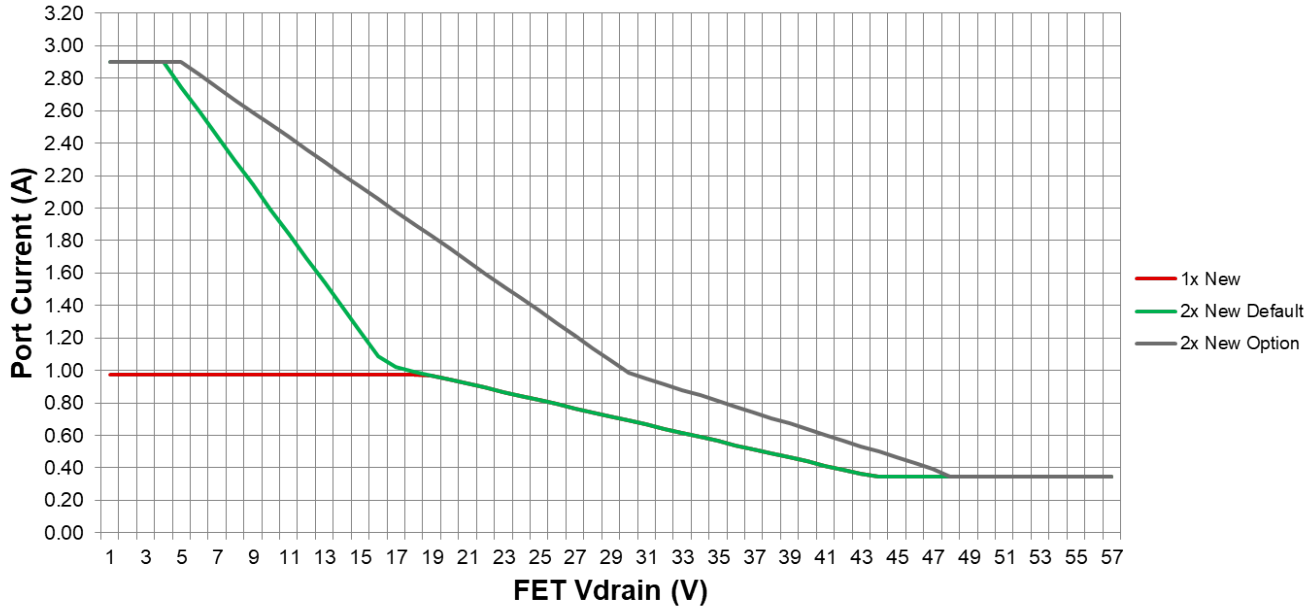

Figure 3. New ILIM Protection Curve of the TPS23880

3.3 High-Power PD Design Considerations

Once the sense resistor of the PSE is known, the PD can be designed.

Figure 4 depicts a recommended design for a high-power PD using two TPS2372-4 in parallel. The diode bridges (or FET bridges for high power applications) combine the current from both sets of pairs to power the two high-power PDs. A TVS serves to protect the PD against transients while the 0.1 uF cap is required per the IEEE802.3 PoE standard. C_{BULK} is required to present low impedance to the converter input for stability and to buffer the converter input for line and load transients. The output of the PDs (VDD-RTN) are also paralleled together for high power.

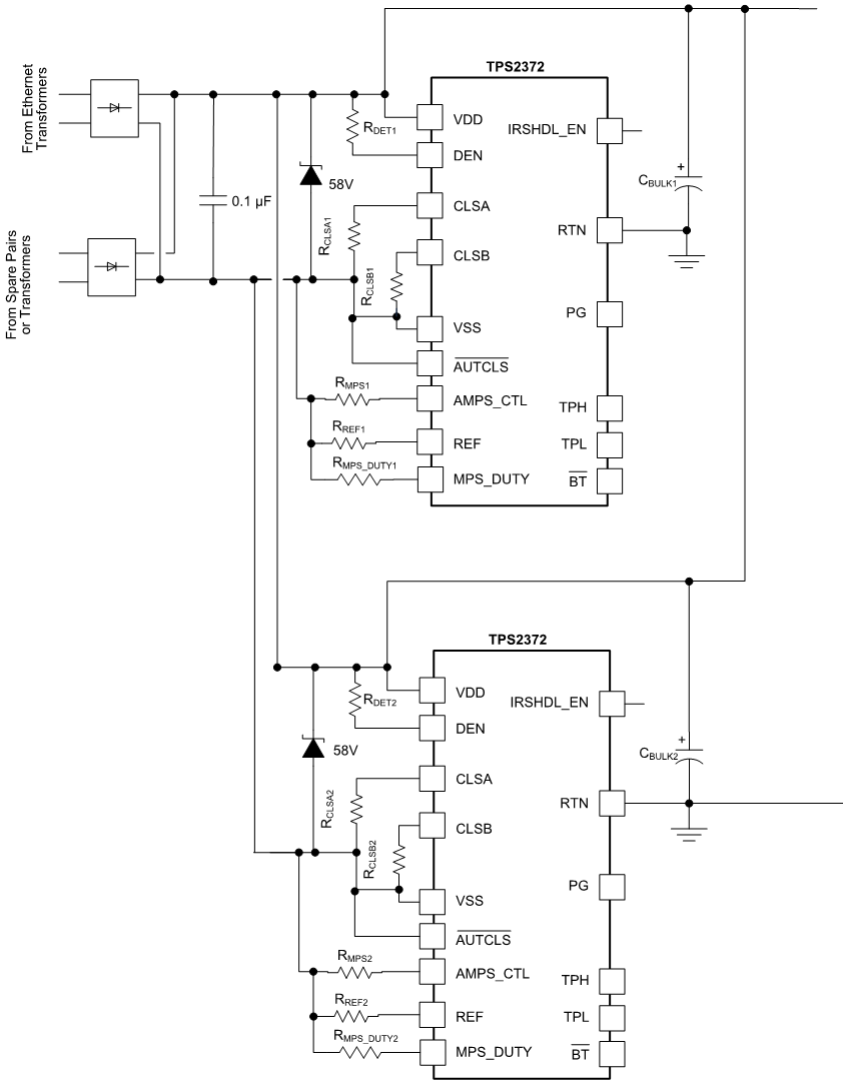

Figure 4. High-Power PD Configuration

3.3.1 Select R_{detx}

Since the two PDs are paralleled from VDD-VSS, it should behave as a single PD. In order to meet the standard detection range, R_{det} of each PD must be set to 50 kΩ to get 25 kΩ for the PSE to detect. Hence R_{detx} = 50 kΩ.

3.3.2 Select R_{CLSA} and R_{CLSB}

Here a non-standard high-power PD is designed as Class 8. During classification, the PSE will measure the voltage on the sense resistor to identify the class current. With the new sense resistor used, the class resistors of A and B both need to be modified according to the different specifications of class levels. Because there are two PDs in parallel, the class current is doubled which should be taken into consideration as well. Table 2 shows the new class resistors of each PD for a 110-mΩ PSE sense resistor. As a result, R_{CLSA} = 54.5 Ω and R_{CLSB} = 77.7 Ω so that the Class 8 PD can be identified by the PSE.

Table 2. New Class Resistor for TPS23880 with 110 mΩ Sense Resistor

Class Level	Class Current Range (mA)	New Class Current Lowest (mA)	New Class Current Highest (mA)	New Class Resistor Highest (Ω)	New Class Resistor Lowest (Ω)	New Class Resistor (Ω)
0	0-4	0.00	4.64	Open	539.22	1078.43
1	9-12	10.43	13.91	239.65	179.74	209.69
2	17-20	19.70	23.18	126.87	107.84	117.36
3	26-30	30.14	34.77	82.96	71.90	77.43
4	36-44	41.73	51.00	59.91	49.02	54.47

3.4 Other Design Considerations

1. The layout of the two PDs should be symmetric for a more balancing current sharing.
2. The Data transformer, Ethernet cable, rectifier bridge, and ferrite beads of the PD side should be selected according to the high current.
3. Enable the Auto MPS function of only one PD and increase the MPS amplitude by the multiplying coefficient *k* according to the new sense resistor, if this function is needed. Pay attention that the MPS amplitude should not be larger than the maximum AMPS_CTL current (50 mA) in TPS2372-4.

4 Experimental Results

4.1 Efficiency

Table 3 provides a summary of system performance under different load conditions at 57 Vin. Efficiency (measured at output of parallel PDs and PSE power supply) decreases as power is increased due to I x V and I^2 x R losses. The efficiency is larger than 90% even with a 200-W input through 25 cm Ethernet cable.

Table 3. PSE-CAT5e-PD System Performance Summary

Iin (A)	Vout (V)	Iout (A)	Pin (W)	Pout (W)	Efficiency
0.6250	56.535	0.5890	35.6250	33.2991	0.9347
1.0450	56.190	1.0100	59.5650	56.7519	0.9528
2.1940	55.078	2.1590	125.0580	118.9134	0.9509
2.8370	54.134	2.8000	161.7090	151.5752	0.9373
3.2600	52.665	3.2150	185.8200	169.3180	0.9112
3.5340	52.199	3.4820	201.438	181.75	0.9023

4.2 Detection and Classification

Configure the TPS23880 into semi-auto mode and enable detection and classification, once the non-standard PoE system is all set, the waveforms of the drain voltage and port current can be measured as Figure 5 displays. The PSE will implement a 4-point detection and connection check first and then three fingers are used to identify the class level. All functions are normal and the PD is seen as a valid class 8 PD.

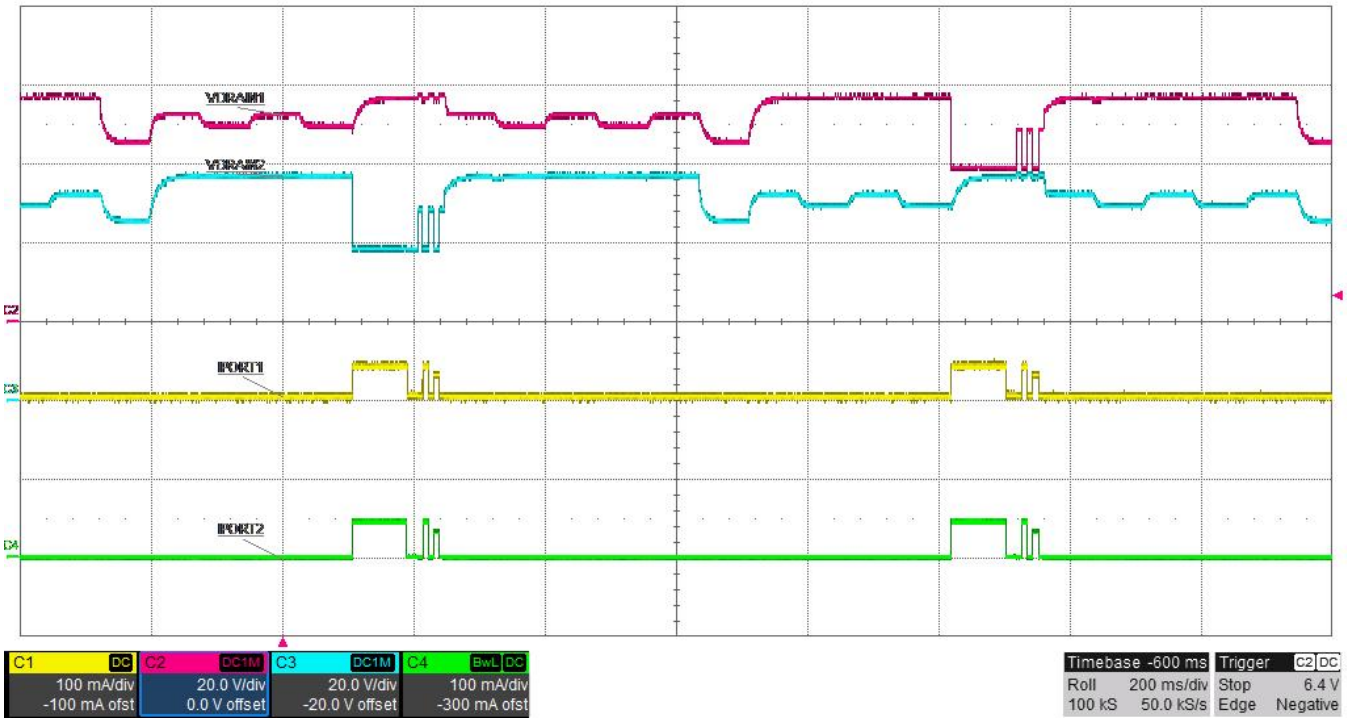

Figure 5. Detection and Classification Waveform

4.3 Power On at No Load

Figure 6 shows the power-on waveforms of the drain voltage and port current by setting the PWON bit in the 19h register. After the command of power on, the PSE will accomplish another detection and then five-finger classification to power on the PD. The inrush current of each channel is limited by its PD.

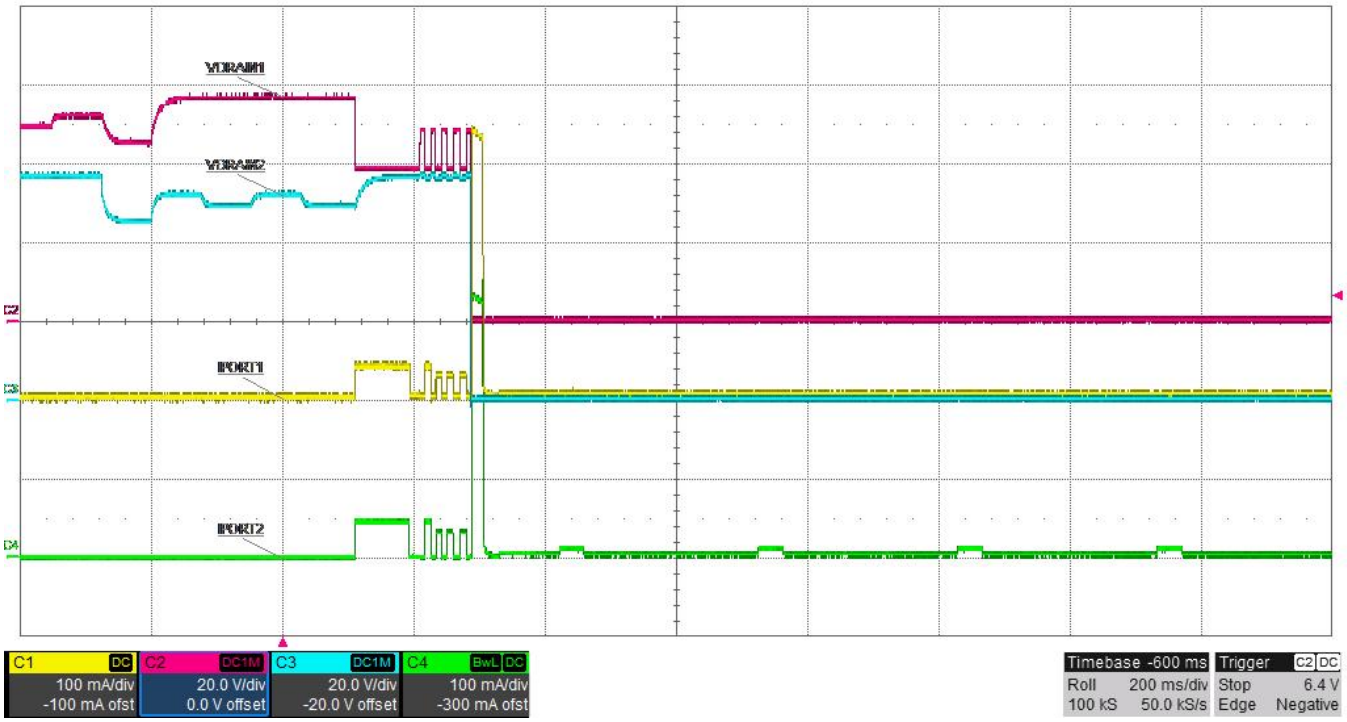

Figure 6. Power On Waveform

4.4 PSE Overload Response

Figure 7 and Figure 8 show a condition that stresses the external MOSFET of the PSE. The voltage of drain, gate and port current are displayed. The PSE regulates the current to ILIM when the load current is increased above ICUT by reducing the voltage on the gate. As a result the voltage of the drain is increasing. In this case, VDS of the FET is 4 V and IDS is 2.8 A for a duration of 6 ms. The PSE FETs must be able to handle this surge as was discussed in the PSE design section.

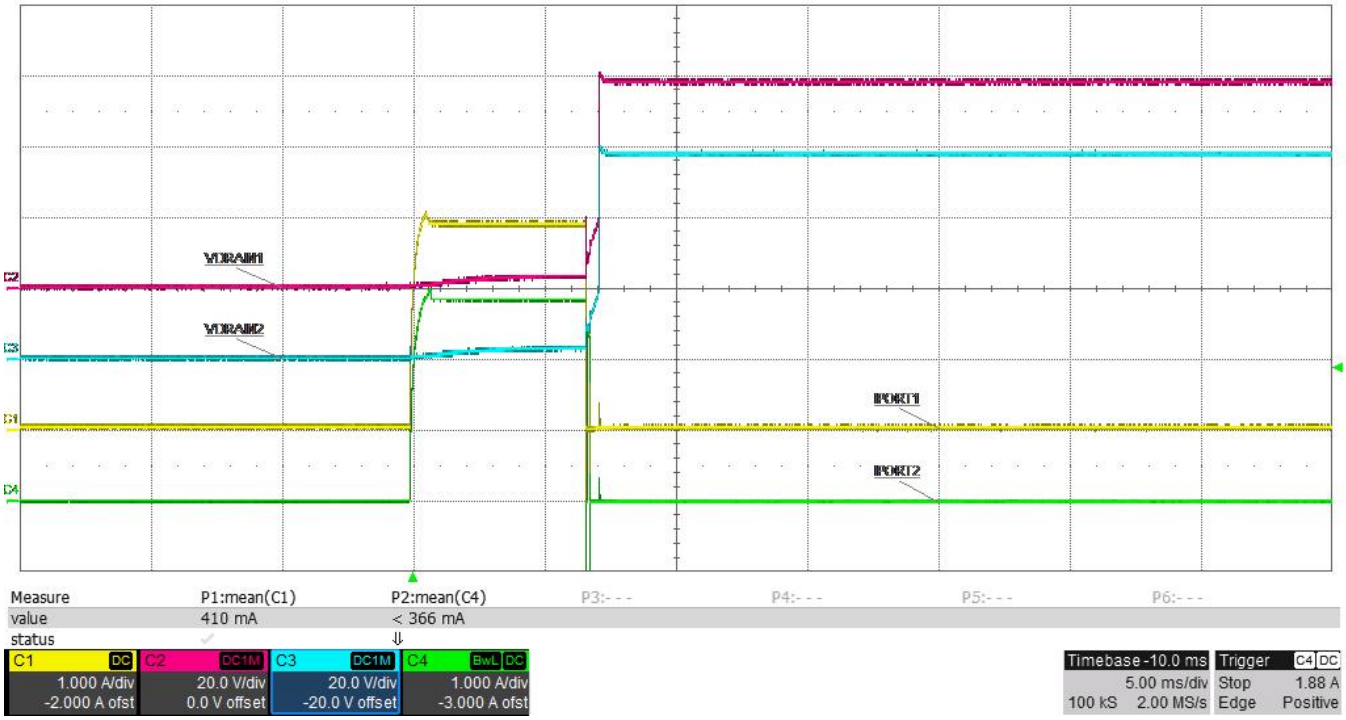

Figure 7. PSE Overload Protection

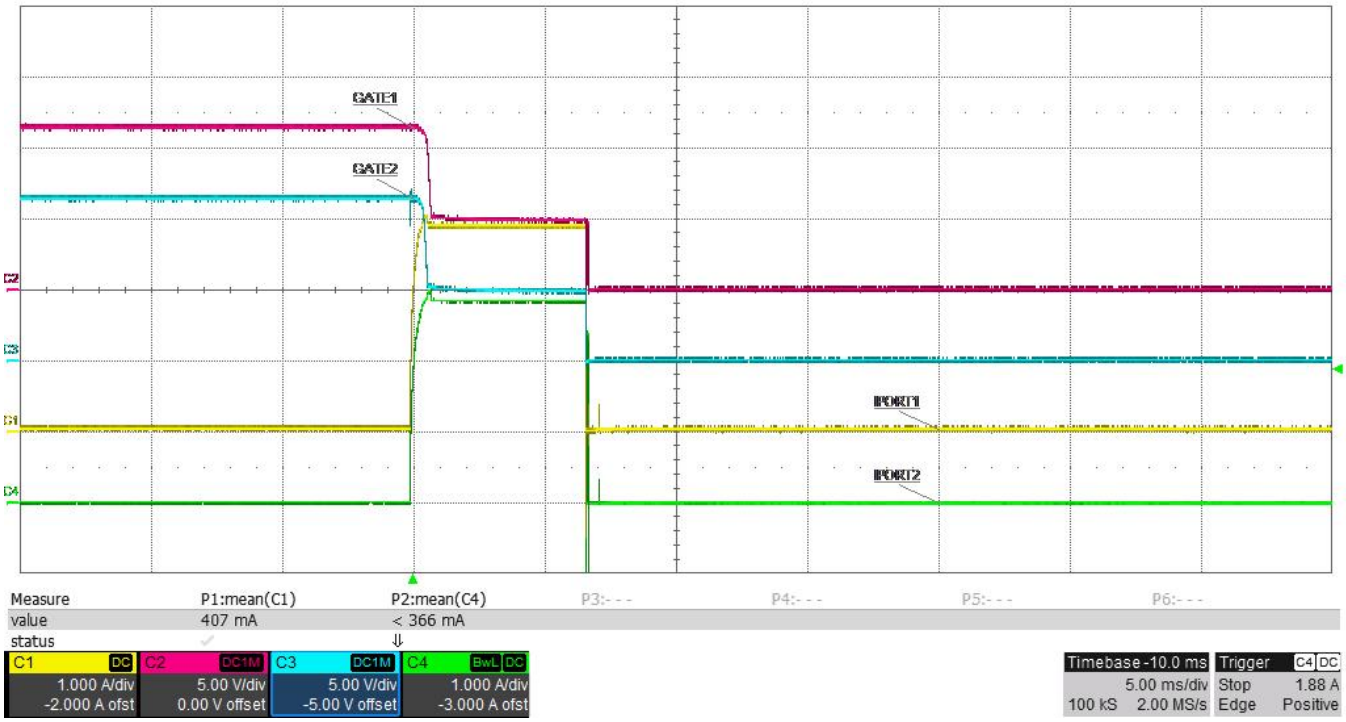

Figure 8. PSE Overload Protection

4.5 PD Overload Response

Figure 9 depicts a condition when the PD load was changed from a light load to 6 Ω. All of the measurements were taken on the PD side, and the signal names refer to pin voltages on the TPS2372-4. During the overload period, the PD will control the gate of the internal hotswap MOSFET to limit the current. As a result the RTN-VSS voltage is rising until it reaches around 14.5 V. Then after a 1.65-ms deglitch, the current limit reverts to the inrush value. The two PDs enter the inrush limited operation.

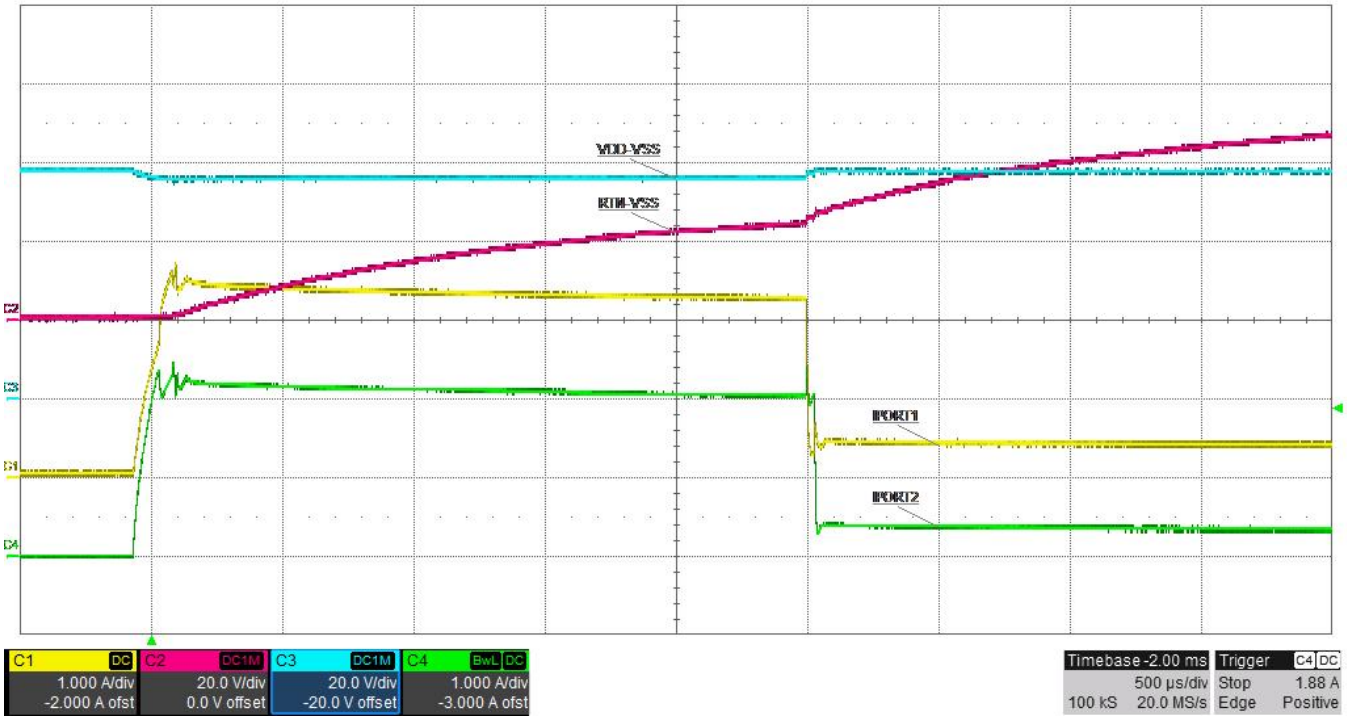

Figure 9. PD Over Load Protection

5 Conclusion

This application report presents a solution for a beyond BT non-standard high-power PoE system using the TPS23880 and TPS2372-4. A 200-W example was provided and its performance was analyzed using the TPS23880EVM-008 and two TPS2372-4EVM-006. It can accomplish normal detection, classification, power on and overload protection on both PSE and PD sides. Users can design their non-standard high-power PoE system based on the procedure above. This PSE solution requires proprietary PD solutions and it can't interoperate with standartd PDs.

6 References

1. *TPS23880 High-Power, 8-Channel, Power-over-Ethernet PSE With Programmable SRAM* Datasheet SLUSD76

2. *TPS2372 High-Power PoE PD Interface with Automatic MPS and Autoclass* Datasheet SLUSCM4

3. *TPS2372-4EVM-006 Evaluation Module* User's Guide SLVUB75

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