How to Load TPS2388x SRAM and Parity Code Over I²C

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The TPS2388x is an 8-channel power sourcing equipment (PSE) controller engineered to insert power onto Ethernet cables in accordance with the IEEE 802.3bt standard. Programmable SRAM enables the in-field firmware upgradability over I²C. This ensures maximum interoperability with the latest PoE enabled devices.

Before sending commands to the TPS2388x, the first thing after power up is to load the SRAM and Parity code. Here are the instructions on how to load it.

If there is more than one TPS2388x device in the system, a global I²C write may be used to load the SRAM and parity code to multiple devices through the global I²C address 0x7F.

The SRAM and parity programming needs to be delayed at least *50 ms* from the initial power on (VPWR and VDD above UVLO) of the device to allow for the device to complete its internal hardware initialization process.

The below procedure applies for either 8-bit (configuration A) or 16-bit (configuration B) I²C operation. The SRAM and parity programming control must be completed at the lower I²C address (Channels 1-4). Configuring SRAM control registers for the upper I²C device address (Channels 5-8) does not program the SRAM or parity.

The latest version of TPS2388x firmware can be accessed from the *TI mySecure Software* webpage.

Table 1. SRAM and Parity Programming Steps During Power Up

	Command	Register	Data	Comments	If Parity Disabled
Step 1	Write	0x60	0x01	Reset the memory address pointer	
Step 2	Write	0x62	0x00	Set start address LSB	
Step 3	Write	0x63	0x80	Set start address MSB	
Step 4	Write	0x60	0xC4	Reset CPU and enable Parity Write	Skip
Step 5	Write	0x61	xx,xx,xx,...	Load Parity data	Skip
After all data is written:					
Step 6	Write	0x60	0xC5	Keep CPU in reset and reset memory pointer	Skip
Step 7	Write	0x62	0x00	Re-Set LSB of start address	Skip
Step 8	Write	0x63	0x80	Re-Set MSB of start address	Skip
Step 9	Write	0x60	0xC0	Keep CPU in reset and enable SRAM I²C write	
Step 10	Write	0x61	xx,xx,xx,...	Load SRAM data	
Step 11	Write	0x60	0x18	Clears CPU reset and enables SRAM and Parity	Write ‘0x08’ instead
Step 12	Delay for approximately 12 ms				
Step 13	Read	0x41		Check firmware version	

Here are the instructions to reload the SRAM and parity code when the device is in safe mode.

Table 2. SRAM and Parity Programming In Safe Mode

	Command	Register	Data	Comments	If Parity Disabled
Step 1	Write	0x60	0x01	Reset the memory address pointer	
Step 2	Write	0x62	0x00	Set start address LSB	
Step 3	Write	0x63	0x80	Set start address MSB	
Step 4	Write	0x60	0x84	*Enable Parity write*	Skip
Step 5	Write	0x61	xx,xx,xx,...	Load Parity data	Skip
After all data is written:					
Step 6	Write	0x60	0x85	Reset memory pointer	Skip
Step 7	Write	0x62	0x00	Re-Set LSB of start address	Skip
Step 8	Write	0x63	0x80	Re-Set MSB of start address	Skip
Step 9	Write	0x60	0x80	Enable SRAM I^2C write	
Step 10	Write	0x61	xx, xx, xx, ...	Load SRAM data	
Step 11	Write	0x60	0x18	Enables SRAM and Parity	Write '0x08' instead
Step 12	Delay for approximately 12 ms				
Step 13	Read	0x41		Check firmware version	

Related Documentation

- Texas Instruments, *TPS23880 High-Power, 8-Channel, Power-over-Ethernet PSE with Programmable SRAM Data Sheet*
- Texas Instruments, *TPS23880EVM-008 User's Guide*
- Texas Instruments, *TPS23880 Product Folder*
- Texas Instruments, *TPS23881 High-power, 8-channel, power-over-ethernet PSE with 200-mΩ RSENSE Data Sheet*
- Texas Instruments, *TPS23881EVM-008 User's Guide*
- Texas Instruments, *TPS23881 Product Folder*
- Texas Instruments, *TPS23882 Type-3 2-Pair 8-Channel PoE PSE Controller with SRAM and 200 mΩ RSENSE Data Sheet*
- Texas Instruments, *TPS23882EVM-008 User's Guide*
- Texas Instruments, *TPS23882 Product Folder*

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