Application Report
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Creating a Dual USB Universal Car Charger From the TPS40170 and Two TPS2511

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ABSTRACT

This application report describes how to design a dual USB Universal Car Charger. The design delivers up to 2.1 A per USB port. The TPS2511 auto-detect feature monitors USB data line voltage, and automatically provides the correct electrical signatures on the data lines to charge compliant devices among the following dedicated charging schemes:

- Divider DCP for Apple devices, required to apply 2.7 V/2.0 V or 2.0 V/2.7 V on the D+/D- lines respectively
- BC1.2 DCP, required to short the D+ line to the D-line
- 1.2 V/1.2 V on the D+/D- lines for Samsung Tablets

The TPS40170 provides the 5-V USB voltage at up to 4.2 A. Due to the small package size and high efficiency, the TPS40170 is able to deliver full power and still meet thermal constraints for the small form-factor design. The form factor of the design complies to the UL standard 2089 and ANSI/SAE J563 specification and is easily adapted to meet other form factors.

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Trademarks

1 Universal Car Charger Design Requirements

Figure 1 shows the front and back of the PMP7390 board.

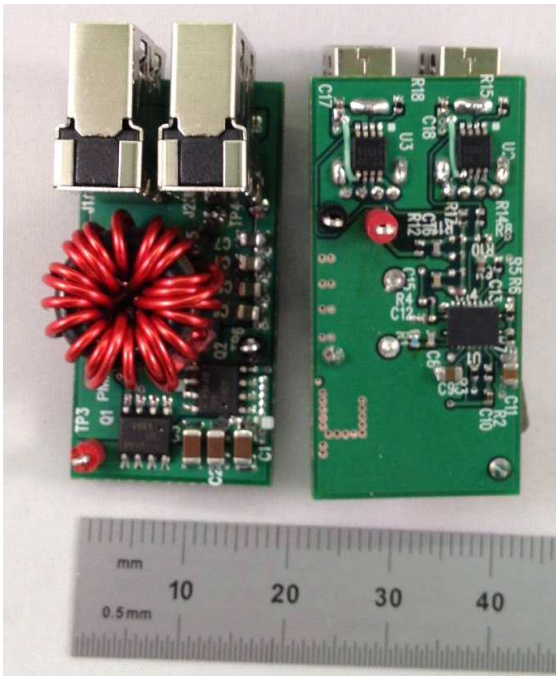

Figure 1. Front and Back of PMP7390 Board

The input voltage supply for a car charger is typically 12 V, but can range from 6 V to 14.5 V with input surges of up to 40 V for multiple 16-ms durations. The power supply must be able to tolerate these surges, and regulate the output to a nominal 5 V with a tolerance of 4.75 V to 5.25 V. Since the USB cable may cause the output voltage to fall at heavy loads, it is desirable to have droop compensation to raise the output voltage during this condition. Short-circuit protection is required in case of a fault with the USB port. The average current consumption depends on the device connected to the USB port, but can be as high as 2.1 A continuously. To handle the 22 W of power delivered to the two ports, a highly efficient synchronous controller with a wide input voltage such as the TPS40170 is needed.

The form factor of the design is an important consideration, allowing easy insertion and removal of the car charger, with little material extending beyond the socket. The form factor must be small enough to meet UL standard 2089 and ANSI/SAE J563 specification. The small form factor is achieved because of the high efficiency of the synchronous TPS40170.

Additionally, to charge devices quickly, the car charger must support the data handshaking protocol required to support USB 2.0 BC1.2 and Divider Mode devices such as the iPod® and iPhone® to allow charging currents as much as four times greater than USB 2.0 allows. Without this handshaking protocol, many handsets and smartphones on the market fail to charge.

This report goes through the step-by-step procedure to design the car charger power supply with the help of a reference design implemented using the TPS40170 and two TPS2511s.

The TPS40170 synchronous converter has the following features:

- Wide Input Voltage Range from 4.5 V to 60 V
- 600-mV Reference Voltage with 1% Accuracy
- Programmable UVLO and Hysteresis
- Voltage Mode Control With Voltage Feed Forward
- Programmable Frequency Between 100 kHz and 600 kHz
- Low-side FET Sensing Overcurrent Protection and High-Side FET Sensing Short-Circuit Protection With Integrated Thermal Compensation
- Thermal Shutdown at 165°C with Hysteresis
- Small 20-Pin 3.5 mm × 3.5 mm QFN (RGY) Package

The TPS2511 USB Charging Port Power Switch and Controller has the following features:

- Meets Battery Charging Specification BC1.2 for DCP.
- Supports Sleep-Mode Charging for most available Apple devices.
- Compatible with USB 2.0 and 3.0 Power Switch requirements.
- 70-mΩ, high-side MOSFET for low power dissipation

2 Input Protection Circuitry

Several different options are available for protecting the car charger from large voltage swings during normal operation, double-battery jump start, or load dump when the battery is disconnected. The lowest cost and simplest approach is to choose a voltage regulator that can tolerate the highest expected voltage. In this case, the TPS40170 is chosen with a 60-V input voltage capability. If additional protection is required against catastrophic failures, a 5-A fuse can be implemented between the input voltage of the converter and the power supply.

3 Switching Power Supply Specifications Using the TPS40170

Consider the following system parameters:

- Output Voltage 5 V
- Transient Response 2 A to 4 A load step V_{OUT} between 4.75 V and 5.25 V (5%)
- Output Current per port: 500 mA for USB, 700 mA for iPhone, 2.1 A for iPad®
- Input Voltage 12-V nominal, 8 V to 60 V
- Output Voltage Ripple 1% of V_{OUT}

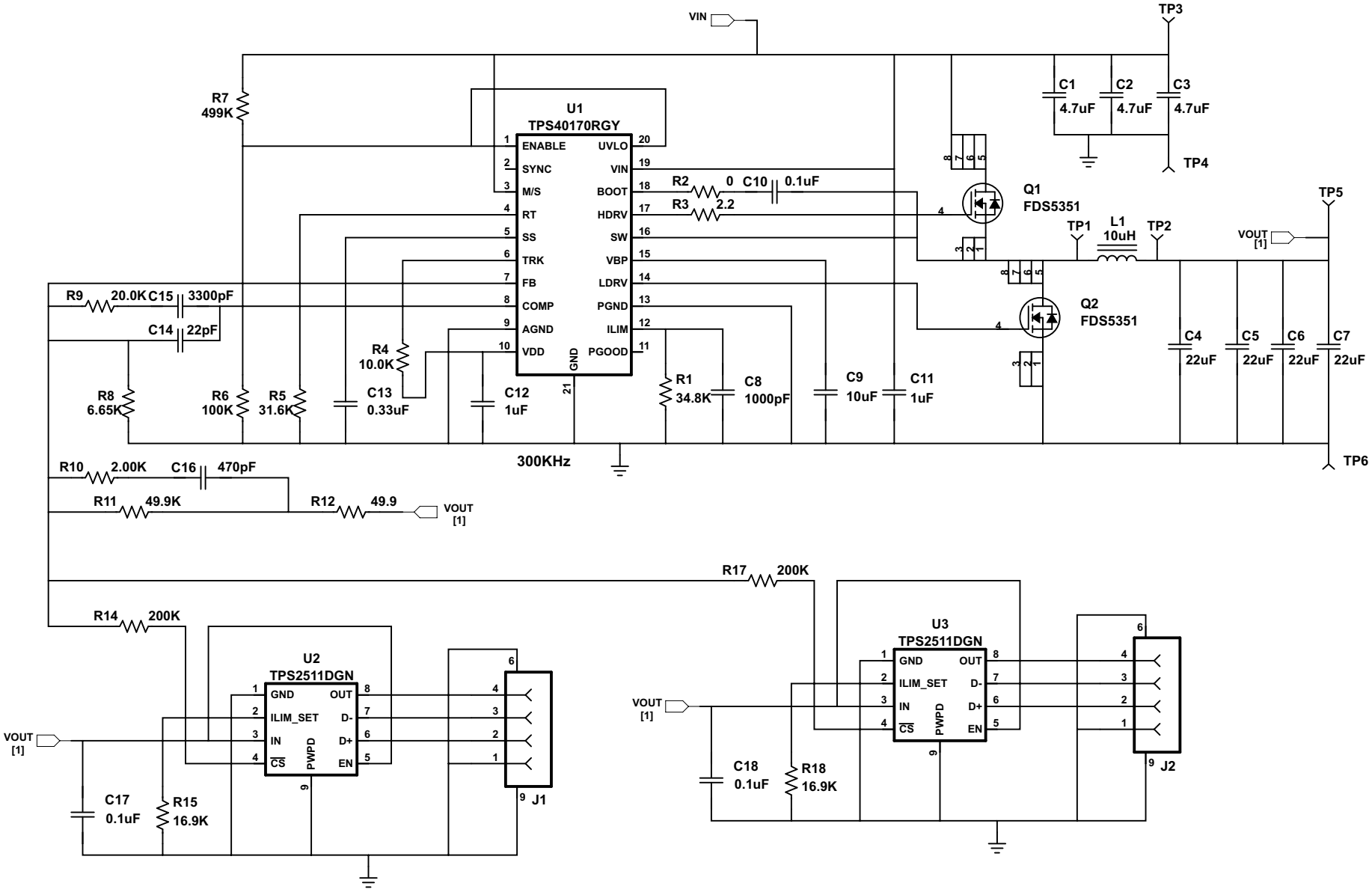

Figure 2. USB Car Charger Input Protection Circuit Schematic

3.1 Selecting a Switching Frequency

Higher switching frequencies enable the use of smaller (and cheaper) output filter components whereas lower switching frequencies tend to have higher efficiencies. They meet both the size and thermal requirements, a suitable switching frequency must be a compromise. The TPS40170 can operate at switching frequencies from 100 kHz to 600 kHz. The design uses a nominal switching frequency of 300 kHz to allow for high efficiency and good thermal performance. The switching frequency is set by placing a resistor, R5, from the RT pin to ground.

The value of R5 is calculated by

$$R_{RT} = \left(\frac{10^4}{f_{SW}}\right) - 2(k\Omega) \tag{1}$$

The calculated value is 31.3 kΩ, so the nearest standard value of 31.6 kΩ is used.

3.2 Output Inductor Selection

Synchronous buck power inductors are typically sized for approximately 20-40% peak-to-peak ripple current. Given this target ripple current, the required inductor size can be calculated.

$$L \approx \frac{V_{IN(max)} - V_{OUT}}{0.3 \times I_{OUT}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{f_{SW}} = \frac{60\,V - 5\,V}{0.3 \times 6\,A} \times \frac{5\,V}{60\,V} \times \frac{1}{300\,kHz} = 8.5\,\mu H \tag{2}$$

The calculated value is 11.5 µH, and a standard value, low cost 10 µH inductor is used. To minimize losses, choose a low-DCR inductor. A compromise between cost and performance resulted in a Torroid inductor with 23 turns of #18AWG wire.

3.3 Output Capacitor Selection

The selection of the output capacitor is typically driven by the output transient response. In this case, the load response is specified as a 5% change in V_{OUT} for a load step from 2 A to 4 A.

$$V_{OVER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta T = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{V_{OUT}} = \frac{(I_{TRAN})^2 \times L}{V_{OUT} \times C_{OUT}} \tag{3}$$

The calculated value is 32 µF. However, since small, low-cost ceramic capacitors are used, they must be derated for DC bias voltage. Choosing four 6.3-V rated, 22-µF capacitors achieves greater than the desired 32-µF output capacitance when the 5-V output is present. By choosing ceramic output capacitors, the ESR max for the allowable output voltage ripple is also met.

3.3.1 Start-up Configuration

The soft-start capacitor provides smooth ramp of the error amplifier reference voltage for controlled start-up. The soft-start capacitor is selected by

$$C_{SS} = \frac{t_{SS}}{0.09} = \frac{4\,ms}{0.09} = 44\,nF \approx 47\,nF \tag{4}$$

Use a 0.33-µF capacitor for a 3-ms soft-start time.

The TPS40170 has an Enable and UVLO function. For this application, these two functions are tied together. The UVLO resistors are calculated by

$$R_7 = \frac{V_{ON} - V_{OFF}}{I_{UVLO}} \tag{5}$$

$$R_6 = R_7 \times \frac{V_{UVLO}}{(V_{ON} - V_{UVLO})} \tag{6}$$

Using 5.5 V as the V_{ON}, 3 V of V_{OFF}, 5 µA for I_{UVLO}, and 0.9 V for V_{UVLO}, the resulting R7 and R6 are 499 kΩ and 100 kΩ, respectively.

The tracking function of the TPS40170 is not used in this design, so the TRK pin is tied to V_{DD} through a 10-kΩ resistor. A 1-µF capacitor must be connected from V_{DD} to Ground.

3.3.2 Peak Current Rating of Inductor

Now that the output inductor and capacitor have been selected, the resulting filter must be checked so the saturation current rating for the inductor is not violated. This is based on the startup charging current for the power supply.

$$I_{CHARGE} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}} = \frac{5\,V \times (2 \times 22\,\mu F + 2 \times 10\,\mu F)}{4\,ms} = 0.08\,A \quad (7)$$

$$I_{L(peak)} = I_{OUT(max)} + (1/2 \times I_{RIPPLE}) + I_{CHARGE} = 6\,A + 1/2 \times 1.86\,A + 0.08\,A = 7.01A \quad (8)$$

Assuming a 3-ms startup time, the charge current is 10 mA. The calculated peak inductor current is 4.93 A.

3.3.3 Input Capacitor Selection

The desired input-voltage ripple for the converter is less than 500 mV. The input voltage ripple is divided between capacitance and ESR. The minimum capacitance and maximum ESR are estimated by

$$C_{IN(min)} = \frac{I_{LOAD} \times V_{OUT}}{V_{RIPPLE(cap)} \times V_{IN} \times f_{SW}} = \frac{6\,A \times 5\,V}{400\,mV \times 10\,V \times 300\,kHz} = 25\,\mu F \quad (9)$$

$$ESR_{MAX} = \frac{V_{RIPPLE(esr)}}{I_{LOAD} + 1/2 \times I_{RIPPLE}} = \frac{100\,mV}{6.93A} = 14.4\,m\Omega \quad (10)$$

$$I_{RMS(cin)} = I_{LOAD} \times \sqrt{D \times (1-D)} = 6\,A \times \sqrt{0.5 \times (1-0.5)} = 3.0\,A \quad (11)$$

Assuming that 90% of the ripple is due to the capacitance, the minimum input capacitance is calculated to be 12.96 µF. The remaining 10% of ripple is due to the ESR of the input caps, and the maximum ESR is calculated to be 10.4 mΩ. The RMS current in the input capacitors is calculated to be 2.07 A. The design uses three 50-V, 4.7-µF ceramic capacitors which meet the minimum capacitance, ESR, and current ratings. A 1-µF bypass capacitor is also placed from V_{IN} to Ground as close to the device as possible. Additionally, a 10-µF capacitor is placed from VBP to Ground.

3.3.4 MOSFET Switch Selection

Using the J/K method for MOSFET optimization, the high-side gate and low-side gate can be selected.

$$J = (10)^{-9} \times \left(\frac{V_{IN} \times I_{OUT}}{I_{DRIVE}} + \frac{Q_G}{Q_{SW}} \times V_{DRIVE} \right) \times f_{SW} \ \left(W/nC \right) \quad (12)$$

$$K = (10)^{-3} \left((I_{OUT})^2 + 1/12 \times (I_{P-P})^2 \right) \times \left(\frac{V_{OUT}}{V_{IN}} \right) \left(W/m\Omega \right) \quad (13)$$

$$K = (10)^{-3} \left((I_{OUT})^2 + 1/12 \times (I_{P-P})^2 \right) \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \left(W/m\Omega \right) \quad (14)$$

$$J = 10^{-9} \left(\frac{V_{FD} \times I_{OUT}}{I_{DRIVE}} + \frac{Q_G}{Q_{SW}} \times V_{DRIVE} \right) \times f_{SW} \ \left(W/nC \right) \quad (15)$$

Optimizing for 300 kHz, 12-V input and 5-V output at 4.2 A, two FDS5351 60-V, 42-mΩ, 6.1-A MOSFETs were chosen for the high side (Q1) and low side (Q2).

3.3.5 Boot-Strap Capacitor

Ensure proper charging of the high-side FET gate by limiting the ripple voltage on the boost capacitor to less than 250 mV.

$$C_{BOOST} = \frac{Q_{G1}}{V_{BOOT(ripple)}} = \frac{25nC}{250mV} = 100nF \quad (16)$$

Assuming a 25 nC gate charge for the upper FET, the Boot capacitor is calculated to be 100 nF.

3.3.6 Current-limit (ILIM) Resistor

The TPS40170 uses the negative drop across the low-side FET at the end of the OFF time to measure the inductor current. Allowing for 25% over the minimum current limit for transient recovery and 20% rise in $R_{DS(on)Q2}$ for self-heating of the MOSFET, the voltage drop across the low-side FET at current limit is given by:

$$v_{oc} = \left(\left(1.25 \times I_{OCP(MIN)}\right) + \left(\frac{1}{2} \times I_{RIPPLE}\right) \right) \times 1.2 \times RDS_{(on)Q2}$$
$$= \left(1.25 \times 4.2A + \tfrac{1}{2} \times 1.86A\right) \times 1.2 \times 42m\Omega = 0.311V \quad (17)$$

Using 4.2 A for the $I_{OCP(min)}$ and 42 mΩ for $R_{DS(on)}$ for the low-side FET, the calculated VOC is 0.311 V. The internal current-limit temperature coefficient helps compensate for the MOSFET RDS(on) temperature coefficient, so the current-limit programming resistor is selected by:

$$R_{CS} = \frac{V_{OC}}{I_{OCSET(min)}} = \frac{0.311V}{9\mu A} = \sim 34.8k\Omega \quad (18)$$

In SLVSB90A, the $I_{OCSET(min)}$ is 9 µA, so the calculated current-set resistor value is 34.8 kΩ. A 1000-pF capacitor is placed in parallel to improve noise immunity of the current-limit set-point.

The short circuit protection level is set to 7 by not connecting any resistor to the LDRV pin.

3.3.7 Feedback and Compensation

Feedback Divider (R8, R11, R14, R17)

Feedback Divider (R8, R11, R14, R17) The TPS40170 controller uses a full operational amplifier with an internally fixed 0.6-V reference. The value of R11 is selected to be between 10 kMΩand 50 kΩ for a balance of feedback current and noise immunity. With the value of R11 set to 49.9 kΩ, the output voltage is programmed with a resistor divider given by Equation 19.

$$R8 = \frac{V_{FB} \times R11}{(V_{OUT} - V_{FB})} = \frac{0.600 \times 49.9}{(5.1V - 0.600V)} \approx 6.65k\Omega \quad (19)$$

The TPS2511 also incorporates a switch to increase the output voltage as the output current is increased. This is used to compensate for voltage drop due to the switch and USB cable. The switch in the TPS2511 is open if the current is less than ½ the current limit setting. Once the current is increased to greater than ½ the current limit setting, the switch closes, placing an additional resistor in parallel with R8. This causes the output voltage to increase. In this case, the values of R14 and R17 are calculated with the following equations

VDroop = 0.15 V

Vout + VDroop = 5.25 V = VFB * (1 + R11/(R8//R14))

R14 = ~200 K

The same value is chosen for R17.

Compensation: (R9, R10, C14, C15, C16)

The TPS40170 compensation uses voltage-mode control with feed forward. With ceramic output capacitors, a type three compensator is used. The following values are obtained using PSpice and lab experiments:

- R9 = 20.0 kΩ
- R10 = 2.00 kΩ

- C14 = 22 pF
- C15 = 3300 pF
- C16 = 470 pF

4 Current-limit Switch Specifications Using the TPS2511

The TPS2511 is operated as a dedicated charging port. Two modes are used, divider mode and BC1.2 mode. Divider mode is used to charge Apple devices. BC1.2 mode is used to charge any BC1.2-mode device; this can include Android phones, Blackberry phones, and other compliant devices. As an optional feature, an LED (D4) provides a status indicator.

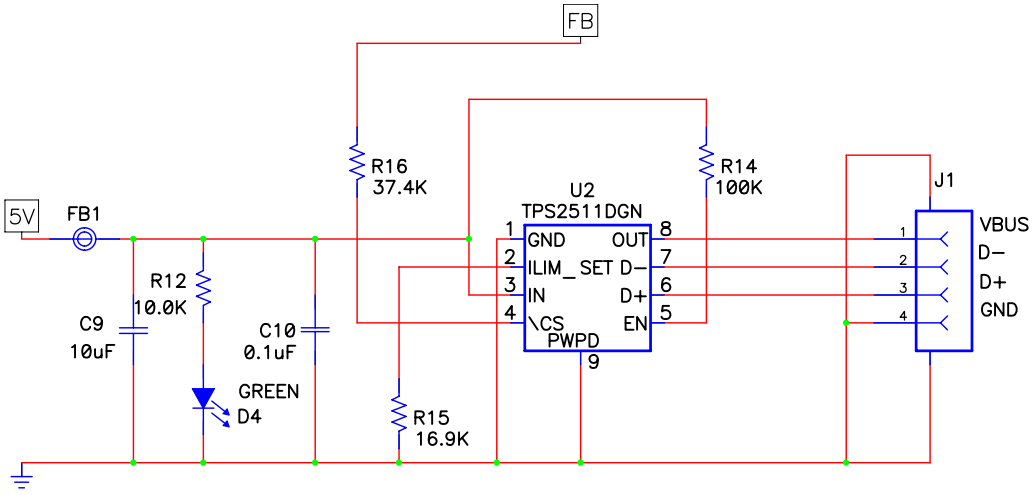

Figure 3. 5-V Output TPS2511 Design Example

4.1 Selecting the Current-limit Resistor

R11 is used to set the current limit for the switch. The current limit is set to the maximum value to ensure that the device provides the full 2.1 A for charging. Equation 20 is used to calculate the nominal short-circuit protection level. Equation 21 and Equation 22 calculate the minimum and maximum protection levels.

$$I_{SHORT} = \frac{51228}{R_{ILIMx}} \quad (20)$$

$$I_{SHORT\_min} = \frac{51228}{R_{ILIMx}^{1.03}} \quad (21)$$

$$I_{SHORT\_max} = \frac{51228}{R_{ILIMx}^{0.967}} \quad (22)$$

4.2 DCP Auto-Detect

The TPS2511 integrates an auto-detect feature supporting Divider mode, short mode and 1.2 V/1.2 V mode. If a divider device is attached, 2.7 V and 2.0 V are presented on the DP and DM pins. If a BC1.2-compliant device is attached, the TPS2511 will automatically switch into short mode. If a device compliant with a 1.2 V/1.2 V charging scheme is attached, 1.2 V will be applied on both DP and DM. The functional diagram of DCP auto-detect is shown in Figure 4 .

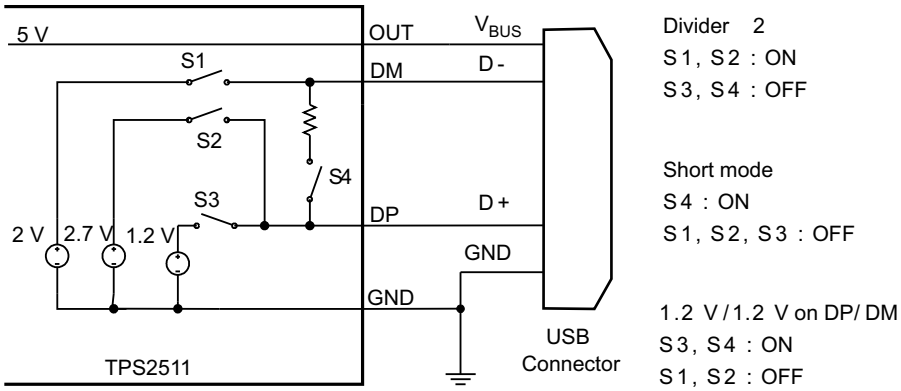

Figure 4. TPS2511 DCP Auto-Detect Functional Diagram

5 Experimental Results

Figure 5 and Figure 6 show the board with 2-A load. The input voltage is 12 V.

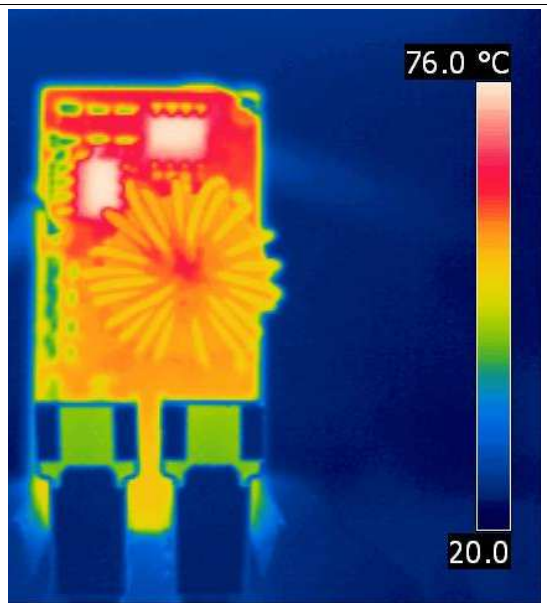

Figure 5. Front Thermal-board Image

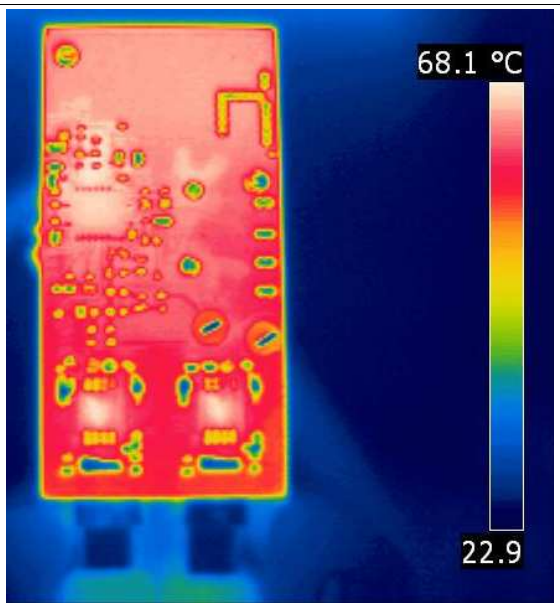

Figure 6. Back Thermal-board Image

5.1 Turn-On - (TPS40170: 5V at 0A)

Figure 7 shows the startup waveforms. The output is not loaded. The timebase is set to 10 ms/division. The input voltage is 12 V. Channel 1 – yellow: 5-V output after the USB switch – (2 V/division), channel 2 – pink: input voltage – (5 V/division)

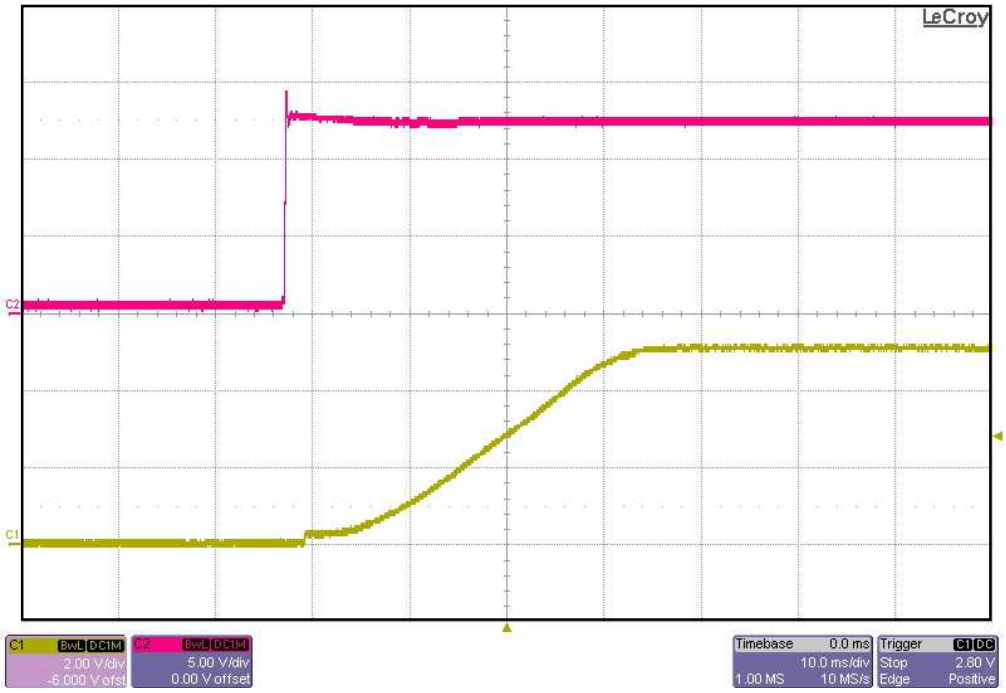

Figure 7. TPS40170

5.2 Output Voltage Ripple – (TPS40170: 5 V at 2.1 A (x2))

Figure 8 shows the output voltage ripple. The input voltage is 12 V. The timebase is set to 2 µs/division. Channel 3 – blue: output voltage ripple – (20 mV/division; AC coupled) channel 4 – green: output current – (2 A/division)

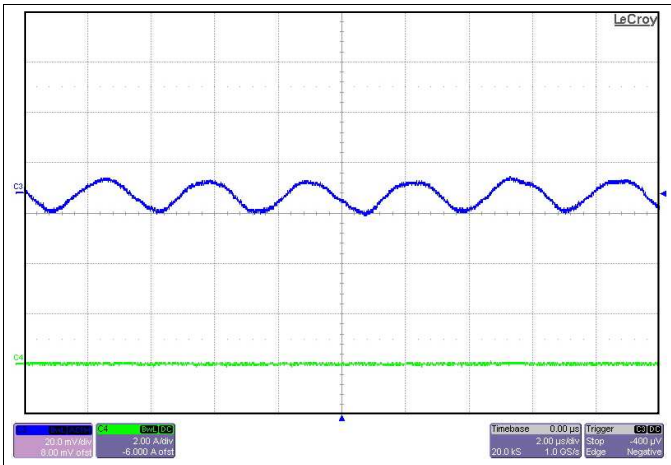

Figure 8. No Load, Measured Before the USB Switch

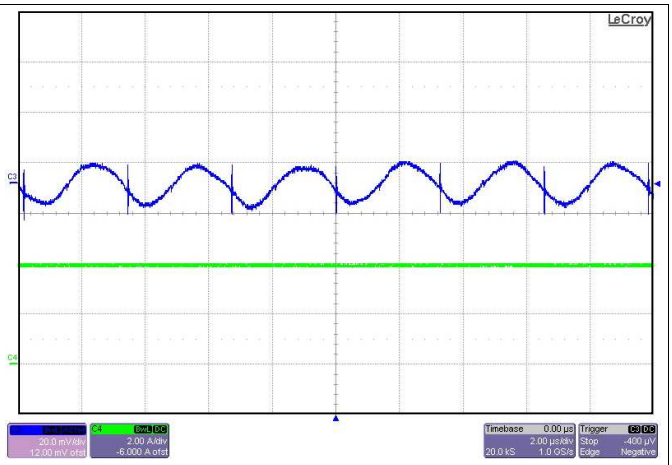

Figure 9. 4.2-A Load, Measured Before the USB Switch

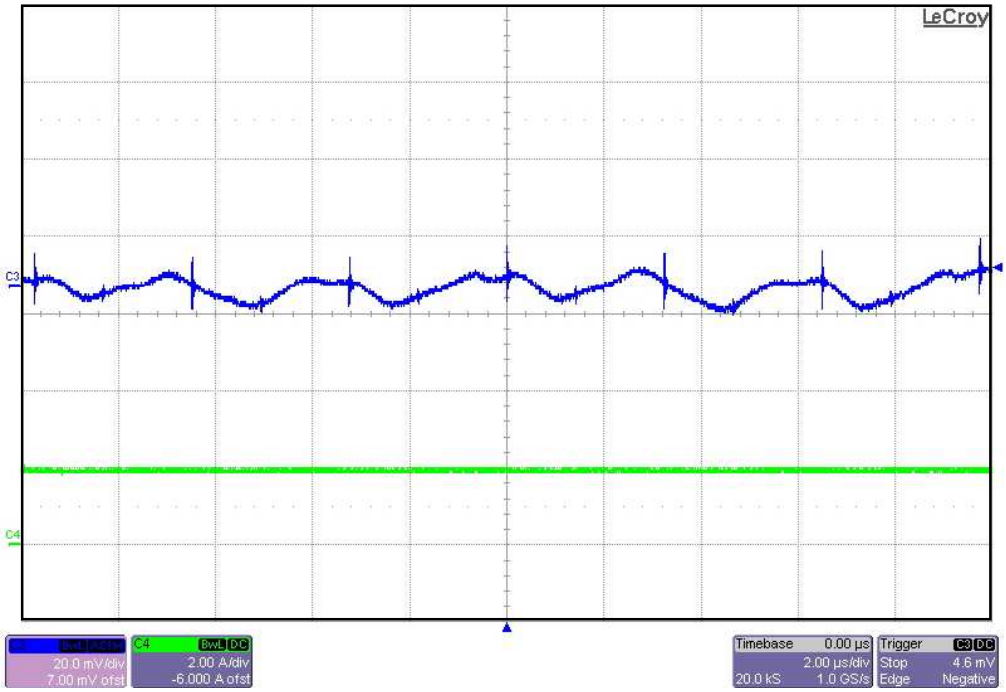

Figure 10. 2.1-A Load, Measured After the USB Switch at the End of an iPhone Cable

5.3 Transient Response – (TPS40170: 5 V at 2.1 A (x2))

The transient response of the converter is shown in the figure below. The input voltage is 12 V. The current is pulsed from 0.1 A to 1 A, 1 A to 2 A and 0.1 A to 2 A. The timebase is set to 2ms/division. The cable droop compensation is set to increase the output voltage 200 mV at ~1.3 A.

Channel 2 – pink: output voltage before the USB switch – (200 mV/division; AC coupled), channel 3 – blue: output voltage after the USB switch – (200 mV/division; AC coupled), channel 4 – green: output current – (1 A/division)

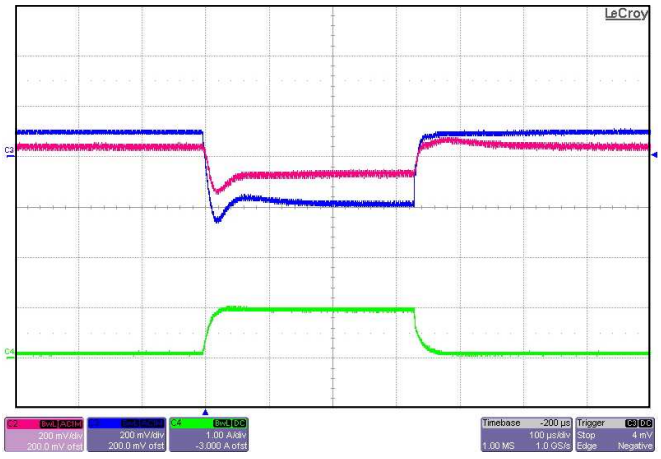

Figure 11. 0.1 A to 1 A (No Cable Droop Compensation)

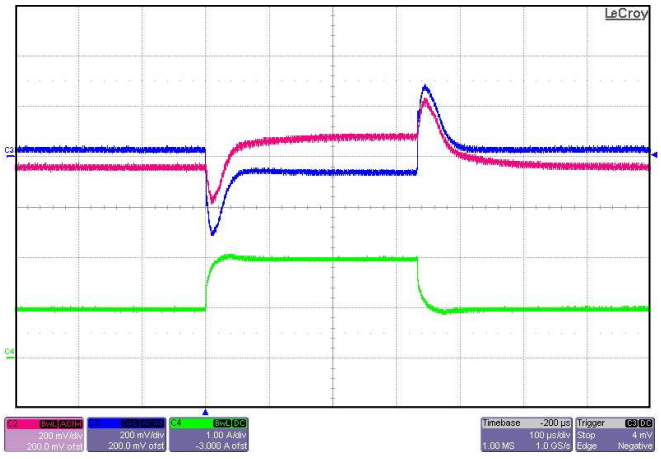

Figure 12. 1 A to 2 A

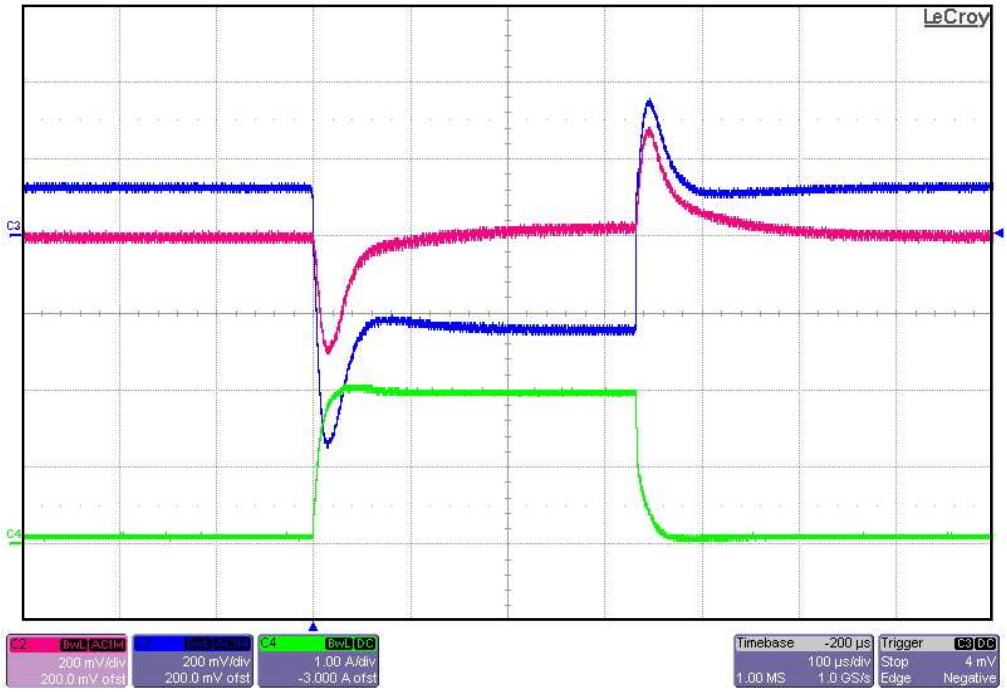

Figure 13. 0.1 A to 2A

5.4 Switching Behavior – (TPS40170: 5 V at 2.1 A (x2))

The switching behavior of the converter is shown in Figure 14 and Figure 15 below. The input voltage is set to 12 V, the output current is set to 4.2 A. The timebase is set to 2 µs/divison.

Channel 1 – yellow: switch node – (5 V/division channel 3 – blue: output voltage before the USB switch – (20 mV/division; AC coupled), channel 4 – green: inductor ripple current – (1 A/division)

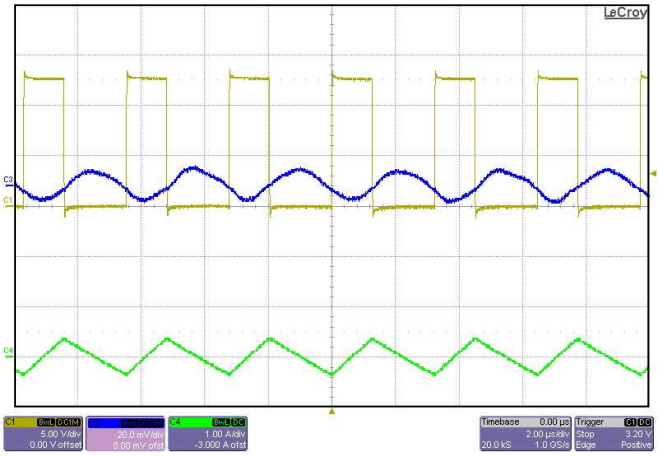

Figure 14. No Load

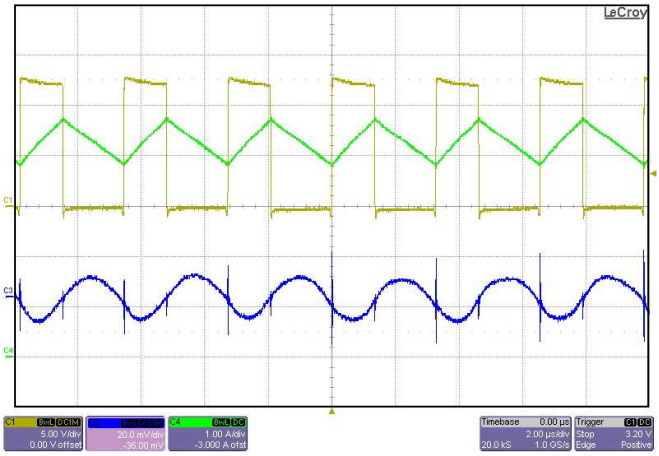

Figure 15. 4.2-A Load

5.5 Efficiency – (TPS40170: 5 V at 2.1 A (x2))

The efficiency of the converter is shown in the figures below.

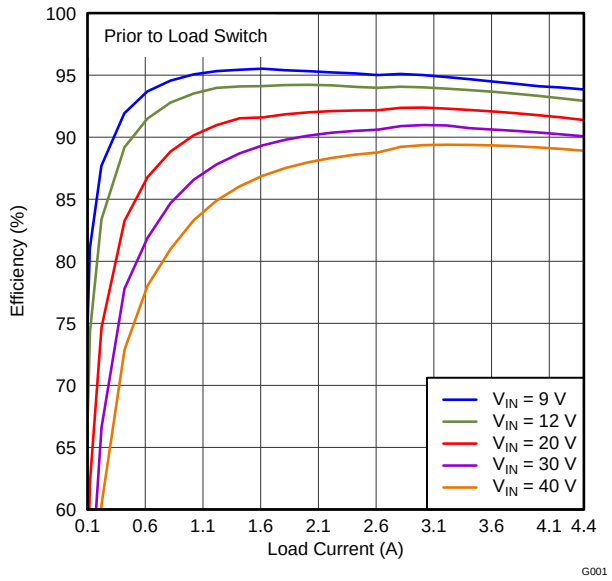

Figure 16. Efficiency Before the USB Switch

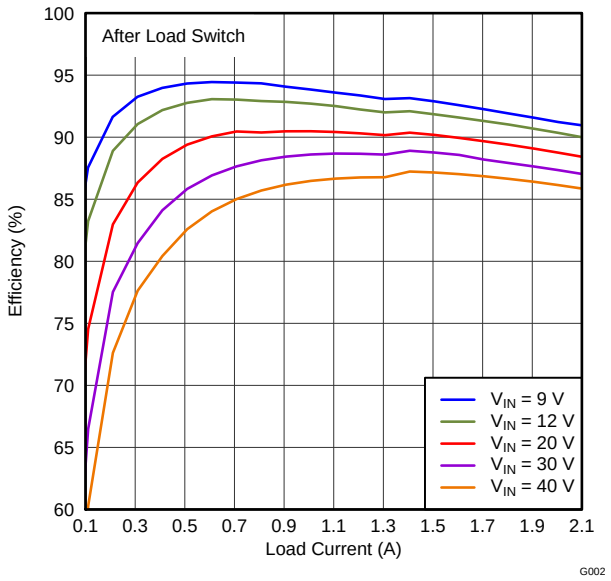

Figure 17. Efficiency After the USB Switch

5.6 Load Regulation – (TPS40170: 5 V at 2.1 A (x2))

The load regulation of the converter is shown in Figure 18.

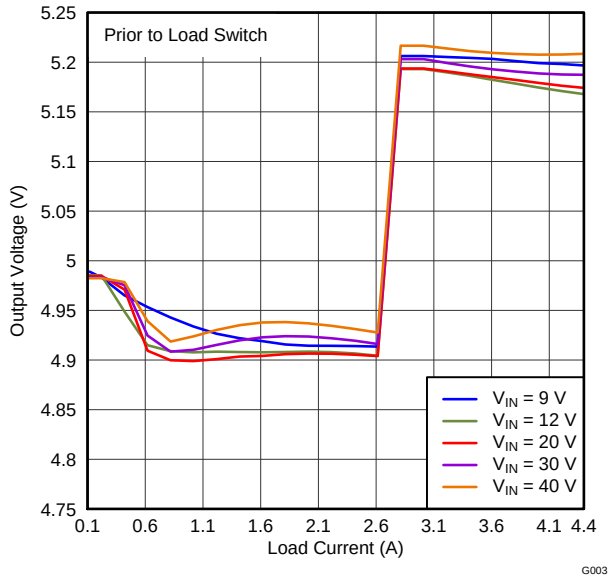

Figure 18. Output Load Regulation Before the USB Switch

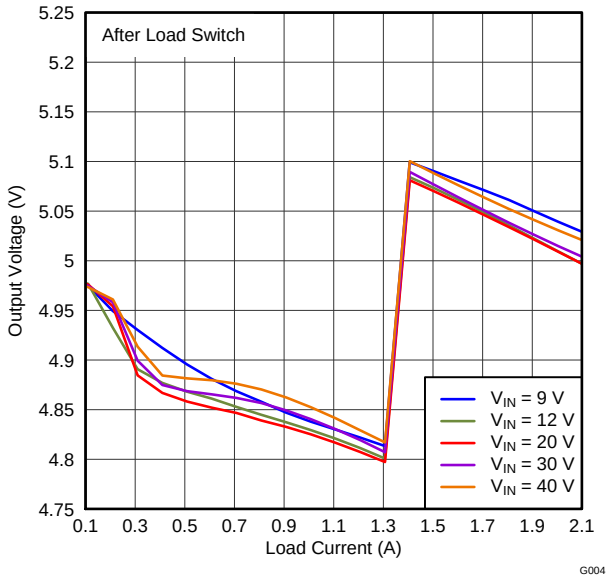

Figure 19. Output Load Regulation After the USB Switch

6 Board Layout

This section provides a description of the board layout and layer illustrations. The board layout for the reference designs is shown in Figure 20 and Figure 21. The top-side layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and V_{PHASE}. Also on the top layer are connections for the remaining pins of the TPS40170 and a large area filled with ground. The bottom layer contains ground and a signal route for the BOOT capacitor. The top and bottom and internal ground traces are connected with multiple vias placed around the board including six vias directly under the TPS54260 device to provide a thermal path from the top-side ground area to the bottom-side ground plane. The input decoupling capacitor (C3) and bootstrap capacitor (C1) are all located as close as possible to the IC. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace past the output capacitors.

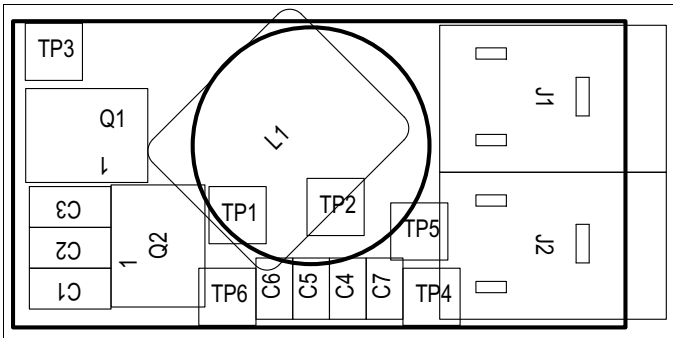

Figure 20. PCB Top Assembly

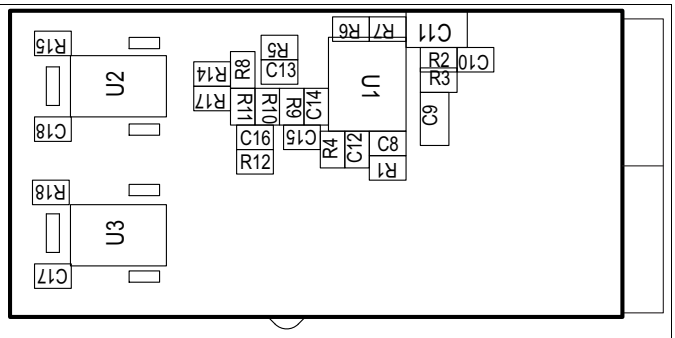

Figure 21. PCB Bottom Assembly

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