Application Report
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Effective System ESD Protection Guidelines TPS254x USB Charging Port Controllers

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ABSTRACT

IEC 61000-4-2 electro-static discharge (ESD) protection of USB charging ports is a necessary system requirement for most products. The USB D+ and D- signals from the charging port controller make direct contact with a potentially charged USB cable and the discharge of energy from the cable to the product can damage the controller. The controller D+, D-, and even VBUS signals must have some form of ESD protection added to the application circuit. This document discusses the design and printed circuit board (PCB) layout of the ESD protection circuitry.

1 Description

The TPS254x family (TPS2540/40A, TPS2541/41A, TPS2543/43Q1, TPS2546/46Q1) of USB charging port controllers do not incorporate internal IEC 61000-4-2 ESD protection. In order to meet IEC 61000-4-2, level 4, external circuitry must be used. In some cases, protection of the D+ and D- signals starts with a transient voltage suppressor (TVS) and may include a choke. Protection of VBUS can usually be accomplished through the use of the USB required VBUS capacitor, C_{PORT}. The basic protection scheme is shown in Figure 1.

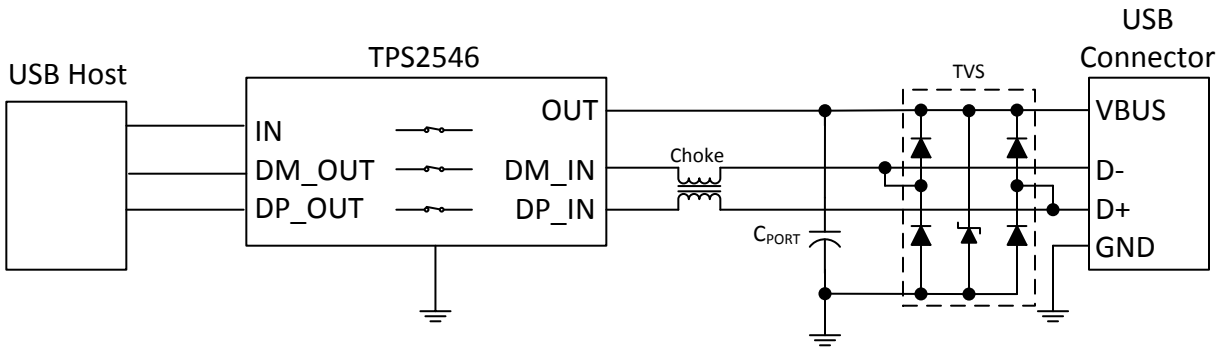

Figure 1. Basic USB ESD Protection Circuit

2 Choosing the TVS

The absolute maximum voltage rating of the TPS254x DP_IN and DM_IN pins with respect to GND ranges from –0.3 V to the lower of V_{IN} + 0.3 V or 5.7 V. For example, if V_{IN} = 5 V, then the maximum rating is 5.3 V. The TVS should clamp the voltage on DP_IN and DM_IN within this voltage range for reliable operation in the presence of ESD surges.

The TVS configuration shown in Figure 1 is one example of an ESD diode array which can clamp D+ and D- between GND and VBUS. The TPD2E001 is used on TPS254x EVMs and benefits from the connection of the TPD2E001 VCC pin to VBUS (and C_{PORT}). For this case, the clamping voltage between GND and VBUS depends on the forward voltage drop of the clamping diodes at peak surge current.

There are alternative options such as the TPD2E2U06 which rely on the clamping voltage of the internal clamp only and do not benefit from a connection to VBUS (and C_{PORT}). An example is shown in Figure 2. This configuration may not protect the TPS254x as the clamping voltage is above the absolute maximum voltage rating of the TPS254x DP_IN and DM_IN pins.

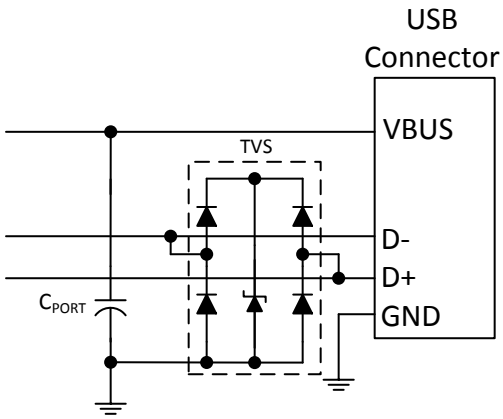

Figure 2. Clamp Type USB ESD Protection Circuit

3 Data Line Choke

In some cases where the signal trace length is far away from the USB connector and TVS, a data line choke may be required. For example, TPS2540EVM-623 incorporates L1 (Coilcraft 0805USB-372ML or Wurth 744231371) to provide additional ESD margin above IEC 61000-4-2, level 4 (±8 kV contact and ±15 kV air discharge). TPS2543EVM-064 also incorporates the L1 choke, but can also meet IEC 61000-4-2, level 4 ESD requirements without the choke. The data line choke also helps suppress EMI generated by the local dc/dc converter.

4 PCB Layout and Routing

4.1 Signal Integrity Considerations

The DP_OUT/DM_OUT, DP_IN/DM_IN traces should be routed as controlled-impedance differential pairs per the USB-2.0 specification. Minimize the use of vias in the high-speed data lines. Place the TPS254x on the bottom side of the PCB so that the connections from DP_IN and DM_IN to the downstream USB connector do not cross. This yields a single via on each connection.

For TPS2543EVM-064, the data pairs are routed as edge-coupled micro-strips on the bottom layer with nominal differential impedance of 90 Ω. The reference plane is tied to GND and is on layer 3 of this four layer PCB. Ensure that the reference plane is void of cuts or splits above the differential pairs to prevent impedance discontinuities. Route through the choke and TVS in a manner that minimizes impedance discontinuities in the high speed traces. Refer to the TPS254xEVM-064 User Guide Layout Guidelines section for the layout example.

4.2 TVS Placement and Hookup

The TVS should be placed close to the downstream USB connector so that ESD energy is shunted back to chassis ground before it can find a discharge path within the end product's internal circuitry. The TVS should be directly connected to the TPS254x DP_IN/DM_IN pins without any vias. Placing the TVS on the same side of the PCB as the TPS254x can help minimize any impedance between the TVS pin and TPS254x pin. Figure 3 shows a poor, good, and best method for connecting TPS254x, TVS and USB connector.

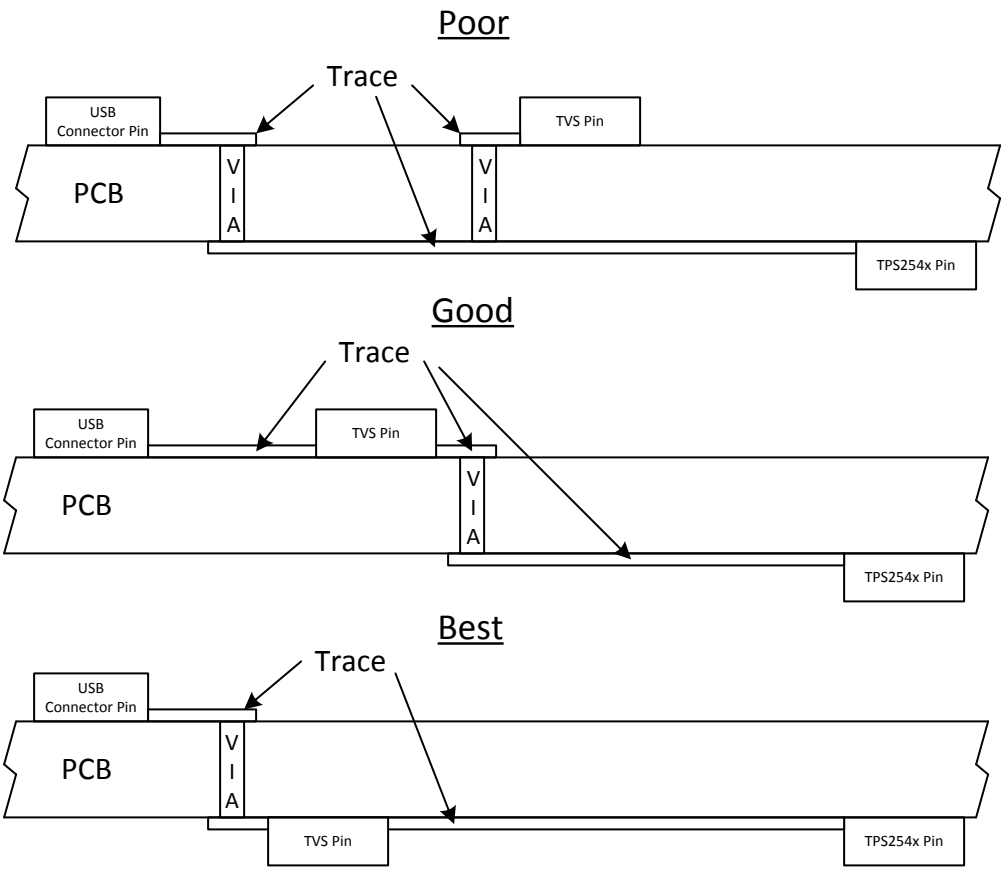

Figure 3. Examples of TVS Placement and Connectivity

Use a heavy connection from TVS VCC and GND pins to VBUS and ground plane respectively. Use multiple vias to make the connection when VBUS and ground are on internal layers.

5 Conclusion

The guidelines in this application report provide a robust solution for ESD suppression in USB charging based devices. Protection up to and above ±8 kV contact and ±15 kV air discharge are achieved by proper PCB layout and choice of the TVS.

6 References

1. Data Sheet: TPS2546 USB Charging Port Controller and Power Switch With Load Detection (SLVSBJ2)
2. Application Report: ESD Protection Layout Guide (SLVA680)
3. Application Report: Design Considerations for System-Level ESD Circuit Protection (SLYT492)
4. User Guide: TPS254xEVM-064 (SLVU660)

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