Latching a Watchdog Timer

Introduction

The purpose of a Watchdog feature in a supervisor is to monitor the watchdog input (WDI) pin. This input is usually driven by a microcontroller output. When the system is running properly, software on the microcontroller regularly toggles, or pulses, a signal output at a specifically defined rate. If the software stops executing properly, this periodically pulsed signal will either speed up, slow down, or stop altogether. When the frequency of the pulsed signal falls outside of a defined window range set on the watchdog timer, the watchdog output ($\overline{WDO}$) is asserted. This active-low output is usually connected to the $\overline{RESET}$ input of the microcontroller, or it may be used to disable some other device via an enable pin. In this way, a watchdog fault causes a reset of the system or controlled function.

In some applications however, such a fault could require further review before the system or function is allowed to resume. In such cases, the $\overline{WDO}$ must latch and remain active and logic low even if the WDI pin begins pulsing again as expected. To clear this latched state requires user intervention.

Such a requirement can often be found in industrial (e.g., motor drive, servo drive, PLC) and automotive safety critical applications (e.g. SIL2 or above).

Latching Watchdog Circuit

Figure 1 shows the latching watchdog circuit which uses a window watchdog timer with a programmable watchdog reset delay pin (CRST) in addition to the WDI and $\overline{WDO}$ pins. Latching this watchdog timer requires one open-drain buffer and a capacitor between the CRST pin and ground. The capacitor adds additional delay before activating $\overline{WDO}$ so the capacitor should be small in value such as 5nF or less but must be above the minimum detectable value of 100pF to successfully latch the watchdog output.

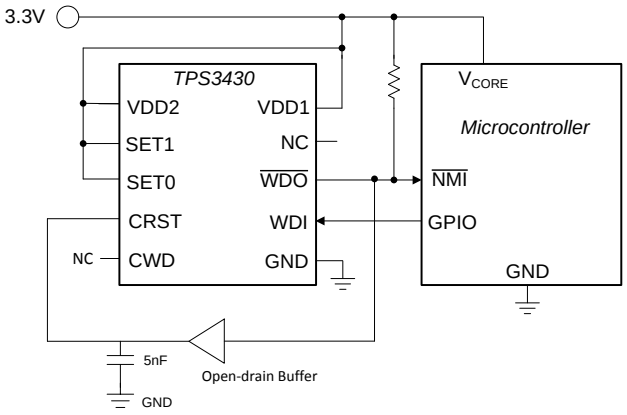

Figure 1. Latching Watchdog Circuit

To understand how this latching watchdog circuit functions, it may be helpful to understand the features of the TPS3430 from the datasheet, SBVS366. The standard operation of the TPS3430 allows the CRST pin to set the watchdog reset delay (t_{RST}) by configuring CRST in one of three ways: connecting a capacitor from CRST to GND, connecting a pull-up resistor from CRST to VDD, or leaving CRST floating. When a watchdog fault occurs on WDI, $\overline{WDO}$ activates to logic low and remains logic low until t_{RST} expires. The configuration of CRST determines the time required for the internal current source to charge up CRST to the internal voltage threshold. Note: if CRST is held logic low by $\overline{WDO}$ or some other external signal, the capacitor connected to the CRST pin can never charge up to the internal reference voltage, and $\overline{WDO}$ will remain logic low as t_{RST} will be infinite.

The way this latching watchdog circuit works is the capacitor connected to the CRST pin charges up to the internal reference voltage upon power up allowing $\overline{WDO}$ to deactivate to logic high suggesting normal operating conditions. Then when a fault occurs, $\overline{WDO}$ activates to logic low and because $\overline{WDO}$ is connected to CRST through the buffer, $\overline{WDO}$ forces the CRST pin to logic low never allowing the capacitor on the CRST pin to charge up to deactivate $\overline{WDO}$ back to logic high thus creating a watchdog fault latch. The next section explains the circuit operation in more detail.

When the voltage rail connected to VDD1 and VDD2 ramps up and crosses $V_{DD\ (min)}$ for the first time, the following sequence of events happen:

1. The watchdog is disabled until t_{RST} expires which is set by the capacitor connected to CRST. The input at the WDI pin is ignored and $\overline{WDO}$ is high-impedance. The watchdog output is logic high due to the external pull-up resistor.

2. After VDD1 and VDD2 are above $V_{DD\ (min)}$, the configuration of the CRST pin is determined and the device recognizes there is a capacitor connected to CRST. The internal current source charges the capacitor connected to the CRST pin which sets the initial watchdog reset delay upon power up. As the input of the buffer is at a high impedance state, the output of the buffer will reflect the same, yielding no effect on the capacitor or internal current source charging it.
3. When the capacitor is fully charged, the watchdog timer will enable $\overline{WDO}$ allowing the watchdog to function correctly and pull $\overline{WDO}$ low if a fault occurs.

In the event of a watchdog input signal fault, the $\overline{WDO}$ activates and goes logic low. This low signal is then passed through the buffer to the CRST pin causing the current from the charged capacitor to sink into ground. The purpose of the buffer is to reject any voltage level on the CRST pin from reflecting back onto the $\overline{WDO}$ pin, ensuring the $\overline{WDO}$ pin stays logic low. With the capacitor drained and the CRST in a low state, the watchdog remains active and logic low and the watchdog timer ignores any input or lack of input from the WDI pin. Because the capacitor can't charge back up due to the buffer holding CRST low, $\overline{WDO}$ will remain active and logic low until the power is removed at VDD. The $\overline{WDO}$ pin latches logic low due to the watchdog fault.

Figure 2 shows the watchdog timer operation with no latch. When a missing pulse on WDI causes a watchdog fault, $\overline{WDO}$ goes active for the delay defined by CRST and coninuously activates and deactivates until the correct timing signal pulses on WDI. Figure 3, in comparison, shows the watchdog timer operation with a latch. When a missing pulse on WDI causes a watchdog fault, $\overline{WDO}$ goes active and remains active permanently until the device is reset regardless of WDI. To reset the circuit, the device must be powered down completely (VDD1 and VDD2 must drop below $V_{DD\ (min)}$) then powered back up.

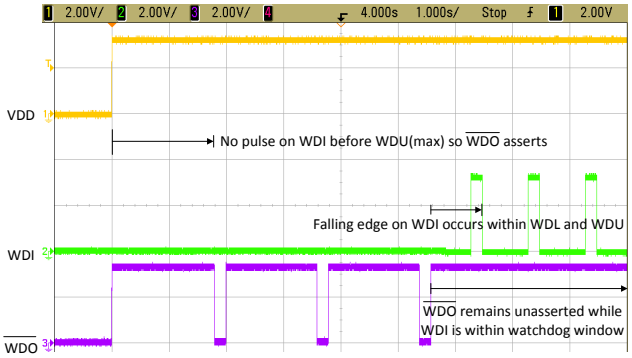

Figure 2. Watchdog Fault Without Latch

Figure 3. Watchdog Fault With Latch

The complete solution uses a Texas Instruments SN74LVC1G07 (or equivalent) and a Texas Instruments TPS3430 window watchdog timer with programmable watchdog timeout and watchdog reset delay. By connecting a SN74LVC1G07 buffer as shown in Figure 1 to the TPS3430, the $\overline{WDO}$ output of the TPS3430 will now be a latching watchdog output.

Related Documentation

TPS3430 Window Watchdog Timer with Programmable Reset Delay data sheet, SBVS366

Table 1. Adjacent Tech Notes

TechNote Title	Literature #
Latching $\overline{RESET}$	SNVA836

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