TEXAS INSTRUMENTS
TPS3899-Q1
SLVSG89A – APRIL 2021 – REVISED SEPTEMBER 2021

TPS3899-Q1 Nano-Power, Precision Voltage Supervisor, Push-Button Monitor with Programmable Sense and Reset Delay

1 Features

Qualified for automotive applications:

- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C7B

Designed for high performance:

- Nano quiescent current: 125 nA (Typical)
- High threshold accuracy: ±0.5% (Typical)
- Built-in precision hysteresis (V_{HYS}): 5% (Typical)

Designed for a wide range of applications:

- Operating voltage range:
  - 0.85 V to 6 V (DL and PL outputs)
  - 1 V to 6 V (PH output)
- Adjustable threshold voltage: 0.505 V (Typical)
- Precision voltage and push-button monitor
- Programmable sense and reset delay
- Fixed (V_{IT-}) voltage: 0.8 V to 5.4 V in 0.1 V steps

Multiple output topologies / Package type:

- TPS3899DL-Q1: open-drain, active-low ($\overline{RESET}$)
- TPS3899PL-Q1: push-pull, active-low ($\overline{RESET}$)
- TPS3899PH-Q1: push-pull, active-high (RESET)
- Package: 1.5-mm × 1.5-mm WSON (DSE)

2 Applications

- Advance Driver Assistance Systems (ADAS)
- Infotainment head unit
- Automotive gateway
- Camera module
- Radar ECU
- Automotive external amplifier

3 Description

The TPS3899-Q1 is a nano power, precision voltage supervisor with ±0.5% threshold accuracy and programmable sense and reset time delay in a 6-pin space saving 1.5 mm × 1.5 mm WSON package. The TPS3899-Q1 is a feature-rich voltage supervisor that offers the smallest total solution size in its class. Built-in hysteresis along with programmable delay prevent false reset signals when monitoring a voltage rail or push button signals.

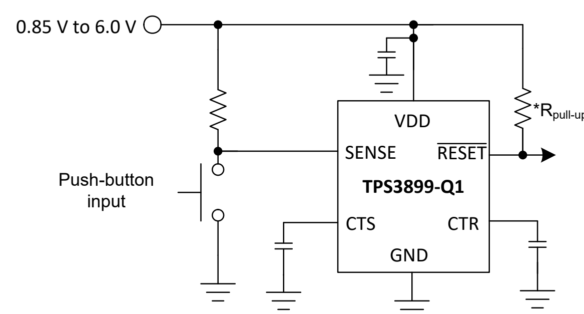
The separate VDD and SENSE pins allow for the redundancy sought by high-reliability systems. SENSE is decoupled from VDD and can monitor rail voltages other than VDD. Optional use of external resistors are supported by the high impedance input of the SENSE pin. Both CTS and CTR provide delay adjustability on the rising and falling edges of the RESET signals. CTS also functions as a debouncer by ignoring voltage glitches on the monitored voltage rails and operates as a "manual reset" that can be used to force a system reset.

The precision performance, best in-class features in a compact form factor, makes the TPS3899-Q1 an ideal solution for wide ranging automotive and battery-powered / low-power applications. The device is fully specified over a temperature range of –40°C to +125°C (T_A).

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TPS3899-Q1	WSON (6) DSE	1.5 mm × 1.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet



*$R_{pull-up}$ is required for open-drain variants only

Typical Application Circuit

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2021) to Revision A (September 2021)	Page
• Production Data Release	1

5 Device Nomenclature

Figure 5-1 shows the device naming nomenclature of the TPS3899-Q1. For all possible output types and threshold voltage options, see Device Naming Convention for a more detailed explanation. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options; minimum order quantities apply.

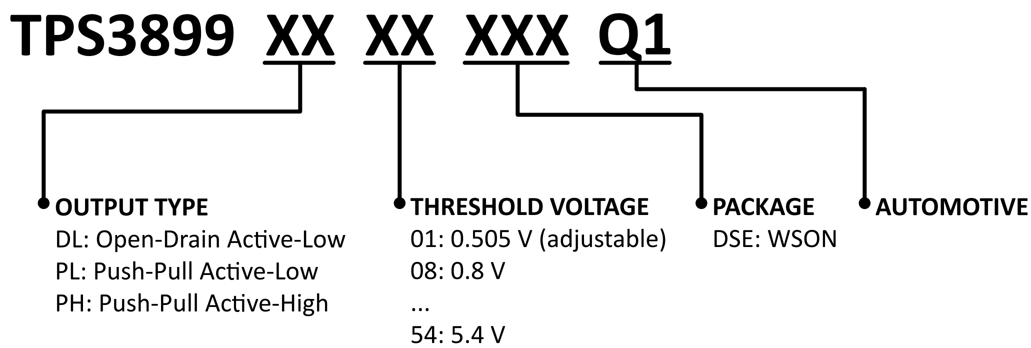


Figure 5-1. Device Naming Nomenclature

6 Pin Configuration and Functions

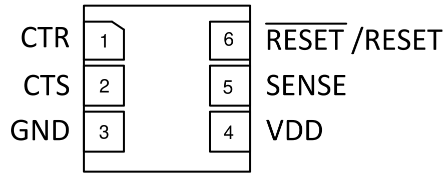


Figure 6-1. DSE Package 6-Pin WSON TPS3899-Q1 (Top View)

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	CTR	—	Capacitor programmable reset delay: The CTR pin offers a user-adjustable delay time when returning from reset condition. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET}}$/RESET delay time to deassert.
2	CTS	—	Capacitor programmable sense delay: The CTS pin offers a user-adjustable delay time when asserting reset condition. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET}}$/RESET delay time to assert.
3	GND	—	Ground
4	VDD	I	Supply voltage pin: Good analog design practice is to place a 0.1-µF decoupling capacitor close to this pin.
5	SENSE	I	This pin is connected to the voltage that will be monitored for fixed variants or to a resistor divider for the adjustable variant. When the voltage on the SENSE pin transitions below the negative threshold voltage V_{IT-}, $\overline{\text{RESET}}$/RESET asserts to active logic after the sense delay set by CTS. When the voltage on the SENSE pin transitions above the positive threshold voltage V_{IT-} + V_{HYS}, $\overline{\text{RESET}}$/RESET releases to inactive logic (deasserts) after the reset delay set by CTR. For noisy applications, placing a 10 nF to 100 nF ceramic capacitor close to this pin may be needed for optimum performance.
6	$\overline{\text{RESET}}$	O	$\overline{\text{RESET}}$ active-low output that asserts to a logic low state after CTS delay when the monitored voltage on the SENSE pin is lower than the negative threshold voltage V_{IT-}. $\overline{\text{RESET}}$ remains logic low (asserted) until the SENSE input rises above V_{IT-} + V_{HYS} and the CTR reset delay expires.
6	RESET	O	RESET active-high output that asserts to a logic high state after CTS delay when the monitored voltage on the SENSE pin is lower than the negative threshold voltage V_{IT-}. RESET remains logic high (asserted) until the SENSE input rises above V_{IT-} + V_{HYS} and the CTR reset delay expires.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted [(1)]

		MIN	MAX	UNIT
Voltage	VDD, SENSE, $\overline{RESET}$ (TPS3899DL)	–0.3	6.5	V
Voltage	CTR, CTS, $\overline{RESET}$ (TPS3899PL), RESET (TPS3899PH)	–0.3	V_{DD}+0.3 [(3)]	V
Current	$\overline{RESET}$ pin and RESET pin		±20	mA
Temperature [(2)]	Operating ambient temperature, T_A	–40	125	°C
Temperature [(2)]	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* (*AMR*) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute maximum rated conditions for long periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.
(3) The absolute maximum rating is (VDD + 0.3) V or 6.5 V, whichever is smaller.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 [(1)]	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	VDD, SENSE, $\overline{RESET}$ (TPS3899DL)	0		6	V
Voltage	CTR, CTS, $\overline{RESET}$ (TPS3899PL), RESET (TPS3899PH)	0		VDD	V
Current	$\overline{RESET}$ pin and RESET pin current	0		±5	mA
T_A	Operating free air temperature	–40		125	°C
C_{CTR}	CTR pin capacitor range	0		10	µF
C_{CTS}	CTS pin capacitor range	0		10	µF

7.4 Thermal Information

THERMAL METRIC[(1)]		TPS3899-Q1 DSE 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	214.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	153.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	112.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	111.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

CTR = CTS = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to V_{DD}, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range –40℃ to 125℃, unless otherwise noted. V_{DD} ramp rate ≤ 1 V / µs. Typical values are at T_A = 25℃.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PARAMETERS						
V_{DD}	Input supply voltage (Open Drain Low and Push Pull Low)		0.85		6	V
V_{DD}	Input supply voltage (Push Pull High)		1		6	V
$V_{IT–}$ (1)	Negative-going input threshold range	for all output configs	0.8		5.4	V
$V_{ADJ-VIT–}$	Negative-going input threshold for adjustable sense threshold version			0.505		V
$V_{IT–}$ accuracy	Negative-going input threshold accuracy	$V_{IT–}$ = 0.505 V (ADJ version) or 0.8 V to 1.7 V (Fixed threshold)	–2.5	±0.5	2.5	%
		$V_{IT–}$ = 1.8 V to 5.4 V (Fixed threshold)	–2	±0.5	2	
V_{HYS}	Hysteresis on $V_{IT–}$	$V_{IT–}$ = 0.505 V and 0.8 V	3	5	8	%
		$V_{IT–}$ = 0.9 V to 5.4 V	3	5	7	%
I_{SENSE}	Current into Sense pin, fixed threshold version	V_{DD} = V_{SENSE} = 6 V		0.025	0.1	µA
	Current into Sense pin, ADJ version	V_{DD} = V_{SENSE} = 6 V		0.025	0.05	µA
I_{DD}	Supply current into VDD pin when sense pin is separate	V_{DD} = V_{SENSE} = 6 V $V_{IT–}$ = 0.505 V and 0.8 V to 5.4 V		0.125	1	µA
V_{TH_CTS}	Voltage threshold to stop CTS capacitor charge and assert RESET			0.73 * V_{DD}		V
V_{TH_CTR}	Voltage threshold to stop CTR capacitor charge and deassert RESET			0.73 * V_{DD}		V
R_{CTS}	CTS pin internal pull up resistance		410	500	590	kΩ
R_{CTR}	CTR pin internal pull up resistance		410	500	590	kΩ
TPS3899DL (Open-drain active-low)						
V_{POR}	Power on reset voltage (2)	$V_{OL(max)}$ = 300 mV $I_{\overline{RESET}(Sink)}$ = 15 µA			700	mV
V_{OL}	Low level output voltage	V_{DD} = 0.85 V $I_{\overline{RESET}(Sink)}$ = 15 µA			300	mV
		V_{DD} = 3.3 V $I_{\overline{RESET}(Sink)}$ = 2 mA			300	mV
$I_{lkg(OD)}$	Open-Drain output leakage current	V_{DD} = V_{PULLUP} = 6 V, T_A = –40℃ to 85℃		10	100	nA
		V_{DD} = V_{PULLUP} = 6 V		10	350	nA
TPS3899PL (Push-pull active-low)						
V_{POR}	Power on reset voltage (2)	$V_{OL(max)}$ = 300 mV $I_{\overline{RESET}(Sink)}$ = 15 µA			700	mV
V_{OL}	Low level output voltage	V_{DD} = 0.85 V $I_{\overline{RESET}(Sink)}$ = 15 µA			300	mV
		V_{DD} = 3.3 V $I_{\overline{RESET}(Sink)}$ = 2 mA			300	mV
V_{OH}	High level output voltage	V_{DD} = 1.8 V $I_{\overline{RESET}(Source)}$ = 500 µA	0.8V_{DD}			V
		V_{DD} = 3.3 V $I_{\overline{RESET}(Source)}$ = 500 µA	0.8V_{DD}			V
		V_{DD} = 6 V $I_{\overline{RESET}(Source)}$ = 2 mA	0.8V_{DD}			V

7.5 Electrical Characteristics (continued)

CTR = CTS = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to V_{DD}, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range –40℃ to 125℃, unless otherwise noted. V_{DD} ramp rate ≤ 1 V / µs. Typical values are at T_A = 25℃.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPS3899PH (Push-pull active-high)						
V_{POR}	Power on reset voltage (2)	$V_{OH(min)}$ = 0.8V_{DD} $I_{RESET\ (Source)}$ = 15 uA			900	mV
V_{OL}	Low level output voltage	V_{DD} = 3.3 V $I_{RESET(Sink)}$ = 500 µA			300	mV
		V_{DD} = 6 V $I_{RESET(Sink)}$ = 2 mA			300	mV
V_{OH}	High level output voltage	V_{DD} = 1V $I_{RESET(Sink)}$ = 15 µA	0.8V_{DD}			V
		V_{DD} = 1.5 V $I_{RESET(Sink)}$ = 500 µA	0.8V_{DD}			V
		V_{DD} = 3.3 V $I_{RESET(Sink)}$ = 2 mA	0.8V_{DD}			V

(1) V_{IT-} threshold voltage range from 0.8 V to 5.4 V (for DL, PL) and 1 to 5.4 V (for PH) in 100 mV steps, for released versions see Device Voltage Thresholds table.
(2) Minimum V_{DD} voltage level for a controlled output state. Below V_{POR}, the output cannot be determined.

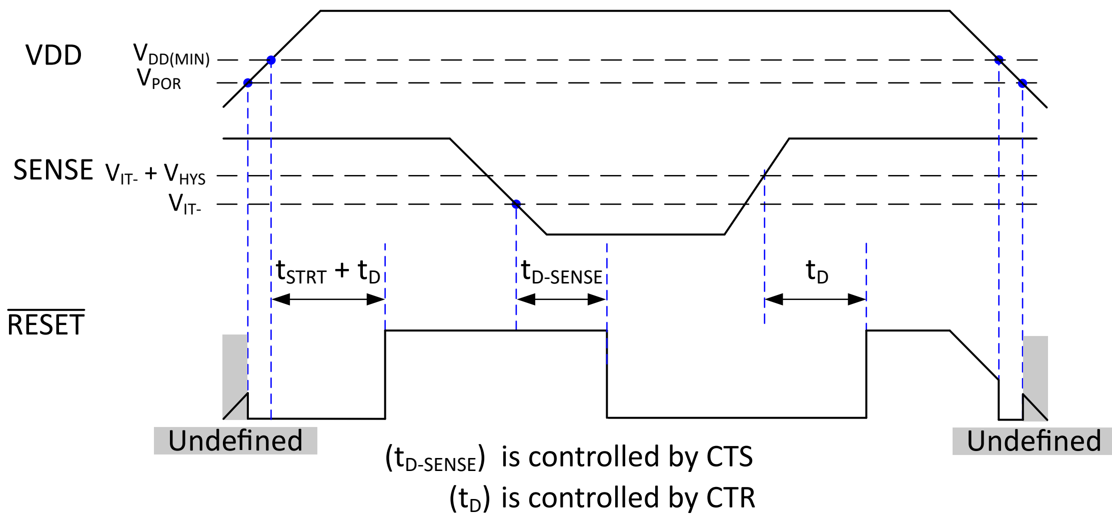
7.6 Timing Requirements

At 0.85 V ≤ V_{DD} ≤ 6 V, CTR = CTS = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to V_{DD}, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range –40°C to 125°C, unless otherwise noted. V_{DD} ramp rate ≤ 1 V / µs. Typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STRT}	Startup Delay (1)	CTR pin = Open or NC			300	µs
$t_{D\text{-}SENSE}$	Detect time delay V_{DD} = (V_{IT+} + 10%) to (V_{IT-} – 10%) (2)	CTS pin = Open or NC		30	50	µs
		CTS pin = 10 nF		6.2		ms
		CTS pin = 1 µF		619		ms
t_D	Reset time delay	CTR pin = Open or NC		40	80	µs
		CTR pin = 10 nF (3)		6.2		ms
		CTR pin = 1 µF (3)		619		ms
t_{GI_VIT-}	Glitch immunity V_{IT-}	5% V_{IT-} overdrive (4)		10		µs

(1) When VDD starts from less than V_{POR} and then exceeds the specified minimum V_{DD}, reset is asserted till startup delay (t_{STRT}) + t_D delay based on capacitor on CTR pin. After this time, the device controls the RESET pin based on the SENSE pin voltage.
(2) t_{D_SENSE} measured from threhold trip point (V_{IT-}) to V_{OL} for active low variants and V_{OH} for active high variants.
(3) Ideal capacitor
(4) Overdrive % = [(V_{DD}/ V_{IT-}) - 1] × 100%

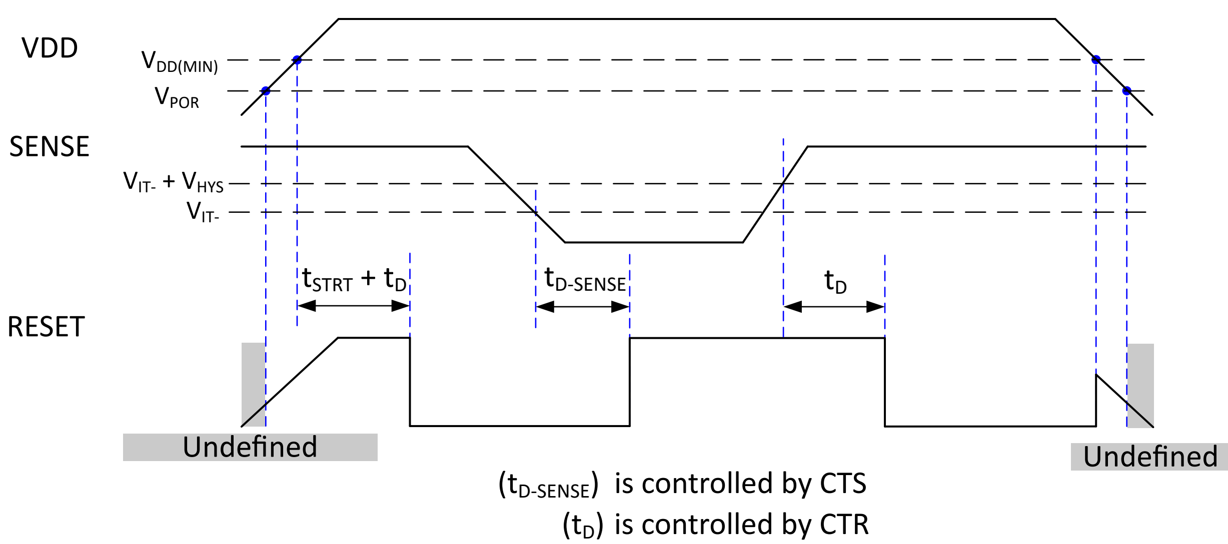
7.7 Timing Diagrams



(1) $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to the CTR pin then t_D programmed time will be added to the startup time.

(2) Be advised, in some instances, that the VDD falling slew rate in Figure 7-1 can be slow or such that VDD decay time is much larger than the SENSE delay time ($t_{D-SENSE}$) time allowing the output to assert. If the VDD falling slew rate is much faster than the ($t_{D-SENSE}$), the output will appear to be not asserted.

Figure 7-1. TPS3899DL01-Q1 and TPS3899PL01-Q1 Timing Diagram



(1) $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to the CTR pin then t_D programmed time will be added to the startup time.

(2) Be advised, in some instances, that the VDD falling slew rate in Figure 7-2 can be slow or such that VDD decay time is much larger than the SENSE delay time ($t_{D-SENSE}$) time allowing the output to assert. If the VDD falling slew rate is much faster than the ($t_{D-SENSE}$), the output will appear to be not asserted.

Figure 7-2. TPS3899PH01-Q1 Timing Diagram

7.8 Typical Characteristics

Typical characteristics show the typical performance of the TPS3899-Q1 device. Test conditions are T_A = 25°C, V_{DD} = 3.3 V, and $R_{pull\text{-}up}$ = 100 kΩ, unless otherwise noted.

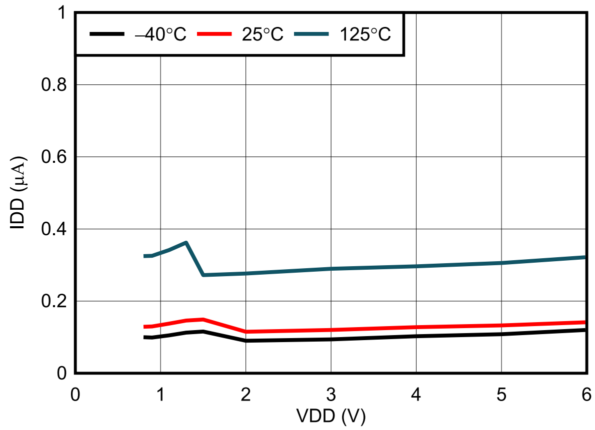


Figure 7-3. Supply Current vs Supply Voltage

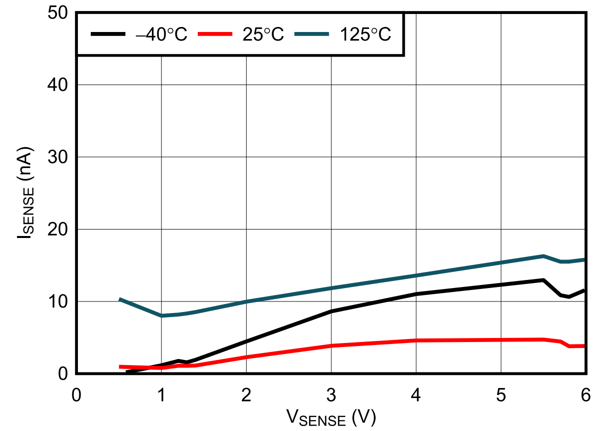


Figure 7-4. SENSE Current vs V_{SENSE}

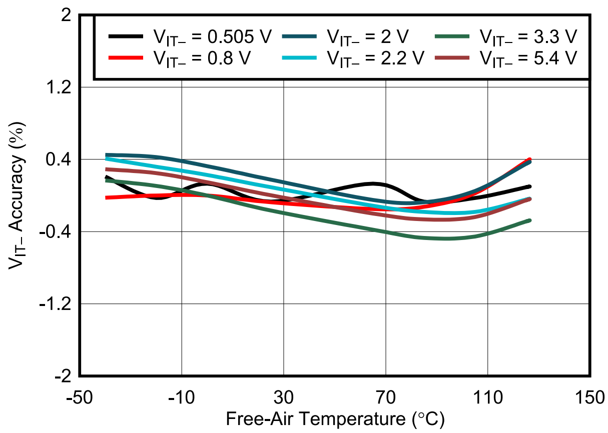


Figure 7-5. V_{IT-} Accuracy vs Temperature

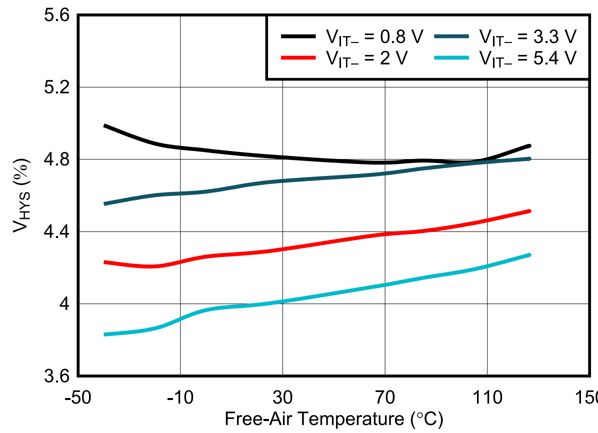


Figure 7-6. V_{HYS} vs Temperature

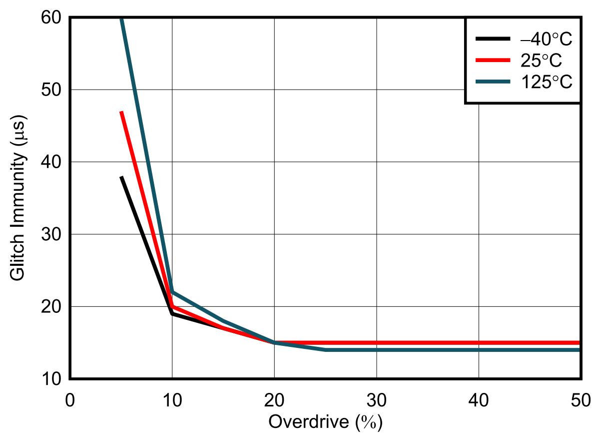


Figure 7-7. SENSE Glitch Immunity (V_{IT-}) vs Overdrive

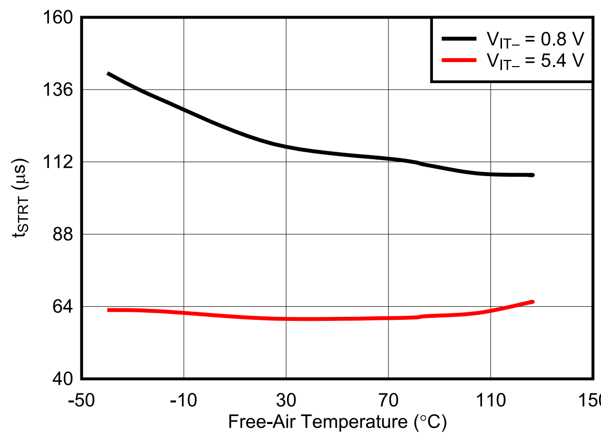
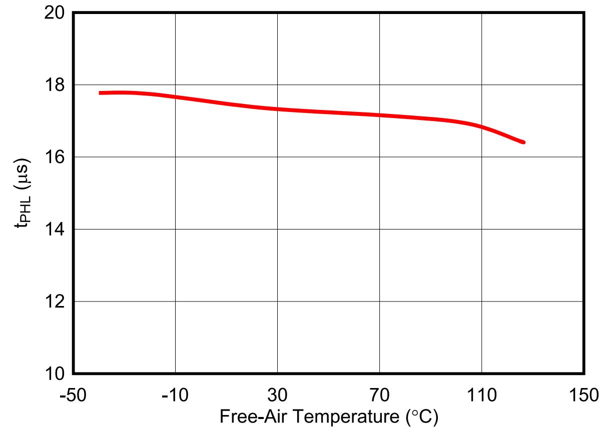


Figure 7-8. Startup Delay vs Temperature

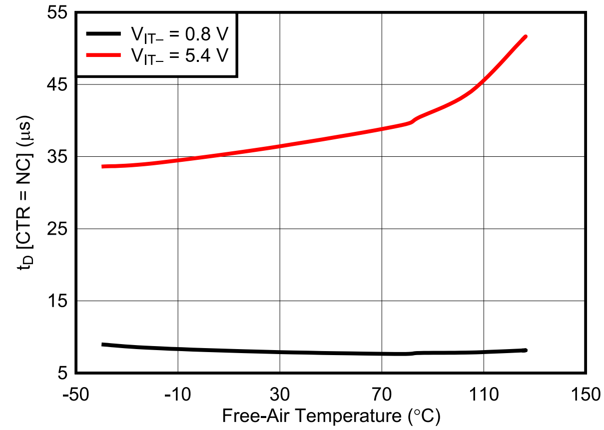
7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3899-Q1 device. Test conditions are T_A = 25°C, V_{DD} = 3.3 V, and $R_{pull\text{-}up}$ = 100 kΩ, unless otherwise noted.



V_{DD} falling below V_{IT-}

Figure 7-9. Propagation Delay vs Temperature



CTR = OPEN

Figure 7-10. Reset Time Delay vs Temperature

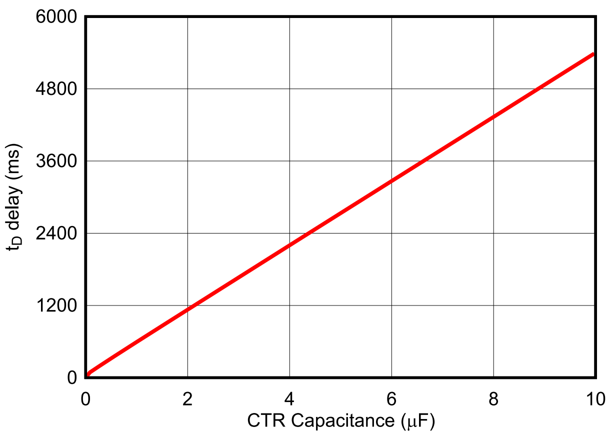
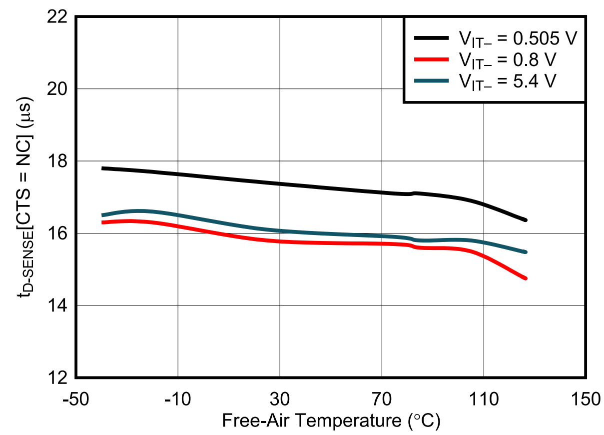


Figure 7-11. RESET Delay vs CTR Capacitance



CTS = OPEN

Figure 7-12. SENSE Delay vs Temperature

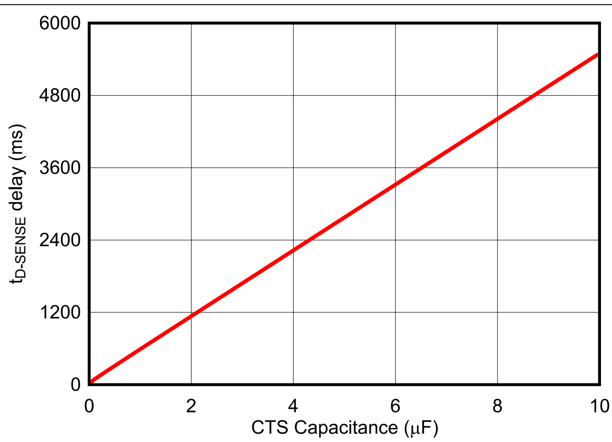


Figure 7-13. SENSE Delay vs CTS Capacitance

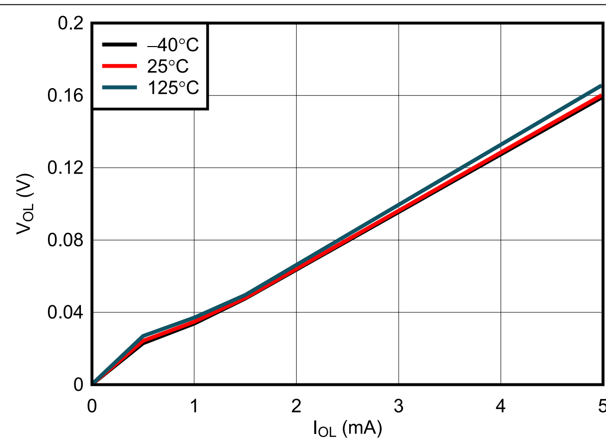


Figure 7-14. V_{OL} vs I_{OL}

7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3899-Q1 device. Test conditions are T_A = 25°C, V_{DD} = 3.3 V, and $R_{pull\text{-}up}$ = 100 kΩ, unless otherwise noted.

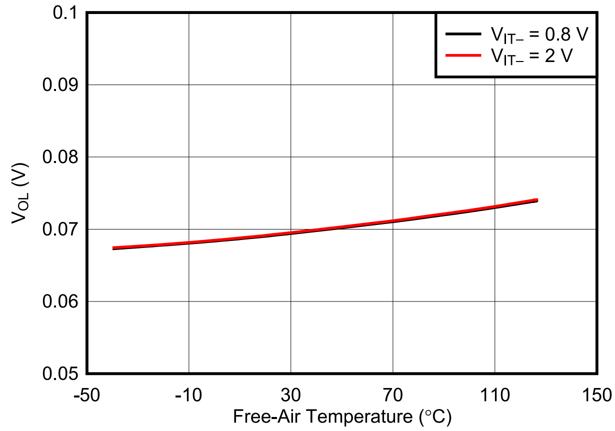


Figure 7-15. V_{OL} vs Temperature

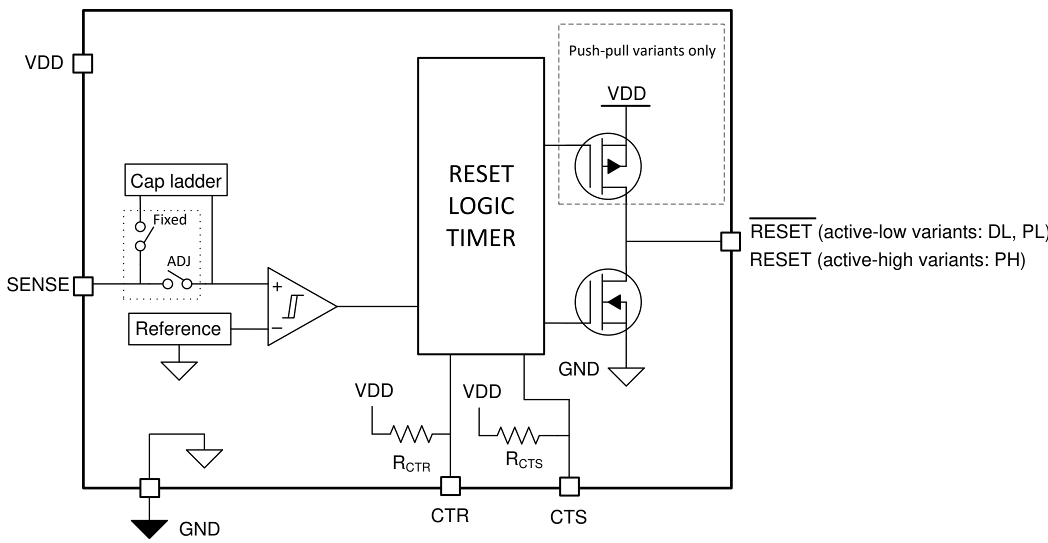
8 Detailed Description

8.1 Overview

The TPS3899-Q1 voltage supervisor with separate SENSE monitor asserts a $\overline{\text{RESET}}$/RESET signal when the SENSE pin voltage drops below V_{IT-} for the duration of the sense delay set by CTS. If the SENSE pin voltage rises above V_{IT-} + V_{HYS} before the sense delay expires, the $\overline{\text{RESET}}$/RESET pin does not assert. When asserted, the $\overline{\text{RESET}}$/RESET output remains asserted until SENSE voltage returns above V_{IT-} + V_{HYS} for the duration of the reset delay set by CTR. If the SENSE pin voltage falls below V_{IT-} before the reset delay expires while $\overline{\text{RESET}}$ is asserted, $\overline{\text{RESET}}$/RESET will remain asserted.

Like most voltage supervisors, the TPS3899-Q1 includes a reset delay t_D to provide time for the power and clocks to settle before letting the processor out of reset. At power up, the circuits inside the TPS3899-Q1 need additional time to start the reset delay timer after its power supply VDD has reached minimum $V_{DD(MIN)}$ for these circuits to start operating properly. This additional time is specified with the parameter start-up delay t_{STRT}. Figure 7-1 shows the timing diagram indicating this additional delay. After VDD is stable and above $V_{DD(MIN)}$ subsequent changes of the sense voltage across the threshold voltage will trigger reset after only the reset delay. The reset time delay t_D is set by a capacitor on the CTR pin. The start-up delay has a maximum limit of 300 μs for a ramp rate of $V_{DD} \leq 1$ V / μs.

8.2 Functional Block Diagram



8.3 Feature Description

The combination of user-adjustable sense delay time via CTS and reset delay time via CTR with a broad range of threshold voltages allow these devices to be used in a wide array of applications. Fixed negative threshold voltages V_{IT-} can be factory set from 0.8 V to 5.4 V in steps of 100 mV [1.1 V to 5.4 V for the -PH (push-pull active high) variants]. CTS and CTR pins allow the sense delay and reset delay to be set to typical values of 30 μs and 40 μs, respectively, by leaving these pins floating. External capacitors can be placed on the CTS and CTR pins to program the sense and reset delays independently.

8.3.1 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD pin falls below V_{IT-} the output reset is asserted. When the voltage at the VDD pin goes above V_{IT-} plus hysteresis (V_{HYS}) the output reset is deasserted after t_D delay.

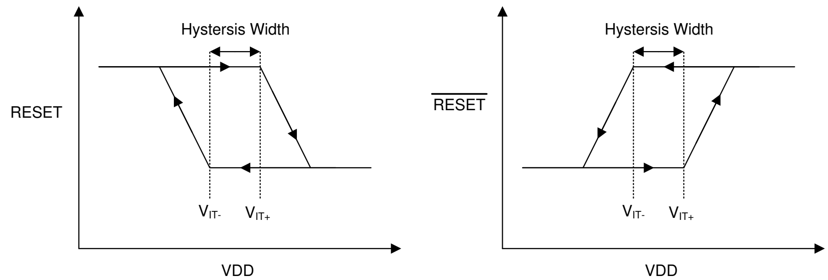


Figure 8-1. Hysteresis Diagram

8.3.2 User-Programmable Sense and Reset Time Delay

The sense delay corresponds to the configuration of CTS and the reset delay corresponds to the configuration of CTR. The sense and reset time delay can be set to a minimum value of 50 µs and 80 µs by leaving the CTS and CTR pins floating respectively, or a maximum value of approximately 6.2 seconds by connecting 10 µF delay capacitor.

The relationship between external capacitor (C_{CT_EXT}) in Farads at CTS or CTR pins and the time delay in seconds is given by Equation 1.

$$t_{D\text{-}SENSE\ (typ)} \text{ or } t_{D\ (typ)} = -\ln(0.29) \times R_{CT\ (typ)} \times C_{CT\_EXT} + t_{D\ (CTS\ or\ CTR\ =\ OPEN)} \quad (1)$$

Equation 1 is simplified to Equation 2 and Equation 3 by plugging $R_{CT\ (typ)}$ and $t_{D\ (CTS\ or\ CTR\ =\ OPEN)}$ given in Section 7.5 and Section 7.6 section:

$$t_{D\text{-}SENSE} = 618937 \times C_{CTS\_EXT} + 50\ \mu s \quad (2)$$

$$t_D = 618937 \times C_{CTR\_EXT} + 80\ \mu s \quad (3)$$

Equation 4 and Equation 5 solves for both external capacitor values (C_{CTS_EXT}) and (C_{CTR_EXT}) in units of Farads where $t_{D\text{-}SENSE}$ and t_D are in units of seconds:

$$C_{CTS\_EXT} = (t_{D\text{-}SENSE} - 50\ \mu s) \div 618937 \quad (4)$$

$$C_{CTR\_EXT} = (t_D - 80\ \mu s) \div 618937 \quad (5)$$

The sense or reset delay varies according to three variables: the external capacitor (C_{CT_EXT}), CTS and CTR pin internal resistance (R_{CT}) provided in Section 7.5, and a constant. The minimum and maximum variance due to the constant is show in Equation 6 and Equation 7:

$$t_{D\text{-}SENSE\ (min)} \text{ or } t_{D\ (min)} = -\ln(0.37) \times R_{CT\ (min)} \times C_{CT\_EXT\ (min)} + t_{D\ (no\ cap,\ min)} \quad (6)$$

$$t_{D\text{-}SENSE\ (max)} \text{ or } t_{D\ (max)} = -\ln(0.25) \times R_{CT\ (max)} \times C_{CT\_EXT\ (max)} + t_{D\ (no\ cap,\ max)} \quad (7)$$

The recommended maximum sense and reset delay capacitors for the TPS3899-Q1 is limited to 10 µF as this ensures there is enough time for either capacitors to fully discharge when a voltage fault occurs. When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before either delay capacitors discharges completely, both delays will be shorter than expected. The capacitors will begin charging from a voltage above zero and resulting in shorter than expected time delays. Larger delay capacitors can be used so long as the capacitors have enough time to fully discharge during the duration of the voltage fault. To ensure the capacitors are fully discharged, the time period or duration of the voltage fault needs to be greater than 10% of the programmed reset time delay.

Figure 8-2 shows the charge and discharge behavior on CTS and CTR that defines the sense and reset delays respectively. When SENSE transitions below V_{IT-}, the capacitor connected to CTS begins to charge. Once the CTS capacitor charges to an internal threshold shown as V_{TH_CTS}, $\overline{RESET}$ transitions to active-low logic state and the CTS capacitor then begins to discharge immediately. When SENSE transitions above V_{IT-} + V_{HYS}, the capacitor connected to CTR begins to charge. Once the CTR capacitor charges to the internal threshold V_{TH_CTR}, $\overline{RESET}$ releases back to inactive logic high state and the CTR capacitor begins to discharge immediately. Please note that for active-high variants, RESET follows the inverse behavior of $\overline{RESET}$.

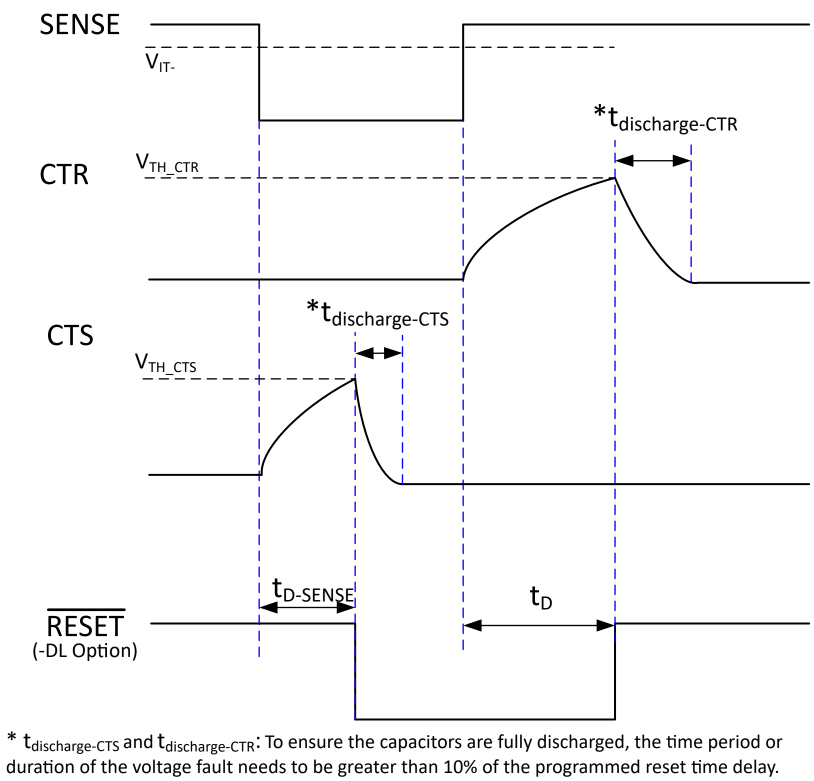


Figure 8-2. CTS and CTR Charge and Discharge Behavior Relative to SENSE and $\overline{RESET}$

Figure 8-3 shows the charge and discharge behavior on CTS and CTR where the monitored voltage is VDD. Similar to Figure 8-2, Figure 8-3 illustrates a SENSE signal that is transitioning below V_{IT-} before the CTR capacitor reaches to an internal threshold voltage V_{TH_CTR} and $t < t_D$. The result of the CTR capacitor not reaching the internal threshold voltage V_{TH_CTR} is $\overline{RESET}$ will become deasserted. Once $\overline{RESET}$ is deasserted, charging beings for the CTS capacitor. When the CTS voltage reaches the internal threshold V_{TH_CTS}, $\overline{RESET}$ will become asserted. This phenomenon is caused by the SENSE falling edge triggering the discharging of the CTR capacitor and producing a deassert signal on the $\overline{RESET}$ output.

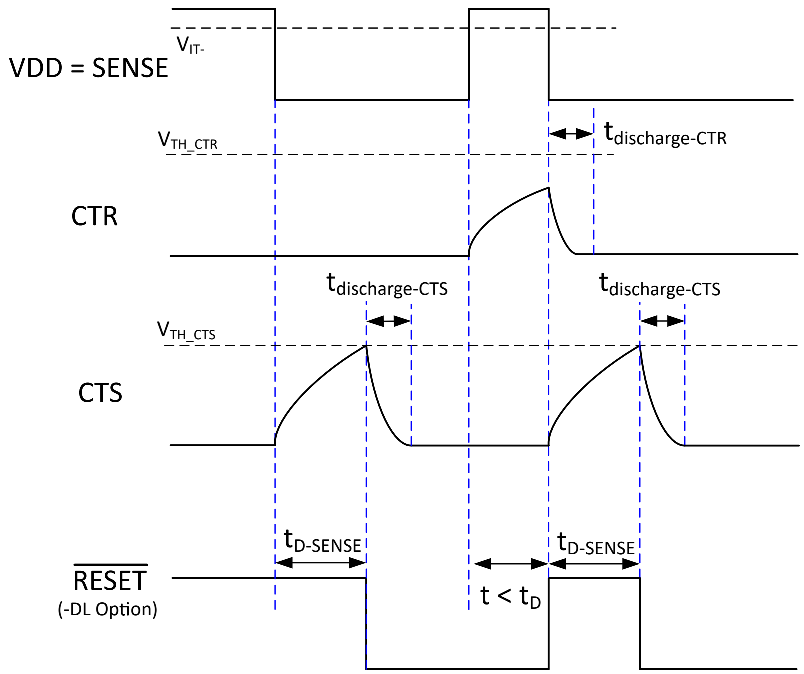


Figure 8-3. CTS and CTR Charge and Discharge Behavior Relative to VDD, SENSE and $\overline{RESET}$

8.3.3 $\overline{RESET}$/RESET Output

Upon power up, $\overline{RESET}$/RESET begins asserted and remains asserted until the SENSE pin voltage rises above the positive voltage threshold $V_{IT-} + V_{HYS}$ for the duration of the reset delay set by CTR. After the SENSE pin voltage is above $V_{IT-} + V_{HYS}$ for the reset delay, $\overline{RESET}$/RESET deasserts. $\overline{RESET}$/RESET remains deasserted long as the SENSE pin voltage is above the positive threshold. If the SENSE pin voltage falls below the negative threshold (V_{IT-}) for the duration of the sense delay set by CTS, then $\overline{RESET}$/RESET is asserted.

An external pull-up resistor is required for the open-drain variants. Connect the external pull-up resistor to the proper voltage rail to enable the outputs to be connected to other devices at the correct interface voltage level. $\overline{RESET}$/RESET can be pulled up to any voltage up to 6.0 V, independent of the device supply voltage.

8.3.4 SENSE Input

The SENSE input can vary from 0 V to 6.0 V, regardless of the device supply voltage used. The SENSE pin is used to monitor a critical voltage rail or push-button input. If the voltage on this pin drops below V_{IT-}, then $\overline{RESET}$/RESET is asserted after the sense delay time set by CTS. When the voltage on the SENSE pin rises above the positive threshold voltage $V_{IT-} + V_{HYS}$, $\overline{RESET}$/RESET deasserts after the reset delay time set by CTR. The internal comparator has built-in hysteresis to ensure well-defined $\overline{RESET}$/RESET assertions and deassertions even when there are small changes on the voltage rail being monitored.

The TPS3899-Q1 device is relatively immune to short transients on the SENSE pin. Glitch immunity ($t_{GI\_V_{IT-}SENSE}$), found in Section 7.6, is dependent on threshold overdrive, as illustrated in Figure 7-7. Although not required in most cases, for noisy applications, good analog design practice is to place a 10 nF to 100 nF bypass capacitor at the SENSE input to reduce sensitivity to transient voltages on the monitored signal.

8.3.4.1 Immunity to SENSE Pin Voltage Transients

The TPS3899-Q1 is immune to short voltage transient spikes on the input pins. To further improve the noise immunity on the SENSE pin, placing a 10 nF to 100 nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal.

Sensitivity to transients depends on both transient duration and overdrive (amplitude) of the transient. Overdrive is defined by how much V_{SENSE} exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the response of the outputs. Threshold overdrive is calculated as a percent of the threshold in question, as shown in Equation 8.

$$\text{Overdrive} = | ((V_{SENSE} / V_{IT-}) - 1) \times 100\% | \quad (8)$$

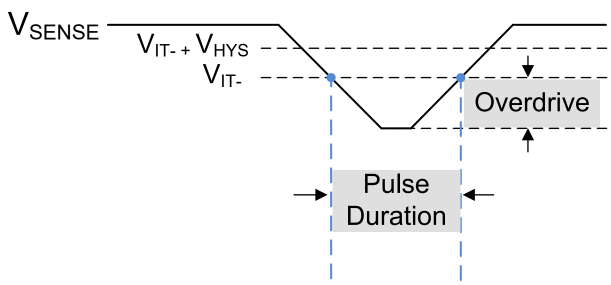


Figure 8-4. Overdrive vs Pulse Duration

8.4 Device Functional Modes

Table 8-1 summarizes the various functional modes of the device.

Table 8-1. Truth Table

V_{DD}	SENSE [(1)]	$\overline{RESET}$	RESET
$V_{DD} < V_{POR}$	—	Undefined	Undefined
$V_{POR} < V_{DD} < V_{DD(MIN)}$ [(2)]	—	L	H
$V_{DD} \geq V_{DD(MIN)}$	$V_{SENSE} < V_{IT-}$	L	H
$V_{DD} \geq V_{DD(MIN)}$	$V_{SENSE} > V_{IT-} + V_{HYS}$	H	L

(1) SENSE pin voltage must be less than V_{IT-} for the sense delay set by CTS or greater than $V_{IT-} + V_{HYS}$ for the reset delay set by CTR before RESET transitions
(2) When V_{DD} falls below $V_{DD(MIN)}$, the internal undervoltage-lockout takes effect and $\overline{RESET}$ is held logic low (RESET is held logic high) until V_{DD} falls below V_{POR} at which the $\overline{RESET}$/RESET output is undefined.

8.4.1 Normal Operation ($V_{DD} > V_{DD(min)}$)

When V_{DD} is greater than $V_{DD(min)}$, the $\overline{RESET}$/RESET pin is determined by the voltage on the SENSE pin and the sense delay and reset delay set by CTS and CTR respectively.

8.4.2 Above Power-On-Reset But Less Than $V_{DD(min)}$ ($V_{POR} < V_{DD} < V_{DD(min)}$)

When the voltage on V_{DD} is less than the $V_{DD(min)}$ voltage, and greater than the power-on-reset voltage V_{POR}, the $\overline{RESET}$/RESET signal is asserted regardless of the voltage on the SENSE pin.

8.4.3 Below Power-On-Reset ($V_{DD} < V_{POR}$)

When the voltage on V_{DD} is lower than V_{POR}, the device does not have enough voltage to assert the output $\overline{RESET}$/RESET to its correct logic state. The output results in being undefined as shown in Figure 7-1 or in Figure 7-2. If the output $\overline{RESET}$/RESET is an open-drain variant, its voltage may be pulled up to V_{DD} or to the pull-up voltage. Neither output should be relied upon for proper device function.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

9.2 Typical Application

9.2.1 Design 1: Dual Rail Monitoring with Power-Up Sequencing

A typical application for the TPS3899-Q1 is voltage rail monitoring and power-up sequencing as shown in Figure 9-1. The TPS3899-Q1 can be used to monitor any rail above 0.8 V. In this design application, two TPS3899-Q1 devices monitor two separate voltage rails and sequences the rails upon power-up. The TPS3899DL01-Q1 is used to monitor the 3.3 V main power rail and the TPS3899PL16-Q1 is used to monitor the 1.8 V rail provided by the LDO for other system peripherals. The $\overline{RESET}$ output of the TPS3899DL01-Q1 is connected to the enable (EN) input of the LDO with an external pull-up resistor $R_{PULL-UP}$ to the 3.3 V power rail. The $\overline{RESET}$ output of the TPS3899PL16-Q1 is connected to the ($\overline{RESET}$) input of the microcontroller. A reset event is initiated on either voltage supervisor when the VDD voltage is less than V_{IT-} falling threshold voltage. For a system reset event, a push-button input is placed at the SENSE pin of the TPS3899DL01-Q1.

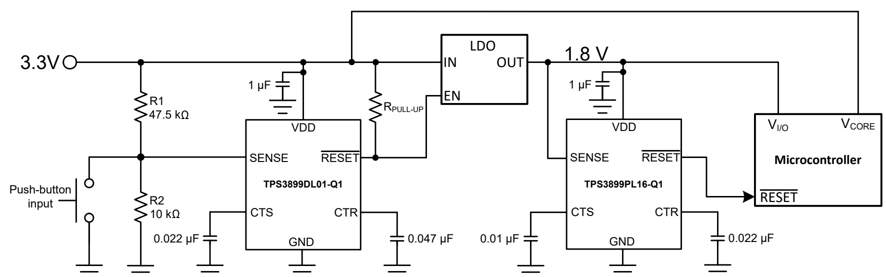


Figure 9-1. TPS3899-Q1 Voltage Rail Monitor and Power-Up Sequencer Design Block Diagram

9.2.1.1 Design Requirements

This design requires voltage supervision on two voltage rails: 3.3 V and 1.8 V. The voltage rails need to sequence upon power up with the 3.3 V coming up at least 25 ms followed by the 1.8 V rail.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Two Rail Voltage Supervision	Monitor 3.3 V and 1.8 V rails	Two TPS3899-Q1 devices provide voltage monitoring with 1% accuracy with either an adjustable threshold device or fixed voltage options available in 0.1 V variations.
Voltage Rail Sequencing	Power up the 3.3 V rail first within 25 ms followed by 1.8 V rail	The CTR capacitors on TPS3899DL01-Q1 and TPS3899PL16-Q1 are set to 0.047 µF and 0.022 µF, respectively, for a reset time delays of 29 ms and 13.7 ms typical.
Reset Asserting and Timing 1	Reset needs to assert under the reset condition of a push-button press or VDD < 2.9 V after a period of 10 ms.	Reset will assert under the reset condition of a push-button press or VDD < 2.9 V after a period of 13.7 ms. The $\overline{RESET}$output will deassert after 29 ms when VDD > 3.05 V.
Reset Asserting and Timing 2	Reset needs to assert under the reset condition of VDD < 1.6 V after a period of 5 ms.	Reset will assert under the reset condition of VDD < 1.6 V after a period of 6.2 ms. The $\overline{RESET}$ output will deassert after 13.7 ms when VDD > 1.68 V.
Max device current consumption	1 µA	Each TPS3899-Q1 requires 125 nA typical.

9.2.1.2 Detailed Design Procedure

The primary constraint for this application is choosing the correct device to monitor the supply voltage of the microprocessor. The TPS3899-Q1 can monitor any voltage with the adjustable voltage threshold option or fixed voltages between 0.8 V and 5.4 V. Depending on how far away from the nominal voltage rail the user wants the voltage supervisor to trigger determines the correct voltage supervisor variant to choose. In this example, Figure 9-2 shows the output, $\overline{RESET}$, of the TPS3899DL01-Q1 when the 3.3 V rail falls to 2.9 V after the sense time delay expires. The TPS3899PL16-Q1 triggers a reset when the 1.8 V rail falls to 1.6 V.

The secondary constraint for this application is the sense and reset time delay. If the monitored voltage rail 3.3 V has large voltage ripple noise and it goes below the programmed threshold voltage but returns above the V_{IT-}+ V_{HYS} before the sense time delay expires, the output will not assert. Therefore, the sense time delay prevents false sense resets by allowing the monitored voltage rail 3.3 V to not assert the output during the programmed sense time delay period set by the capacitor on the CTS pin. In the application, the CTS capacitors for both the TPS3899DL01-Q1 and TPS3899PL16-Q1 are set to be 0.022 µF and 0.01 µF, respectively, and resulted in sense time delays of 13.7 ms and 6.2 ms. In addition to the sense delay time, the reset time delay for the TPS3899DL01-Q1 must be at least 25 ms to allow the microprocessor, and all other devices using the 3.3 V rail, enough time to startup correctly before the 1.8 V rail is enabled via the LDO. Once the LDO is enabled, the reset time delay for the TPS3899PL16-Q1 must be at least 10 ms to allow the 1.8 V rail to settle. For applications with ambient temperatures ranging from –40°C to +125°C, CTS and CTR can be calculated using R_{CTS} and R_{CTR}. Solving for C_{CTS} and C_{CTR} in Equation 4 and Equation 5 for 10 ms and 25 ms gives a minimum capacitor value of 0.016 µF and 0.0403 µF which are rounded up to standard values of 0.022 µF and 0.047 µF, respectively, to account for capacitor tolerance.

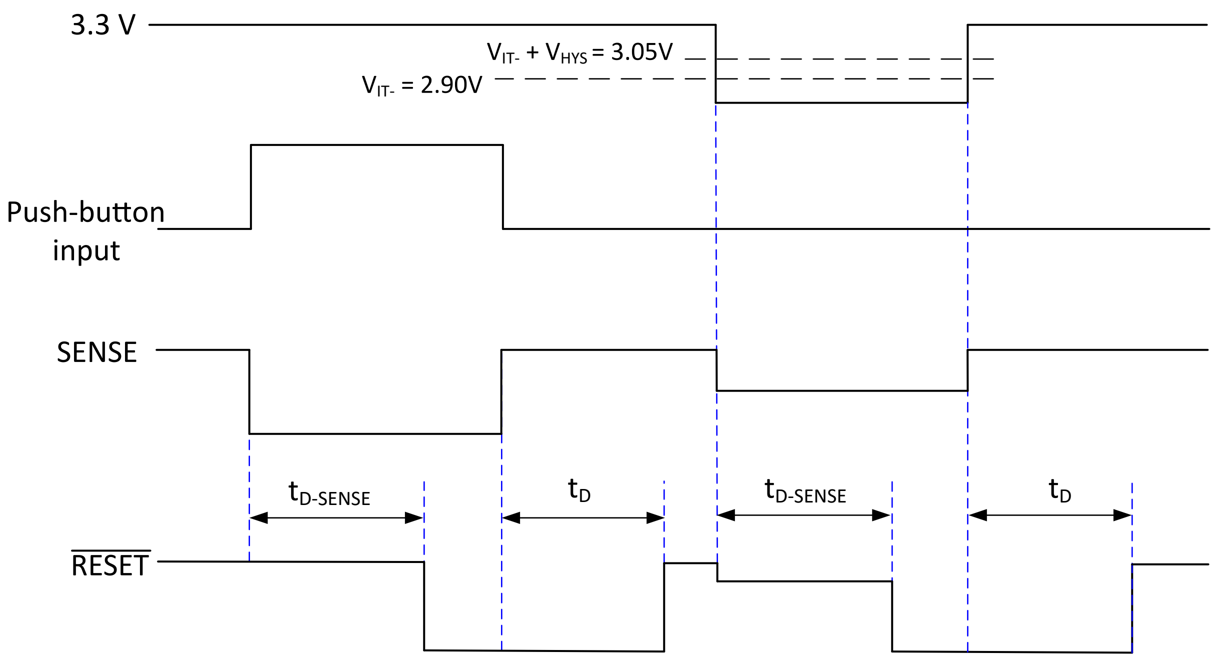


Figure 9-2. TPS3899DL01-Q1 3.3 V Voltage Rail Monitor Timing Diagram

A 1 µF decoupling capacitor is connected to the VDD pin as a good analog design practice. The pull-up resistor is only required for the open-drain device variants and is calculated to ensure that V_{OL} does not exceed max limit given the $I_{\overline{RESET}(Sink)}$ possible at the expected supply voltage. The open-drain variant is used in this design example and the nominal VDD is 3.3 V but dropping to 2.9 V for V_{IT-}, the voltage across the pull-up resistor can be determined. In Section 7.5, max V_{OL} provides 2 mA $I_{\overline{RESET}(Sink)}$ for 3.3 V VDD. Using 2 mA of $I_{\overline{RESET}(Sink)}$ and 300 mV max V_{OL}, gives us 1.3 kΩ for the pull-up resistor. Any value higher than 1.3 kΩ would ensure that V_{OL} will not exceed 300 mV max specification.

9.3 Application Curves

These application curves were taken with the TPS3899EVM which uses the TPS3899DL01DSER. Please see the TPS3899EVM User Guide for more information.

Figure 9-3. Sense Delay where CTS = 0.1 µF

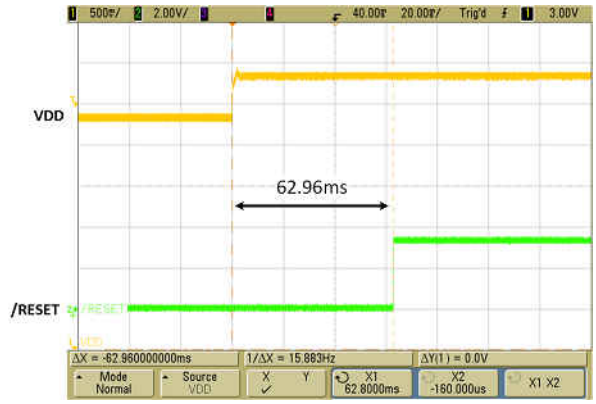


Figure 9-4. Reset Delay where CTR = 0.1µF

10 Power Supply Recommendations

The TPS3899-Q1 is designed to operate from an input supply with a voltage range between 0.85 V and 6 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1 µF capacitor between the VDD pin and the GND pin. Also, placing a 10 nF to 100 nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal. This device has a 6.5 V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 6.5 V, additional precautions must be taken.

11 Layout

11.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1 µF ceramic capacitor near the VDD pin. If a capacitor is not connected to the CTS or CTS pins, then minimize parasitic capacitance on this pin so the sense delay or reset delay times are not adversely affected. To improve noise immunity on the SENSE pin, place a capacitor (C_{SENSE}) as close as possible to the SENSE pin. Placing a 10 nF to 100 nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal.

11.2 Layout Example

The layout example in Figure 11-1 shows how the TPS3899-Q1 is laid out on a printed circuit board (PCB) with a user-defined sense delay and reset delay.

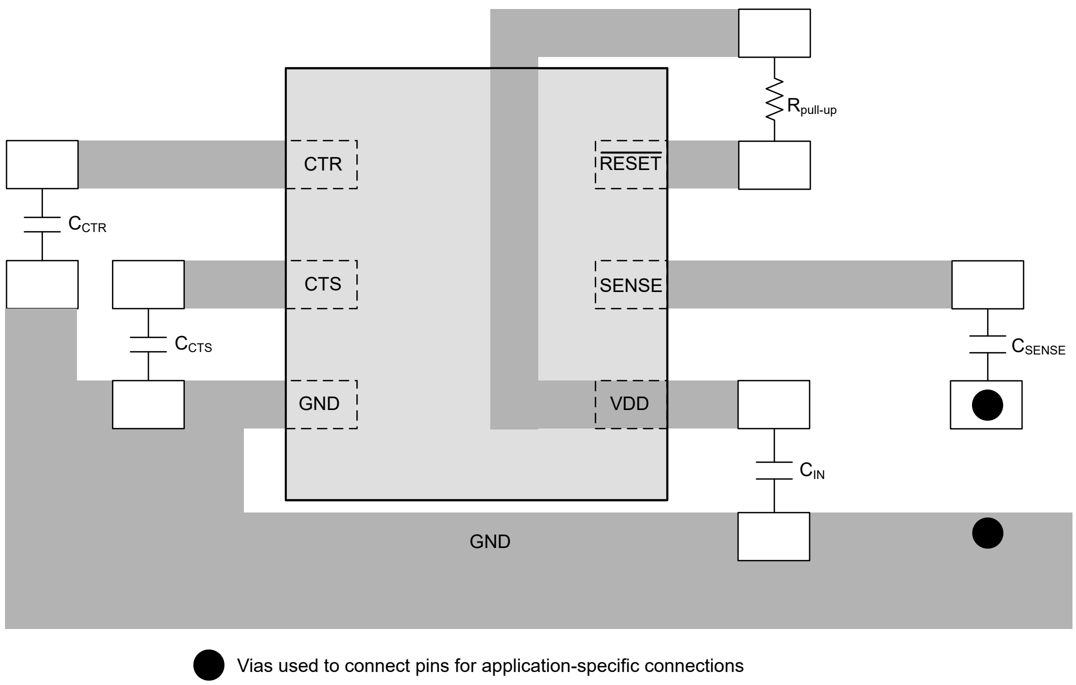


Figure 11-1. Recommended Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

Figure 5-1 in Device Nomenclature and Table 12-1 shows how to decode the function of the device based on its part number shown in Table 12-2.

Table 12-1. Device Naming Convention

DESCRIPTION	NOMENCLATURE	VALUE
Generic Part number	TPS3899-Q1	TPS3899-Q1
Variant code (Output Toplogy)	DL	Open-Drain, Active-Low
	PL	Push-Pull, Active-Low
	PH	Push-Pull, Active-High
Detect Voltage Option	## (two characters)	01: 0.505 V (adjustable)
		Example: 08 stands for 0.8 V threshold 0.8 V to 5.4 V (fixed threshold voltage)
Package	DSE	WSON
Reel	R	Large Reel
Automotive Version	Q1	AEC-Q100

Table 12-2 shows the possible variants of the TPS3899-Q1. Please refer to the Package Option Addendum (POA), in this datasheet, for which variant is orderable and available; minimum order quantities apply.

Table 12-2. Device Naming Convention

ORDERABLE DEVICE NAME			THRESHOLD VOLTAGE (V)
-DL (OPEN-DRAIN ACTIVE-LOW)	-PL (PUSH-PULL ACTIVE-LOW)	-PH (PUSH-PULL ACTIVE-HIGH)	
TPS3899DL01-Q1	TPS3899PL01-Q1	TPS3899PH01-Q1	0.505
TPS3899DL08-Q1	TPS3899PL08-Q1	N/A	0.80
TPS3899DL09-Q1	TPS3899PL09-Q1	N/A	0.90
TPS3899DL10-Q1	TPS3899PL10-Q1	N/A	1.00
TPS3899DL11-Q1	TPS3899PL11-Q1	TPS3899PH11-Q1	1.10
TPS3899DL12-Q1	TPS3899PL12-Q1	TPS3899PH12-Q1	1.20
TPS3899DL13-Q1	TPS3899PL13-Q1	TPS3899PH13-Q1	1.30
TPS3899DL14-Q1	TPS3899PL14-Q1	TPS3899PH14-Q1	1.40
TPS3899DL15-Q1	TPS3899PL15-Q1	TPS3899PH15-Q1	1.50
TPS3899DL16-Q1	TPS3899PL16-Q1	TPS3899PH16-Q1	1.60
TPS3899DL17-Q1	TPS3899PL17-Q1	TPS3899PH17-Q1	1.70
TPS3899DL18-Q1	TPS3899PL18-Q1	TPS3899PH18-Q1	1.80
TPS3899DL19-Q1	TPS3899PL19-Q1	TPS3899PH19-Q1	1.90
TPS3899DL20-Q1	TPS3899PL20-Q1	TPS3899PH20-Q1	2.00
TPS3899DL21-Q1	TPS3899PL21-Q1	TPS3899PH21-Q1	2.10
TPS3899DL22-Q1	TPS3899PL22-Q1	TPS3899PH22-Q1	2.20
TPS3899DL23-Q1	TPS3899PL23-Q1	TPS3899PH23-Q1	2.30
TPS3899DL24-Q1	TPS3899PL24-Q1	TPS3899PH24-Q1	2.40
TPS3899DL25-Q1	TPS3899PL25-Q1	TPS3899PH25-Q1	2.50
TPS3899DL26-Q1	TPS3899PL26-Q1	TPS3899PH26-Q1	2.60

Table 12-2. Device Naming Convention (continued)

ORDERABLE DEVICE NAME			THRESHOLD VOLTAGE (V)
-DL (OPEN-DRAIN ACTIVE-LOW)	-PL (PUSH-PULL ACTIVE-LOW)	-PH (PUSH-PULL ACTIVE-HIGH)	
TPS3899DL27-Q1	TPS3899PL27-Q1	TPS3899PH27-Q1	2.70
TPS3899DL28-Q1	TPS3899PL28-Q1	TPS3899PH28-Q1	2.80
TPS3899DL29-Q1	TPS3899PL29-Q1	TPS3899PH29-Q1	2.90
TPS3899DL30-Q1	TPS3899PL30-Q1	TPS3899PH30-Q1	3.00
TPS3899DL31-Q1	TPS3899PL31-Q1	TPS3899PH31-Q1	3.10
TPS3899DL32-Q1	TPS3899PL32-Q1	TPS3899PH32-Q1	3.20
TPS3899DL33-Q1	TPS3899PL33-Q1	TPS3899PH33-Q1	3.30
TPS3899DL34-Q1	TPS3899PL34-Q1	TPS3899PH34-Q1	3.40
TPS3899DL35-Q1	TPS3899PL35-Q1	TPS3899PH35-Q1	3.50
TPS3899DL36-Q1	TPS3899PL36-Q1	TPS3899PH36-Q1	3.60
TPS3899DL37-Q1	TPS3899PL37-Q1	TPS3899PH37-Q1	3.70
TPS3899DL38-Q1	TPS3899PL38-Q1	TPS3899PH38-Q1	3.80
TPS3899DL39-Q1	TPS3899PL39-Q1	TPS3899PH39-Q1	3.90
TPS3899DL40-Q1	TPS3899PL40-Q1	TPS3899PH40-Q1	4.00
TPS3899DL41-Q1	TPS3899PL41-Q1	TPS3899PH41-Q1	4.10
TPS3899DL42-Q1	TPS3899PL42-Q1	TPS3899PH42-Q1	4.20
TPS3899DL43-Q1	TPS3899PL43-Q1	TPS3899PH43-Q1	4.30
TPS3899DL44-Q1	TPS3899PL44-Q1	TPS3899PH44-Q1	4.40
TPS3899DL45-Q1	TPS3899PL45-Q1	TPS3899PH45-Q1	4.50
TPS3899DL46-Q1	TPS3899PL46-Q1	TPS3899PH46-Q1	4.60
TPS3899DL47-Q1	TPS3899PL47-Q1	TPS3899PH47-Q1	4.70
TPS3899DL48-Q1	TPS3899PL48-Q1	TPS3899PH48-Q1	4.80
TPS3899DL49-Q1	TPS3899PL49-Q1	TPS3899PH49-Q1	4.90
TPS3899DL50-Q1	TPS3899PL50-Q1	TPS3899PH50-Q1	5.00
TPS3899DL51-Q1	TPS3899PL51-Q1	TPS3899PH51-Q1	5.10
TPS3899DL52-Q1	TPS3899PL52-Q1	TPS3899PH52-Q1	5.20
TPS3899DL53-Q1	TPS3899PL53-Q1	TPS3899PH53-Q1	5.30
TPS3899DL54-Q1	TPS3899PL54-Q1	TPS3899PH54-Q1	5.40

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3899DL01DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M4	Samples
TPS3899DL30DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M5	Samples
TPS3899DL31DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M7	Samples
TPS3899PL16DSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3899-Q1 :

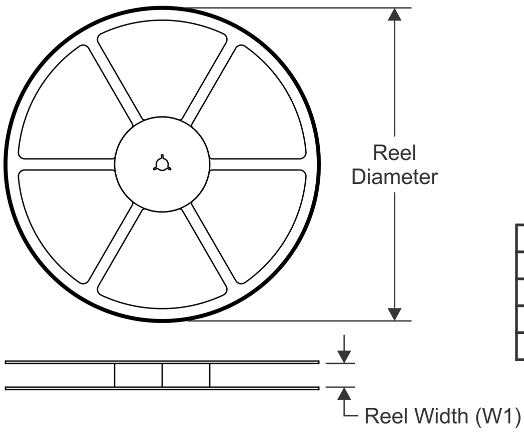
- Catalog : TPS3899

NOTE: Qualified Version Definitions:

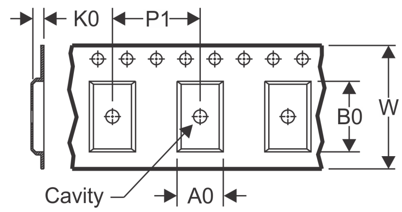
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

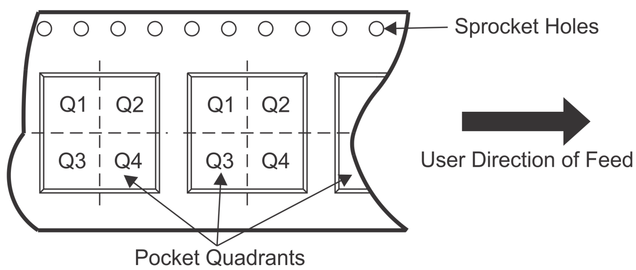


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

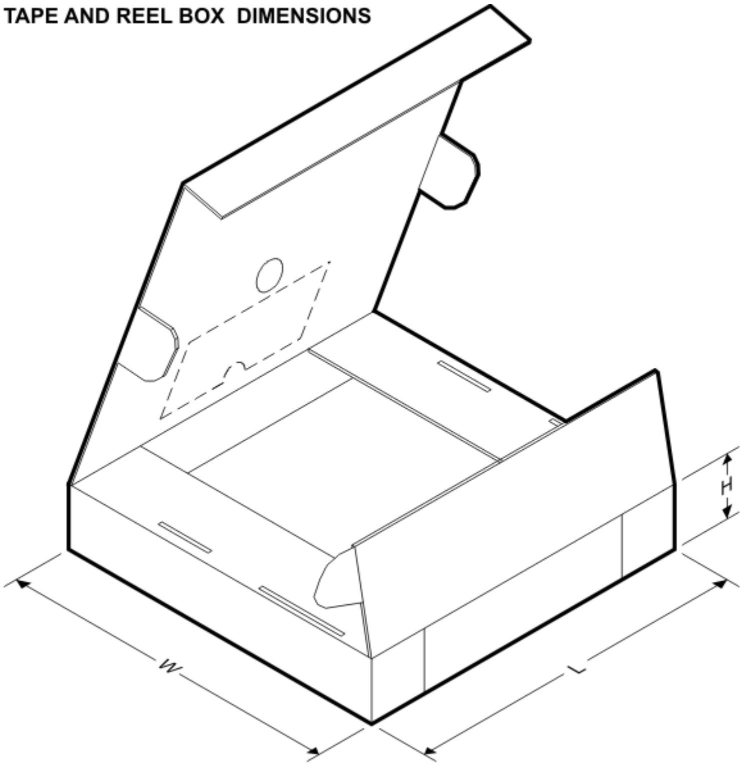
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3899DL01DSERQ1	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL30DSERQ1	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL31DSERQ1	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899PL16DSERQ1	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2

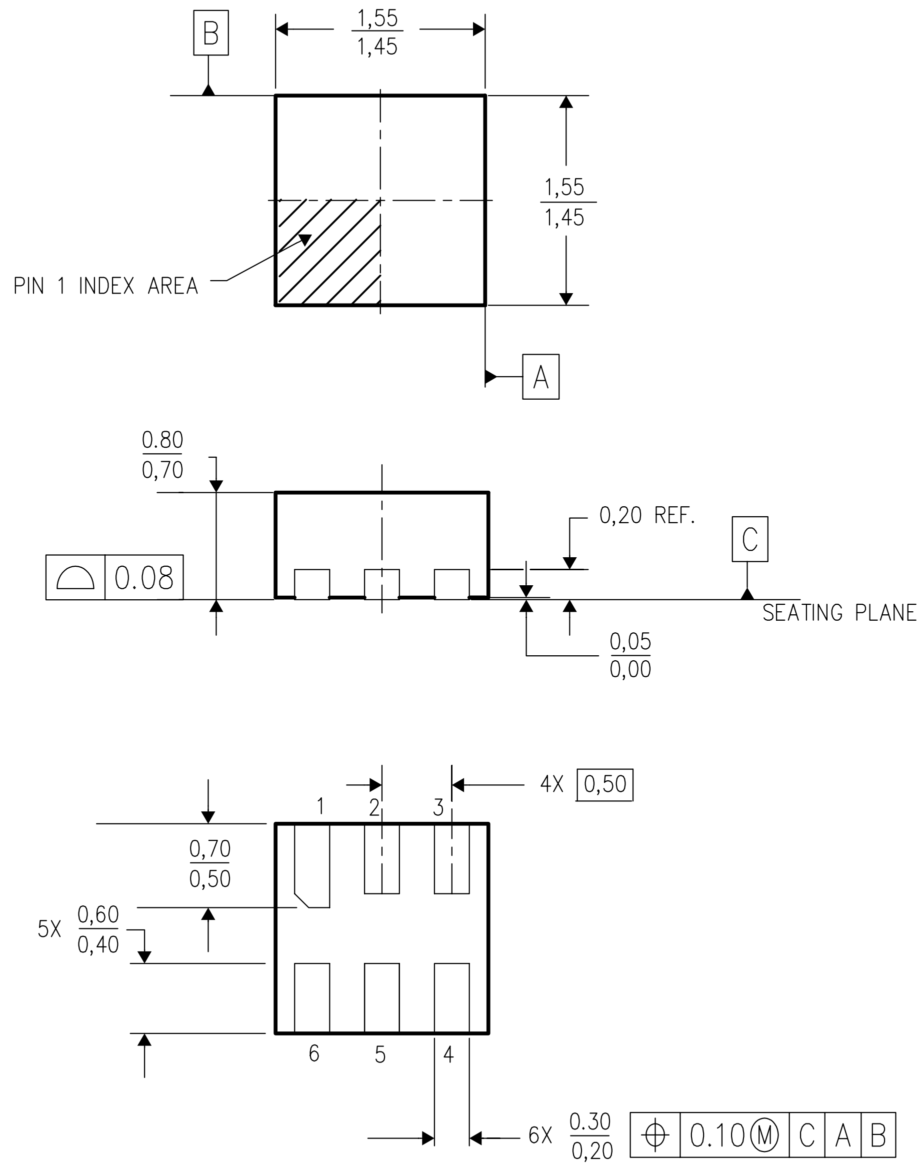
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3899DL01DSERQ1	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL30DSERQ1	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL31DSERQ1	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899PL16DSERQ1	WSON	DSE	6	3000	210.0	185.0	35.0

DSE (S-PDSO-N6) PLASTIC SMALL OUTLINE



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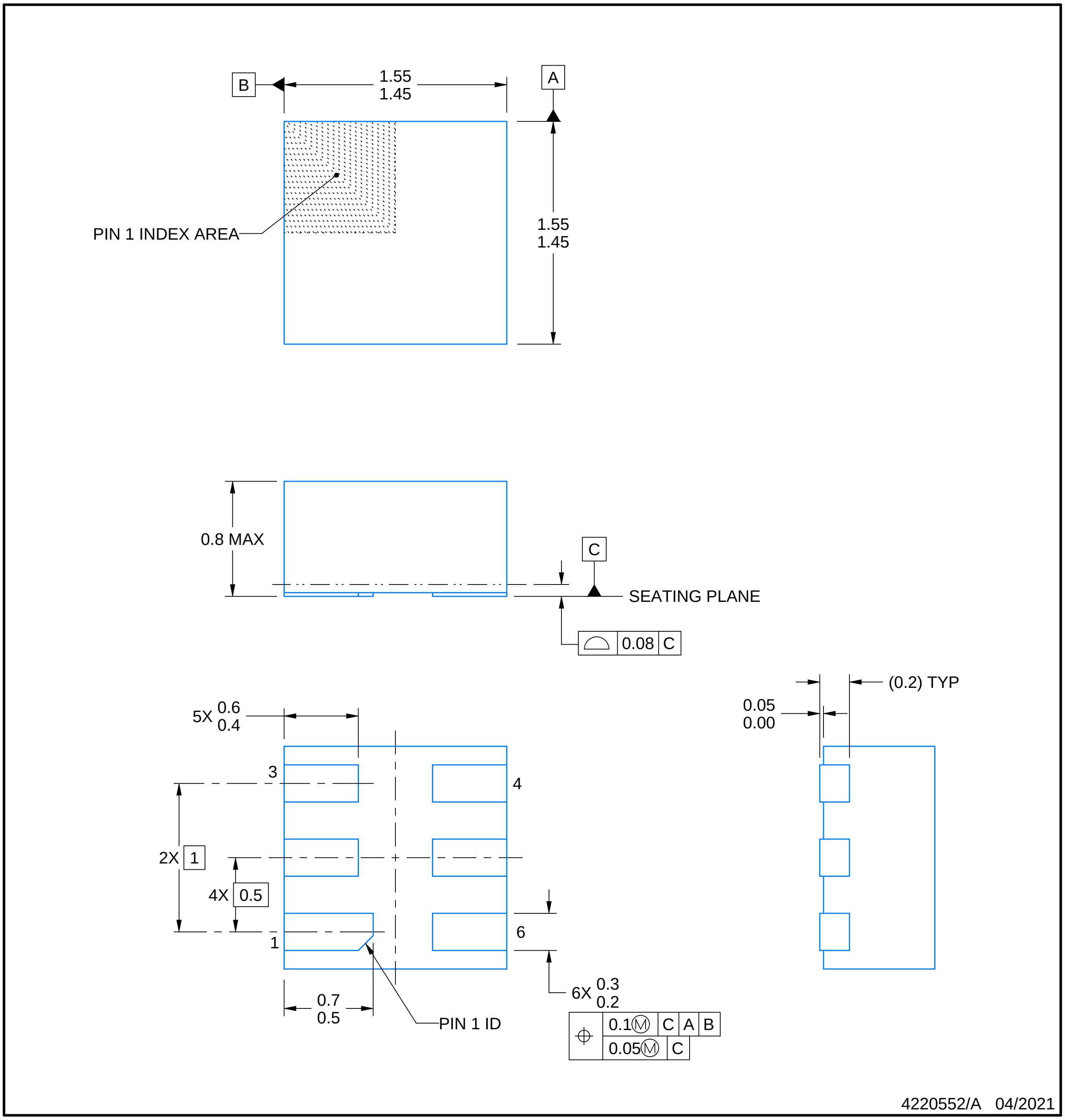
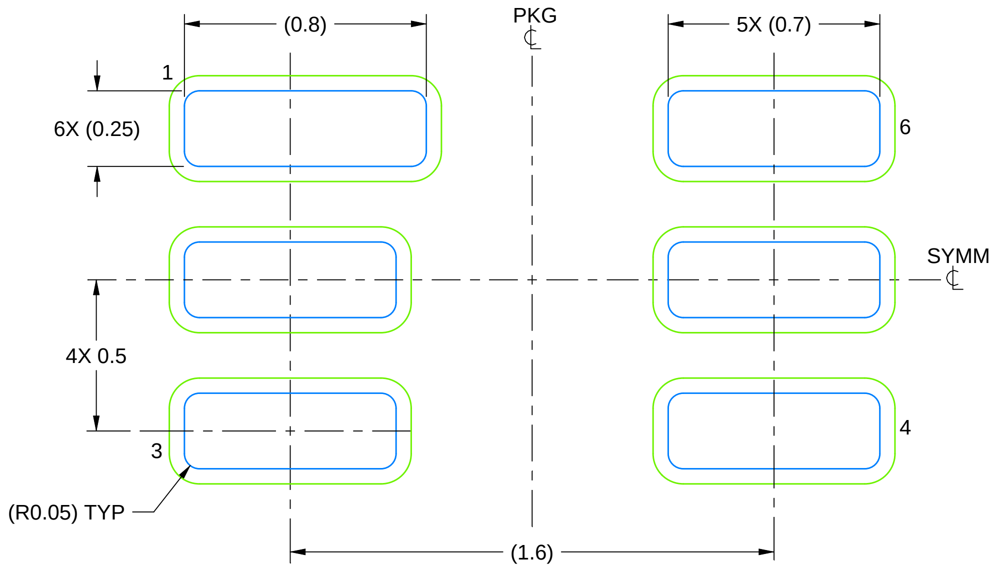
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.
- D. This package is lead-free.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

PADS 4-6
NON SOLDER MASK
DEFINED

PADS 1-3
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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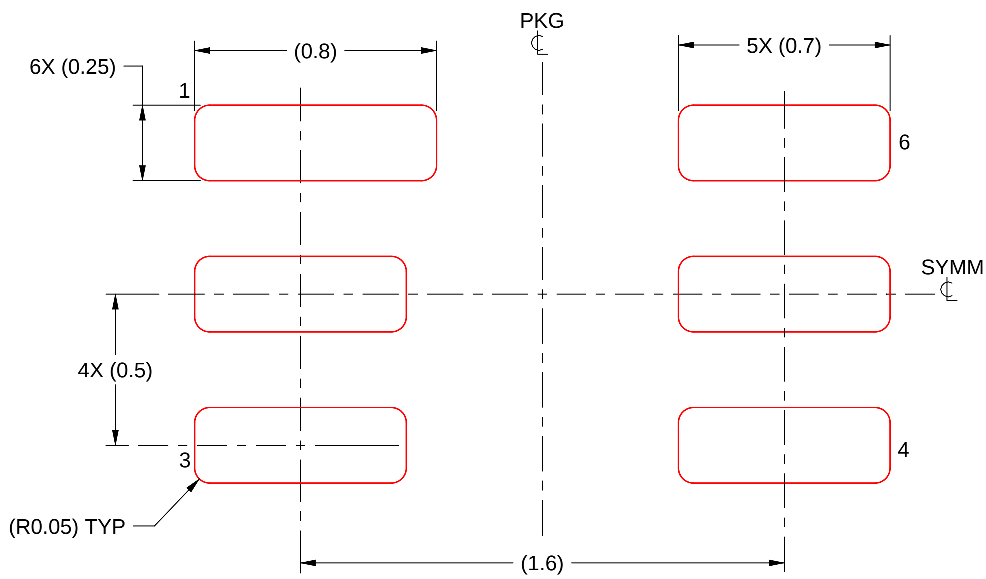
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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