Texas Instruments

TPS40000/1 Controller Enables High-Power Synchronous Step-Down Converter for Low-Logic Voltages, (PR071)

Reference Design

TPS40000/1 Controller Enables High-Power Synchronous Step-Down Converter for Low Voltages Logic, (PR071)

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1 Introduction

The TPS40000 and the TPS40001 are voltage-mode, synchronous buck PWM controllers that utilize TI's proprietary Predictive Gate Drive™ technology to wring maximum efficiency from step-down converters. This controller family provides a bootstrap charging circuit to allow the use of an N-channel MOSFET as the topside buck switch to reduce conduction losses and increase silicon device utilization. Predictive Gate Drive™ technology controls the delay from main switch turn-off to synchronous rectifier turn-on and also the delay from rectifier turn-off to main switch turn-on. This allows minimization of the losses in the MOSFET body diodes, both conduction and reverse recovery. This reference design provides details on a 10-A buck converter that converts 3.3 V down to a 1.2 V level utilizing either the TPS40000 or TPS40001 controller.

The specification for this board is as follows:

- V_{IN} = 3.0 V to 3.6 V
- V_{OUT} = 1.2 V
- I_{OUT} = 10 A
- Efficiency = >90% with load from 1 A to 5 A
- Output voltage ripple < 2% V_{OUT}
- Power semiconductor devices: each MOSFET is a single SO-8 package

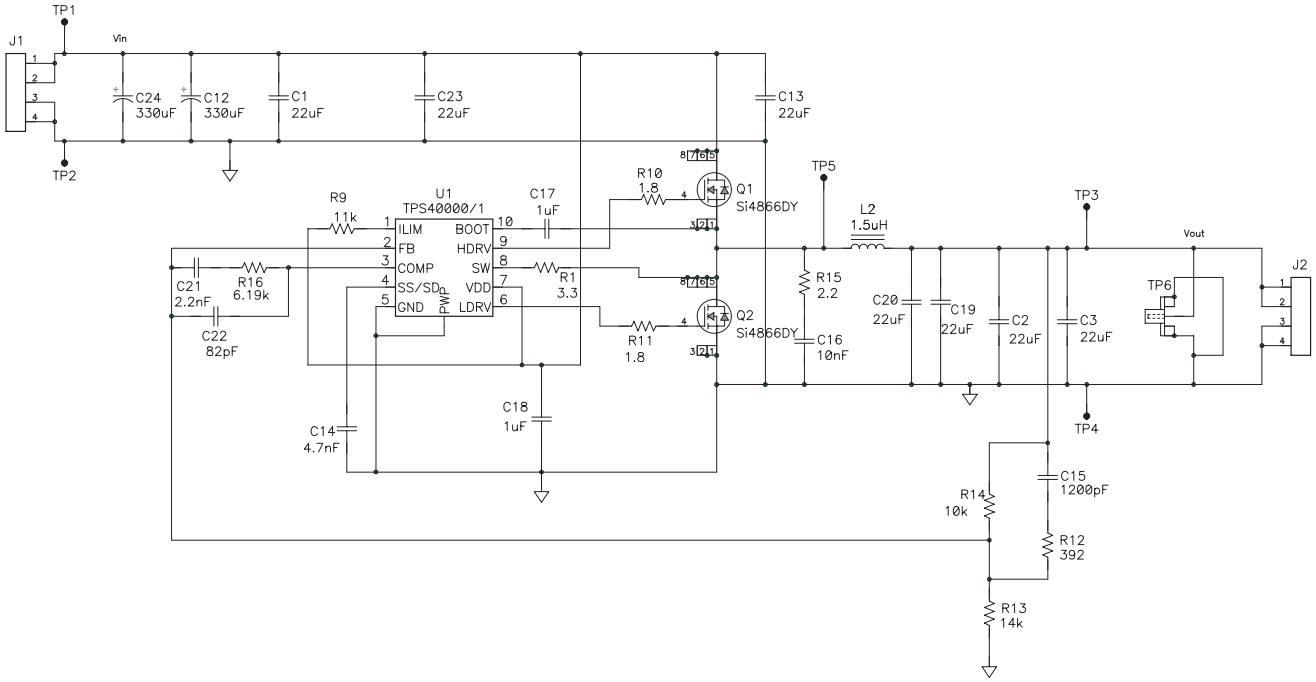

Figure 1. Application Diagram

2 Design Procedure

2.1 TPS4000X Family Device

The TPS4000X family of devices offers four selections to encompass the frequency and output current mode choices. The TPS4000/1 are selected for this high current application because the 300-kHz switching frequency will improve efficiency in this design. The TPS40002/3 are available for applications needing 600-kHz operation. The TPS4000X family also allows the user to select discontinuous current mode (DCM) operation or continuous current mode (CCM) operation at lighter loads. In this reference design the TPS40001 is selected to maintain continuous mode operation down to zero load. If desired, the TPS40000 can be installed to turn the synchronous MOSFET OFF when the controller senses the inductor current reaching zero, indicating the circuit is entering DCM operation.

2.2 Inductance Value

The output inductor value is selected to set the ripple current to a value most suited to overall circuit functionality. An inductor selection that is too small leads to larger ripple current that increases RMS current losses in the inductor and MOSFETs also leads to more ripple voltage on the output. The inductor value is calculated by equation (1).

$$L_{MIN} = \frac{V_{OUT}}{F \times I_{RIPPLE}}\left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right) \quad (1)$$

in which I_{RIPPLE} is chosen to be 20% of I_{OUT}, or 2.0 A. This calculates to a value of 1.5 µH. A device with minimal resistance helps to reduce losses at the high current levels in this converter.

2.3 Input Capacitor Selection

Bulk input capacitor selection is based on allowable input voltage ripple and required RMS current carrying capability. In typical buck converter applications, the converter is fed from an upstream power converter with its own output capacitance. In this standalone converter, one or more capacitors are required to supply the current required during the top MOSFET ON-time while keeping ripple within acceptable limits. For this power level, input voltage ripple of 150 mV is reasonable, and the minimum capacitance is calculated as:

$$C = \frac{I \times \Delta t}{\Delta V} = \frac{10\ A \times 1.21\mu s}{0.15\ V} = 80\ \mu F \quad (2)$$

In addition to this minimum capacitance requirement, the RMS current stresses must be considered. In this converter, the large duty cycle causes the input RMS current to be nearly as large as the output current, as shown in equation (3), which is a simplified formula for the RMS current for a trapezoidal current waveform.

$$I_{RMS} = I \times \sqrt{D} \quad (3)$$

Additional terms for the ripple component of the current add only a few percent to the total RMS current, so that can be neglected. With V_{IN} = 3.3 V and I_{OUT} = 10 A the input RMS current is 6.3 A. To meet this initial requirement with small size and cost, a combination of capacitors is considered. To carry the high frequency ripple current, three 22-µF, X5R ceramic capacitors are placed close to the power circuitry. Although these capacitors have an extremely small resistance the datasheet indicates that the part undergoes a 30°C temperature rise with 2 A_{RMS} current at 500 kHz, and therefore more current capability is needed. Two 330-µF POSCAPs with an RMS current capability of 4.4 A each is selected. For many embedded designs with capacitance present in the upstream converter these POSCAPs are not required.

2.4 Output Capacitor Selection

Selection of the output capacitor is based on many application variables, including function, cost, size, and availability. The minimum allowable output capacitance is determined by the amount of inductor ripple current and the allowable output ripple, as given in equation (4)

$$C_{OUT(min)} = \frac{I_{RIPPLE}}{8 \times f \times V_{RIPPLE}} \quad (4)$$

This gives $C_{OUT(min)}$ to be 69 μF for V_{RIPPLE} = 0.012 V. However, this only affects the capacitive component of the ripple voltage. In addition, the voltage component due to the capacitor ESR must be considered, as in equation (5).

$$C_{ESR} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}} \quad (5)$$

When using multiple large X5R ceramic capacitors the ESR contribution to ripple is often negligible. Four 22-μF, 6.3-V, X5R capacitors are used in parallel.

2.5 MOSFET Selection

One constraint this design is the use of one SO-8 MOSFET in the upper switch device and one SO-8 in the lower synchronous rectifier location in the buck converter power stage. In this design, the Si4866DY serves well in both the top and bottom switch locations. This device provides a good compromise between moderately low gate charge for fast switching and a low $R_{DS(on)}$ of around 8 mΩ.

2.6 Short Circuit Protection

The TPS40003 implements short circuit protection by comparing the voltage across the topside MOSFET while it is ON to a voltage dropped from VDD by R_{LIM} due to an internal current source of 15 μA inside pin 1. Due to tolerances in the current source and variations in the power MOSFET ON-voltage versus temperature, the short circuit level can protect against gross overcurrent conditions only, and should be set considerably higher than rated load. In this particular case, R_{LIM} is selected as

$$R_{LIM} = R1 = \frac{2 \times \left(I_{OUT}\right) \times R_{DS(on)}}{15\ \mu A} \quad (6)$$

For this design, R_{LIM} = 11 kΩ, and the factor of 2 in the equation accounts for the variations in component tolerances and output current ripple. The high currents that are switched under short circuit conditions may cause SW pin 8 to be driven below ground several volts, possibly injecting substrate current which can cause improper operation of the device. A 3.3-Ω resistor has been placed in series with this pin to limit its excursion to safe levels.

2.7 Compensation Design

The TPS40000 uses voltage mode control in conjunction with a high frequency error amplifier. The power circuit L-C double pole corner frequency f_C is located at 13.8 kHz. The output capacitor ESR zero is above 1.5 MHz and is thus not a real factor in loop compensation. The feedback compensation network is implemented to provide two zeroes and three poles. The first pole is placed at the origin to improve dc regulation.

The first zero is placed a little below f_C, at 11.7 kHz,

$$f_{z1} = \frac{1}{2 \times \pi \times R_{16} \times C_{21}} \quad (7)$$

The second zero is placed near fc at 12.8kHz,

$$f_{z2} = \frac{1}{2 \times \pi \times \left(R_{12} + R_{14}\right) \times C_{15}} \quad (8)$$

Since the ESR zero is at a very high frequency, it has a minimal impact on the selection of compensation components. This allows placement of the two poles around 325 kHz to allow maximum utilization of the high frequency error amplifier on board the TPS40001.

$$f_{p1} = \frac{1}{2 \times \pi \times R_{16} \times \left[\frac{C_{21} \times C_{22}}{\left(C_{21} + C_{22}\right)}\right]} \quad (9)$$

and the second pole is placed at one-half the switching frequency,

$$f_{p2} = \frac{1}{2 \times \pi \times R_{12} \times C_{15}} \quad (10)$$

The plot of gain and phase in Figure 2 shows a crossover frequency of 42 kHz and a phase margin of approximately 50 degrees.

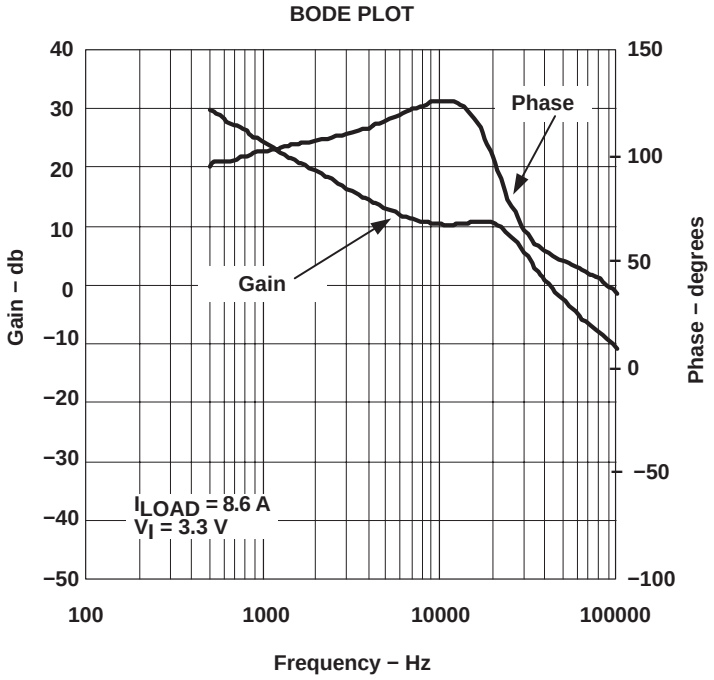

Figure 2.

2.8 Snubber Component Selection

The switch node where Q1 and L1 come together is very noisy. An R-C network fitted between this node and ground can help reduce ringing and voltage overshoot on Q2. This ringing noise should be minimized to prevent it from confusing the control circuitry which is monitoring this node for current limit, Predictive Gate Drive™, and DCM control functions.

As a starting point, the snubber capacitor, C16, is generally chosen to be 5−8 times larger than the parasitic capacitance at the node, which is primarily C_{OS} of Q2. Since C_{OS} is around 2800 pF for Q2 at 5 V, C8 is chosen to be 10 nF. R2 is empirically determined to be 2.2 Ω, which minimizes the ringing and overshoot at the switch node. With the relatively low input voltage of 5 V, the power loss, ½ CV^2f , is relatively small at 37 mW.

3 PowerPAD Packaging

The TPS4000X family is available in the DGQ version of TI's PowerPAD™ thermally enhanced package. In the PowerPAD™, the integrated circuit die is attached to the leadframe die pad using a thermally conductive epoxy. The leadframe die pad is exposed on the bottom side of the package, and can be soldered to the PCB using standard solder flow techniques. This construction technique provides extremely low thermal resistance from the junction to the PCB ambient temperature.

The PowerPAD™ package helps to keep the junction temperature rise relatively low even with the power dissipation inherent in the onboard MOSFET drivers. This power loss is proportional to switching frequency, drive voltage, and the gate charge needed to enhance the N-channel MOSFETs. Effective heat removal allows the use of ultra small packaging while maintaining high component reliability.

To effectively remove heat from the PowerPAD™ package, a thermal land should be provided directly underneath the package. This thermal land usually has vias that help to spread heat to internal copper layers and/or the opposite side of the PCB. The vias should not have thermal reliefs that are often used on ground planes, because this reduces the copper area to transfer heat. Additionally, the vias should be small enough so that the holes are effectively plugged when plated. This prevents the solder from wicking away from the connection between the PCB surface and the bottom of the part. A typical construction utilizes two-five vias of 0.013" diameter plated with 1 ounce copper in the land under the TPS40003. A typical footprint pattern is shown in Figure 3, but it does not show the copper land which would encompass the vias above and below the device.

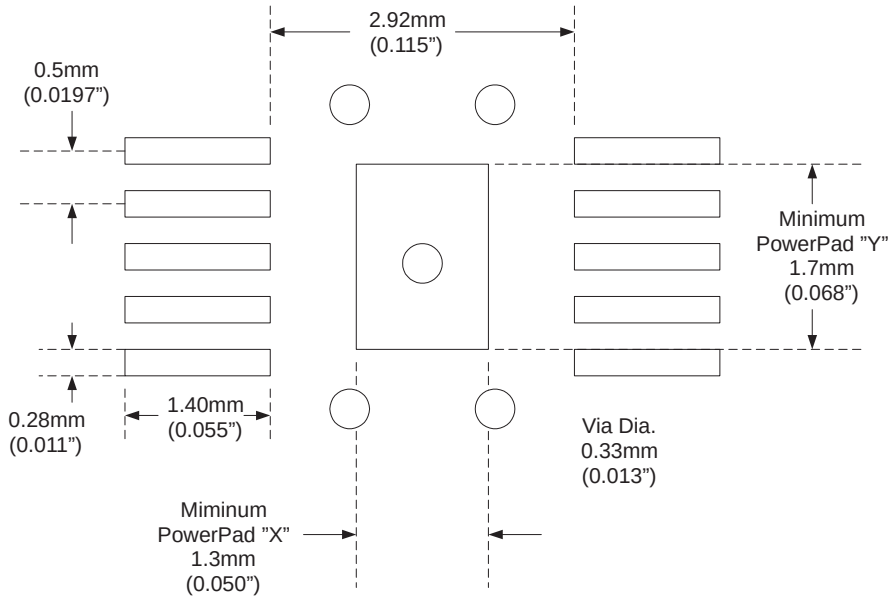

Figure 3. PCB Footprint

The Texas Instrument document, *PowerPAD™ Thermally Enhanced Package Application Report* (TI Literature Number SLMA002) should be consulted for more information on the PowerPAD™ package. This report offers in-depth information on the package, assembly and rework techniques, and illustrative examples of the thermal performance of the PowerPAD™ package.

4 Test Results/Performance Data

Typical efficiency curves are shown in Figure 4 for two input voltages.

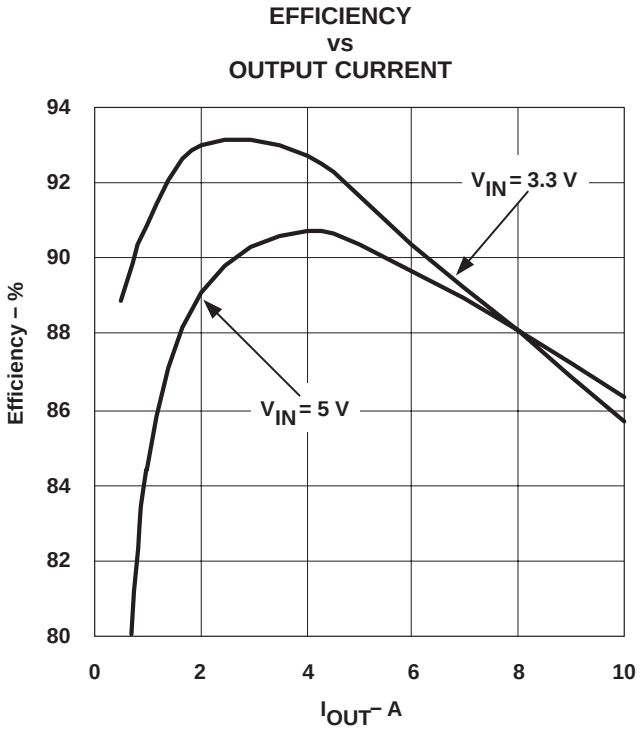

Figure 4.

Figure 5 shows the switch node of the converter at full load. This highlights the minimal diode conduction intervals possible with predictive gate drive technology.

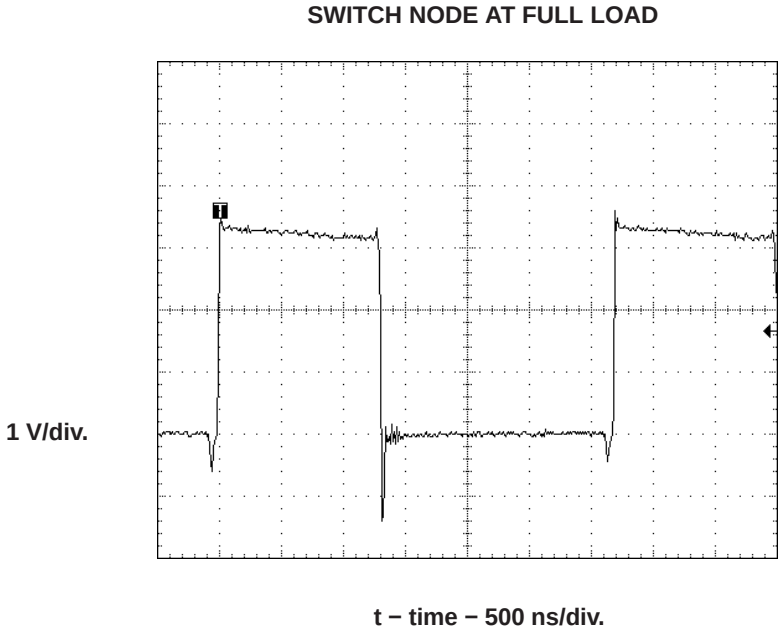

Figure 5.

Figure 6 shows the stable transient response for a load step between 5 Amps and 10 Amps.

OUTPUT TRANSIENT RESPONSE

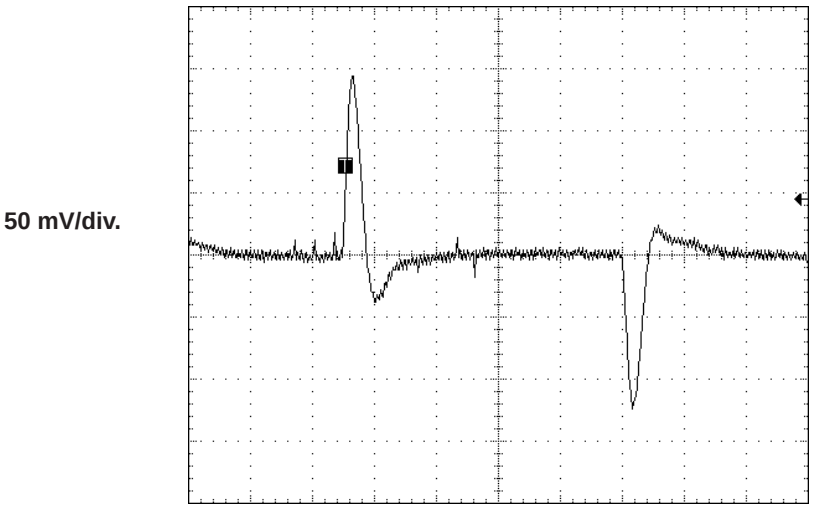

Figure 6.

Figure 7 shows the short circuit operation of the converter. Note that the burst of pulses occurs every 7.5 ms, so the input power during a hard fault is extremely low.

SHORT CIRCUIT RESTART CYCLES, TP5

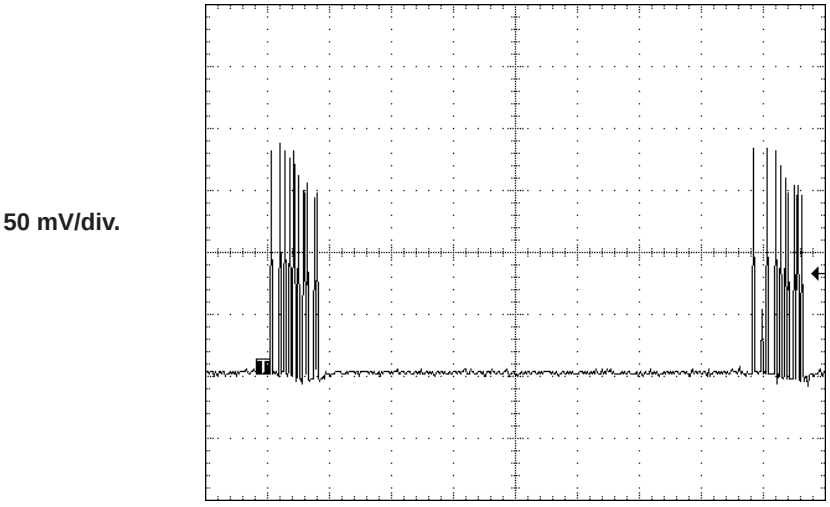

Figure 7.

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