ENHANCED, LOW-INPUT VOLTAGE-MODE SYNCHRONOUS BUCK CONTROLLER

Check for Samples: TPS40021-EP

FEATURES

- **Operating Input Voltage 2.25 V to 5.5 V**
- **Output Voltage as Low as 0.7 V**
- **1% Internal 0.7-V Reference**
- **Predictive Gate Drive™ N-Channel MOSFET Drivers for Higher Efficiency**
- **Externally Adjustable Soft-Start and Short Circuit Current Limit**
- **Programmable Fixed-Frequency 100-kHz to 1-MHz Voltage-Mode Control**
- **Source or Sink Current**
- **Quick Response Output Transient Comparators With Power Good Indication Provide Output Status**
- **16-Pin PowerPAD™ Package**

APPLICATIONS

- **Networking Equipment**
- **Telecom Equipment**
- **Base Stations**
- **Servers**
- **DSP Power**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C to 125°C) Temperature Range** (1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Custom temperature ranges available

DESCRIPTION

The TPS40021 is a dc-to-dc controller designed for non-isolated synchronous buck regulators, providing enhanced operation and design flexability through user programmability.

The device utilizes a proprietary Predictive Gate Drive technology to minimize the diode conduction losses associated with the high-side and synchronous rectifier N-channel MOSFET transistions. The integrated charge pump with boost circuit provides a regulated 5-V gate drive for both the high side and synchronous rectifier N-channel MOSFETs. The use of the Predictive Gate Drive technology and charge pump/boost circuits combine to provide a highly efficient, smaller and less expensive converter.

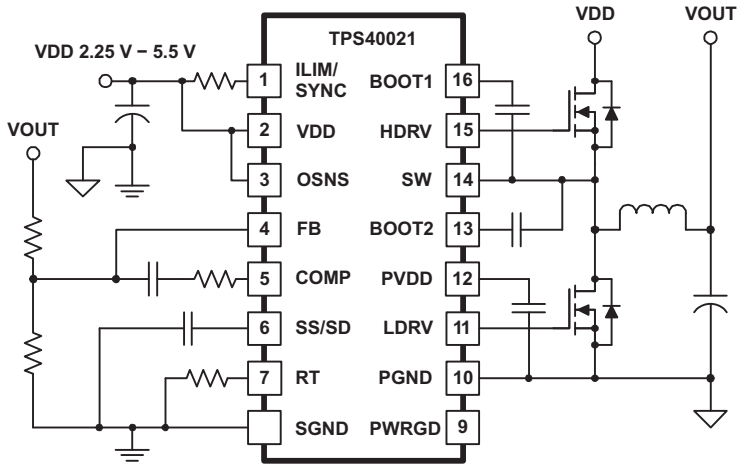
Design flexibility is provided through user programmability of such functions as: operating frequency, short circuit current detection thresholds, soft-start ramp time, and external synchronization frequency. The operating frequency is programmable using a single resistor over a frequency range of 100 kHz to 1 MHz. Higher operating frequencies yield smaller component values for a given converter power level as well as faster loop closure.

The short circuit current detection is programmable through a single resistor, allowing the short circuit current limit detection threshold to be easily tailored to accommodate different size ($R_{DS(on)}$) MOSFETs. The short circuit current function provides pulse-by-pulse current limiting during soft-start and short term transient conditions as well as a fault counter to handle longer duration short circuit current conditions. If a fault is detected the controller shuts down for a period of time determined by six consecutive soft-start cycles. The controller automatically retries the output every seventh soft-start cycle.

In addition to determining the off time during a fault condition, the soft-start ramp provides a closed loop controlled ramp of the converter output during startup. Programmability allows the ramp rate to be adjusted for a wide variety of output L-C component values.

The output voltage transient comparators provide a quick response , first strike, approach to output voltage transients. The output voltage is sensed through a resistor divider at the OSNS pin. If an overvoltage condition is detected the HDRV gate drive is shut-off and the LDRV gate drive is turned on until the output is returned to regulation. Similarly, if an output undervoltage condition is sensed the HDRV gate drive goes to 95% duty cycle to pump the output back up quickly. In either case, the PowerGood open drain output pulls low to indicate an output voltage out of regulation condition. The PowerGood output can be daisy-chained to the SS/SD pin or enable pin of other controllers or converters for output voltage sequencing. The transient comparators can be disabled by simply tying the OSNS pin to VDD.

The TPS40021 can be externally synchronized through the ILIM/SYNC pin up to 1.5× the free-running frequency. This allows multiple contollers to be synchronized to eliminate EMI concerns due to input beat frequencies between controllers.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_J	PACKAGE	ORDERABLE PART NUMBER		TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	Plastic HTSSOP PowerPAD (PWP)(2)	TPS40021MPWPREP	Tape and Reel, 2000	40021M	V62/12601-01XE
		TPS40021MPWPEP	Tube, 90		V62/12601-01XE-T

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) With Cu NIPDAU lead/ball finish

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range unless otherwise noted

			MIN	MAX	UNIT
V_{IN}	Input voltage range	SS/SD, VDD, PVDD, OSNS	–0.3	6	V
		BOOT2, BOOT1	V_{SW} + 6		
		SW	–0.3	10.5	
		SWT (SW transient < 50 ns)	–5		
		FB, ILIM	–0.3	6	
V_{OUT}	Output voltage range	COMP, PWRGD, RT	–0.3	6	V
I_S	Sink current	PWRGD	10		mA
T_J	Maxium juction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260		°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS40021-EP PWP 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	38.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	28	
θ_{JB}	Junction-to-board thermal resistance(4)	9	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.4	
ψ_{JB}	Junction-to-board characterization parameter(6)	8.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	2.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Supply voltage, V_{IN}	2.25	5.50	V
Operating temperature range, T_J	–55	125	°C

ELECTRICAL CHARACTERISTICS

T_J = −55°C to 125°C, T_J = T_A, VDD = 5.0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{DD}	Input voltage range		2.25		5.50	V
V_{PVDD}	PVDD pin voltage	V_{DD} = 3.3 V		4.9	5.2	V
I_{DD}	Switching current	500 kHz, No load on HDRV, LDRV		3.5	5	mA
	Quiescent current	FB = 0.8 V		2	3	
	Shutdown current	SS/SD = 0 V, Outputs OFF		0.38	1	
V_{UVLO}	Minimum on-voltage		1.95	2.05	2.15	mV
	Hysteresis		72	130	200	
OSCILLATOR						
f_{OSC}	Accuracy	2.25 V ≤ V_{DD} ≤ 5.00 V, R_T = 69.8 kΩ	405	500	575	kHz
		2.25 V ≤ V_{DD} ≤ 5.00 V, R_T = 34.8 kΩ	740	950	1100	
V_{RAMP}	Ramp voltage	V_{PEAK} − V_{VAL}	0.80	0.93	1.07	V
V_{VAL}	Ramp valley voltage		0.24	0.31	0.41	V
PWM						
d_{MAX}	Maximum duty cycle	V_{OSNS} = V_{DD}, R_T = 34.8 kΩ, V_{DD} = 3.3 V, F_B = 0 V	85	94		%
		V_{OSNS} = V_{DD}, R_T = 70 kΩ, V_{DD} = 5 V, F_B = 0 V	90	95		
d_{MIN}	Minimum duty cycle				0	%
t_{MIN}	Minimum HDRV on-time(1)			250		ns
ERROR AMPLIFIER						
V_{FB}	Feedback input voltage	2.25 V ≤ V_{DD} ≤ 5 V	0.683	0.690	0.701	V
I_{BIAS}	Input bias current			30	130	nA
V_{OH}	High-level output voltage	I_{OH} = 0.5 mA, V_{FB} = GND	2	2.5		V
V_{OL}	Low-level output voltage	I_{OL} = 0.5 mA, V_{FB} = V_{DD}		0.08	0.15	V
I_{OH}	High-level output source current	V_{FB} = GND	2.7	7		mA
I_{OL}	Low-level output sink current	V_{FB} = V_{DD}	3	8		mA
G_{BW}	Gain bandwidth(2)			10		MHz
A_{OL}	Open loop gain		53	85		dB
CURRENT LIMIT						
I_{SINK}	Current limit sink current	2.25 V ≤ V_{DD} ≤ 5.00 V, R_T = 69.8 kΩ	165	190	215	µA
V_{OS}	Current limit offset voltage		-20	0	20	mV
t_{ON}	Minimum HDRV on−time in overcurrent	V_{DD} = 3.3 V		200	300	ns
	Switch leading-edge blanking pulse time(2)			140		
t_{SS}	Soft-start cycles			6		cycles
V_{ILIM}	Current limit input voltage range		2		V_{DD}	V
SOFT START						
I_{SS}	Soft-start source current	Outputs = OFF	2	3.3	5.4	µA

(1) Operation below the minimum on-time could result in overlap of the HDRV and LDRV outputs.
(2) Specified by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

T_J = −55°C to 125°C, T_J = T_A, VDD = 5.0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SHUTDOWN						
V_{SD}	Shutdown threshold voltage		0.2	0.26	0.29	V
V_{EN}	Device enable threshold voltage		0.25	0.28	0.32	V
OUTPUT DRIVER						
R_{HDHI}	High-side driver pull-up resistance	$V_{(BOOT1)} - V_{(SW)}$ = 3.3 V, I_{SOURCE} = 100 mA	1	2.5	5	Ω
R_{HDLO}	High-side driver pull-down resistance	$V_{(BOOT1)} - V_{(SW)}$ = 3.3 V, I_{SINK} = 100 mA	0.7	1.5	3	Ω
R_{LDHI}	Low-side driver pull-up resistance	P_{VDD} = 3.3 V, I_{SOURCE} = 100 mA	1	2.5	5	Ω
R_{LDLO}	Low-side driver pull-down resistance	P_{VDD} = 3.3 V, I_{SINK} = 100 mA	0.41	0.80	1.50	Ω
t_{LRISE}	Low-side driver rise time	C_{LOAD} = 1 nF		15	35	ns
t_{LFALL}	Low-side driver fall time			10	25	ns
t_{HRISE}	High-side driver rise time			15	35	ns
t_{HFALL}	High-side driver fall time			10	25	ns
THERMAL SHUTDOWN						
T_{SD}	Shutdown temperature(3)			165		°C
	Hysteresis(3)			15		
CHARGE PUMP						
R_{VB2}	$R_{DS(on)}$ VDD to BOOT2	V_{DD} = 5 V, I_{SOURCE} = 10 mA	2.8	6.6	10.4	Ω
R_{B2P}	$R_{DS(on)}$ BOOT2 to PVDD	V_{DD} = 5 V, I_{SOURCE} = 10 mA	2.8	5.6	8.4	Ω
R_{PB1}	$R_{DS(on)}$ PVDD to BOOT1	V_{DD} = 5 V, I_{SOURCE} = 10 mA	2.9	5.9	8.9	Ω
POWER GOOD						
V_{PGD}	Pull-down voltage	V_{OSNS} = 0.8 V, I_{PWRGD} = 0.5 mA, V_{DD} = 3.3 V	50	90	140	mV
t_{ONHPL}	Output sense high to power good low delay time	0.7 V ≤ V_{OSNS} ≤ 0.8 V, I_{PWRGD} = 0.5 mA, V_{DD} = 3.3 V	6	10	14	µs
t_{ONLPL}	Output sense low to power good low delay time	0.6 V ≤ V_{OSNS} ≤ 0.7 V, I_{PWRGD} = 0.5 mA, V_{DD} = 3.3 V	6	10	14	µs
t_{SDHPH}	Shutdown high to power good high delay time	V_{OSNS} = 0.7 V, I_{PWRGD} = 0.5 mA, V_{DD} = 3.3 V, 0 V ≤ $V_{SS/SD}$ ≤ 0.4 V	2	4	6	µs
t_{SDLPL}	Shutdown low to power good low delay time	V_{OSNS} = 0.7 V, I_{PWRGD} = 0.5 mA, V_{DD} = 3.3 V, 0 V ≤ $V_{SS/SD}$ ≤ 0.4 V	0.5	1.5	3	µs
t_{ONHPH}	Output sense high to nominal to power good high delay time	0.7 V ≤ V_{OSNS} ≤ 0.8 V, I_{PWRGD} = 0.5 mA, V_{DD} = 3.3 V	140	500	1000	ns
t_{ONLPH}	Output sense low to nominal to power good high delay time	0.6 V ≤ V_{OSNS} ≤ 0.7 V, I_{PWRGD} = 0.5 mA, V_{DD} = 3.3 V	140	500	1000	ns
TRANSIENT COMPARATORS						
V_{OV}	Overvoltage output threshold voltage	Referenced to V_{FB}	23	29	35	mV
	Hysteresis		8	15	22	
V_{UV}	Undervoltage output threshold voltage	Referenced to V_{FB}	-37	-31	-25	mV
	Hysteresis		8	15	22	
V_{DIS}	OSNS minimum disable voltage	Referenced to VDD	0.5			V

(3) Specified by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

T_J = −55°C to 125°C, T_J = T_A, VDD = 5.0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYNCHRONIZATION						
V_{ENSY}	Synchronization enable low threshold voltage				0.7	V
V_{BLNK}	Synchronization current limit enable threshold voltage	Referenced to VDD	-0.7			V
t_{MIN}	Minimum synchronization input pulse width			35	50	ns
PREDICTIVE DELAY						
V_{SWP}	Sense voltage to modulate delay			-200		mV
t_{LDHD}	Maximum delay modulation	LDRV OFF-to-HDRV ON	40	65	90	ns
	Counter delay/bit time	LDRV OFF-to-HDRV ON	2.5	4.5	6.2	
t_{HDLD}	Maximum delay modulation	HDRV OFF-to-LDRV ON		80		ns
	Counter delay/bit time	HDRV OFF-to-LDRV ON		5		
RECTIFIER ZERO CURRENT COMPARATOR						
t_{ZBLNK}	Zero current blanking time(4)			150		ns

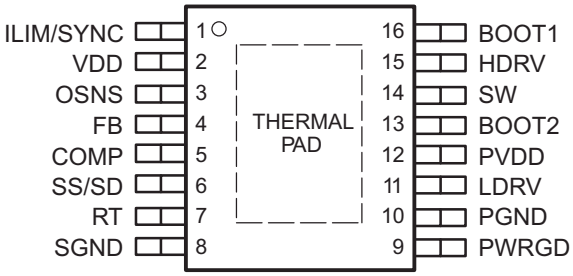
(4) Specified by design. Not production tested.

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO. PWP		
BOOT1	16	I	This pin provides a bootstrapped supply for the high side FET driver, enabling the gate of the high side FET to be driven above the input supply rail. Connect a capacitor from this pin to the SW pin.
BOOT2	13	I	This pin provides a secondary bootstrapping necessary for generation of PVDD. Connect a capacitor from this pin to SW.
COMP	5	O	Output of the error amplifier. Refer to Electrical Characteristics table for loading constraints.
FB	4	I	Inverting input of the error amplifier. In normal operation, V_{FB} is equal to the internal reference level of 690 mV.
HDRV	15	O	The gate drive output for the high side N-channel MOSFET switch is bootstrapped to near PVDD for good enhancement of the high-side switch. The HDRV switches from BOOT1 to SW.
ILIM/SYNC	1	I	The current limit pin is used to set the current limit threshold. A current sink from this pin to GND sets the threshold voltage for output short circuit current across a resistor connected to VDD. Synchronization is accomplished by pulling IMAX to less than 1 V for a period greater than the minimum pulse width and then releasing. An open collector or drain device should be used. These pulses must be of higher frequency than the free running frequency of the local oscillator.
LDRV	11	O	Gate drive output for the low-side synchronous rectifier N-channel MOSFET. LDRV switches from PVDD to PGND.
OSNS	3	O	The output sense pin is connected to a resistor divider from VOUT to GND (identical to the main feedback loop) and is used to sense power good condition and provides reference for the transient comparators.
PGND	10	O	Power (high-current) ground used by LDRV.
PWRGD	9	-	Power good. This is an open-drain output which connects to the supply via an external resistor.
PVDD	12	O	This pin is the regulated output of the charge-pump and provides the supply voltage for the LDRV driver stage. PVDD also drives the bootstrap circuit which generates the voltage on BOOT1.
RT	7	I	External pin for programming the oscillator frequency. Connnected a resistor between this pin and GND.
SGND	8	-	Signal ground
SS/SD	6	I	The soft-start/shutdown pin provides user programmable soft-start timing and shutdown capability for the controller.
SW	14	I	This pin, used for overcurrent, zero-current, and in the anti-cross conduction sensing is connected to the switched node on the converter. Output short circuit is detected by sensing the voltage at this pin with respect to VDD while the high-side switch is on. Zero current is detected by sensing the pin voltage with respect to ground when the low-side rectifier MOSFET is on.
VDD	2	I	Power input for the device. Maximum voltage is 5.5 V. De-coupling of this pin is required.

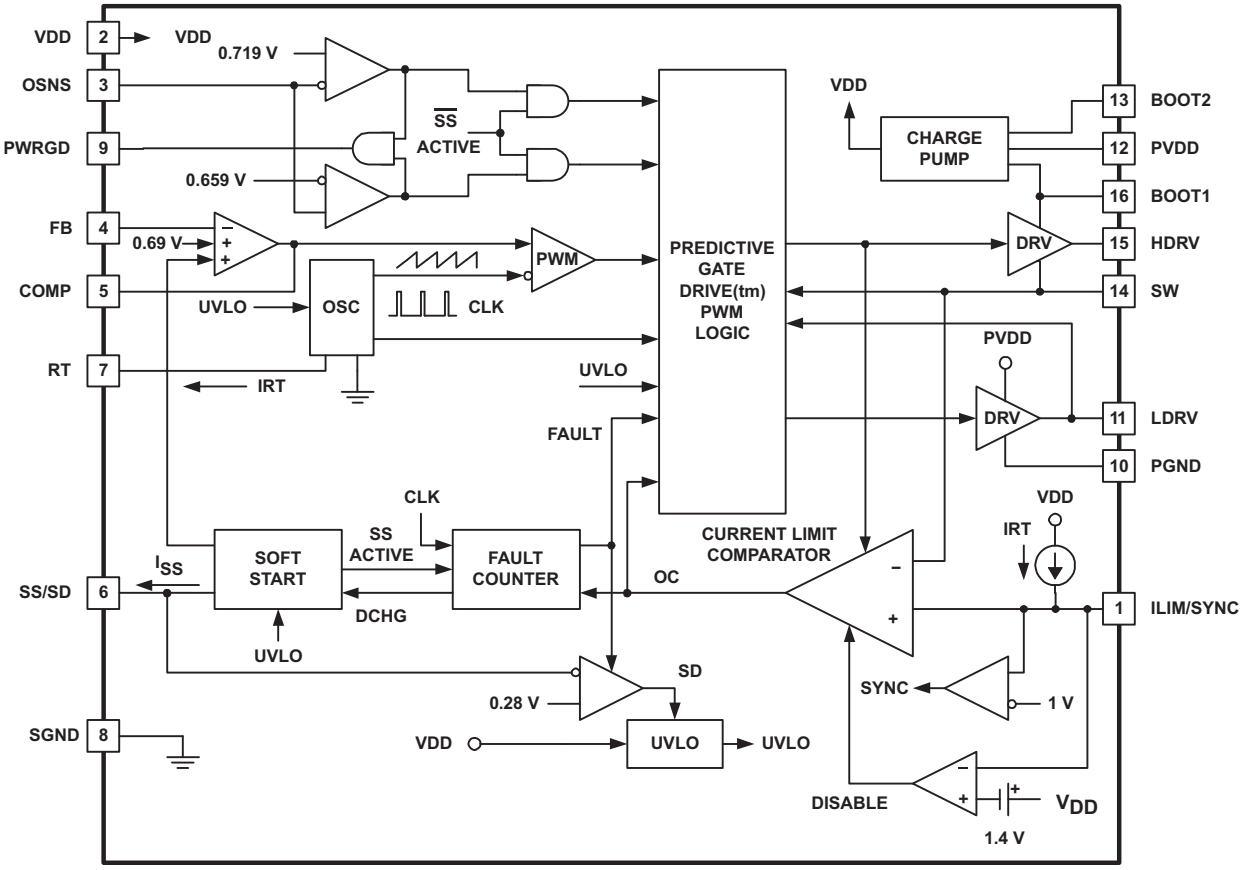
PWP PACKAGE
(TOP VIEW)



A. For more information on the PWP package, refer to TI Technical Brief, Literature No. SLMA002.

B. PowerPAD heat slug must be connected to SGND (Pin 8), or electrically isolated from all other pins.

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

The TPS40021 is a low-input voltage, synchronous, voltage mode-buck controller. A typical application circuit is shown in Figure 1. These controllers are designed to allow construction of high-performance dc-to-dc converters with input voltages from 2.25 V to 5.5 V, and output voltages as low as 690 mV. Using a top side N-channel MOSFET for the primary buck switch results in lower switch resistance for a given gate charge.

The device controls the delays from main switch off to rectifier turn on and from rectifier turn off to main switch turn on in a way that minimizes diode losses (both conduction and recovery) in the synchronous rectifier. The reduction in these losses is significant and can mean that for a given converter power level, smaller FETs can be used, or that heat sinking can be reduced or even eliminated.

The TPS40021 is the controller of choice for most general purpose synchronous buck designs, operating in two quadrant mode (i.e. source or sink current) full time. This device provides the best performance for output voltage load transient response over the widest load current range.

The controller provides for a coarse short circuit current-limit function that provides pulse-by-pulse current limiting, as well as integrates short circuit current pulses to determine the existence of a persistant fault state at the converter output. If a fault is detected, the converter shuts down for a period of time (determined by six soft-start cycles) and then restarts. The current-limit threshold is adjustable with a single resistor connected from VDD to the ILIM/SYNC pin. This overcurrent function is designed to protect against catastrophic faults only, and cannot be guaranteed to protect against all overcurrent conditions.

The controller implements a closed-loop soft start function. Startup ramp time is set by a single external capacitor connected to the SS/SD pin. The SS/SD pin also doubles as a shutdown function.

Voltage Reference

The bandgap cell is designed with a trimmed, curvature corrected (< 1%) 0.69-V output, allowing output voltages as low as 690 mV to be obtained.

Oscillator

The ramp waveform is a saw-tooth form at the PWM frequency with a peak voltage of 1.25 V, and a valley of 0.3 V. The PWM duty cycle is limited to a maximum of 97%, allowing the bootstrap and charge pump capacitors to charge during every cycle.

Bootstrap/Charge Pump

The TPS40021 includes a charge pump to boost the drive voltage to the power MOSFET's to higher levels when the input supply is low. A capacitor connected from PVDD to PGND is the storage cap for the pump. A capacitor connected from SW to BOOT2 gets charged every switching cycle while LDRV is high and its charge is dumped on the PVDD capacitor when HDRV goes high. An internal switch disables the charge pump when the voltage on PVDD reaches approximately 4.8 V and enables pumping when PVDD falls to approximately 4.6 V. The high-side driver uses the capacitor from SW to BOOT1 as its power supply. When SW is low, this capacitor charges from the PVDD capacitor. When the SW pin goes high, this capacitor provides above-rail drive for the high-side N-channel FET.

PVDD, BOOT1 and BOOT2 are pre-charged to the VDD voltage during a shutdown condition. For low-input voltage converters, utilizing higher gate threshold voltage MOSFETs, it may be necessary to add an Schottky diode from VDD (anode) to BOOT1 to guarantee sufficient voltage for initial start up. Once switching starts the charge pump reverses bias on the Schottky diode.

Drivers

The HDRV and LDRV MOSFET drivers are capable of driving gate-to-source voltages up to 5.0 V. Using appropriate MOSFETs, a 25-A converter can be achieved. The LDRV driver switches between VDD and ground, while the HDRV driver is referenced to SW and switches between BOOT1 and SW. The maximum voltage between BOOT1 and SW is 5.0 V when PVDD is in regulation.

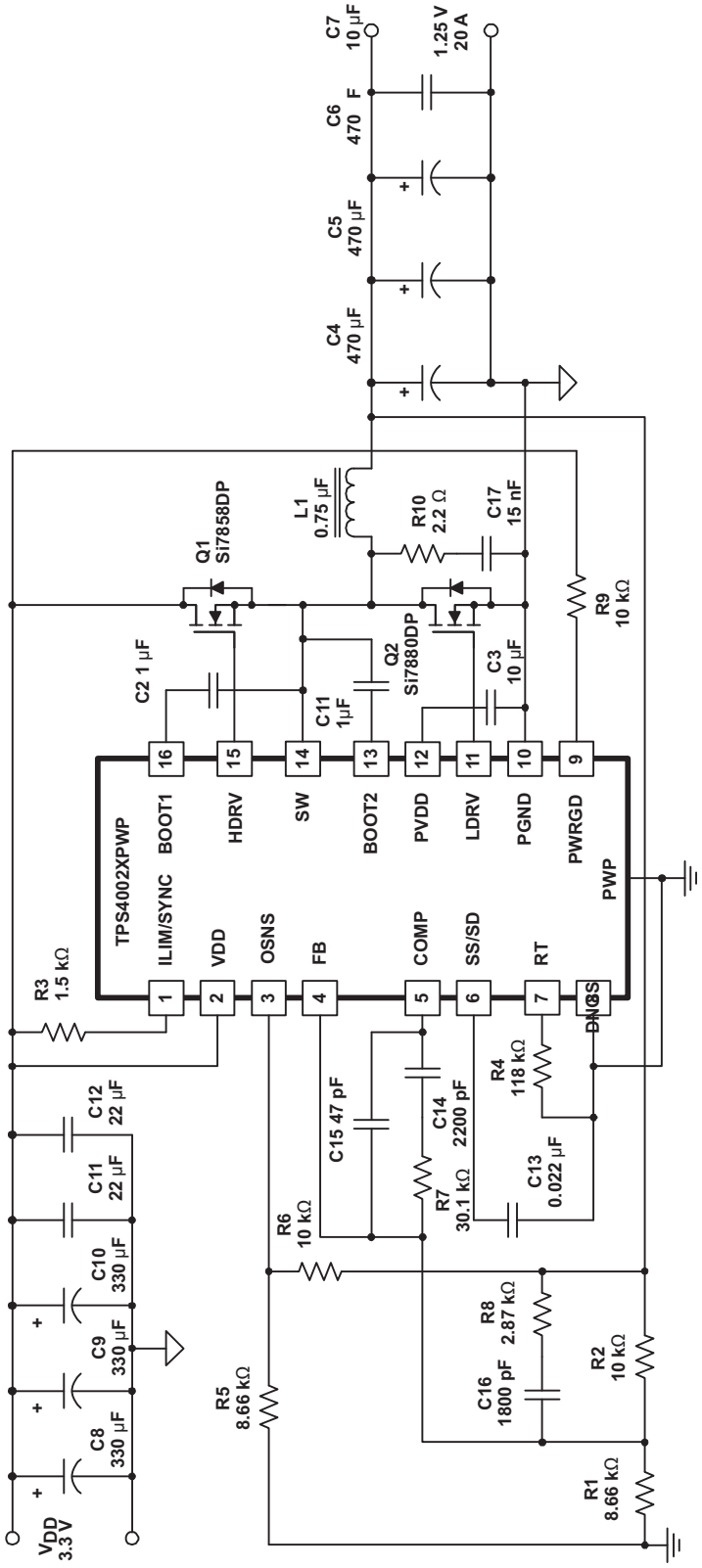


Figure 1. Typical Application

Synchronous Rectification and Predictive Gate Delay

In a normal buck converter, when the high−side switch turns off, current is flowing in the inductor. Since this current cannot be stopped immediately a rectifier or catch device is used to give this current a path to flow and maintain voltage levels at a safe level. This device can be a simple diode or it can be an actively−controlled transistor if a control signal is available to drive it. The TPS40021 provides a signal to drive an N−channel MOSFET as a synchronous rectifier. This control signal is carefully coordinated with the drive signal for the main switch so that there is absolute minimum dead−time between the turn off of one FET and the turn on of the other. This TI−patented function, predictive gate delay, uses information from the current switching cycle to adjust the delays for the next cycle virtually eliminating diode conduction while preventing cross−conduction or shoot through. Figure 2 shows the switch−node voltage waveform for a synchronously rectified buck converter during the synchronous rectification period. Illustrated are the relative effects of a fixed delay drive scheme (constant, pre−set delays for the turn−off to turn−on intervals), an adaptive delay drive scheme (variable delays based on voltages sensed on the current switching cycle) and TI's predictive delay drive scheme. Since the diode voltage drop is greater than the conduction drop of the FET, the longer time spent in diode conduction, the more power dissipated in the rectifier and the lower the efficiency. Also, not shown in the figure, is the fact that the predictive delay circuit can actually prevent the body diode from becoming forward biased at all, avoiding reverse recovery and its associated losses. This results in a significant power savings when the main FET turns on.

The predictive gate drive architecture on the TPS40021 requires a minimum pulse width of greater than 150 ns for proper operation. At pulse widths below 150 ns, the low−side FET turn−on could overlap the high−side FET turn−off leading to cross conduction in the power stage.

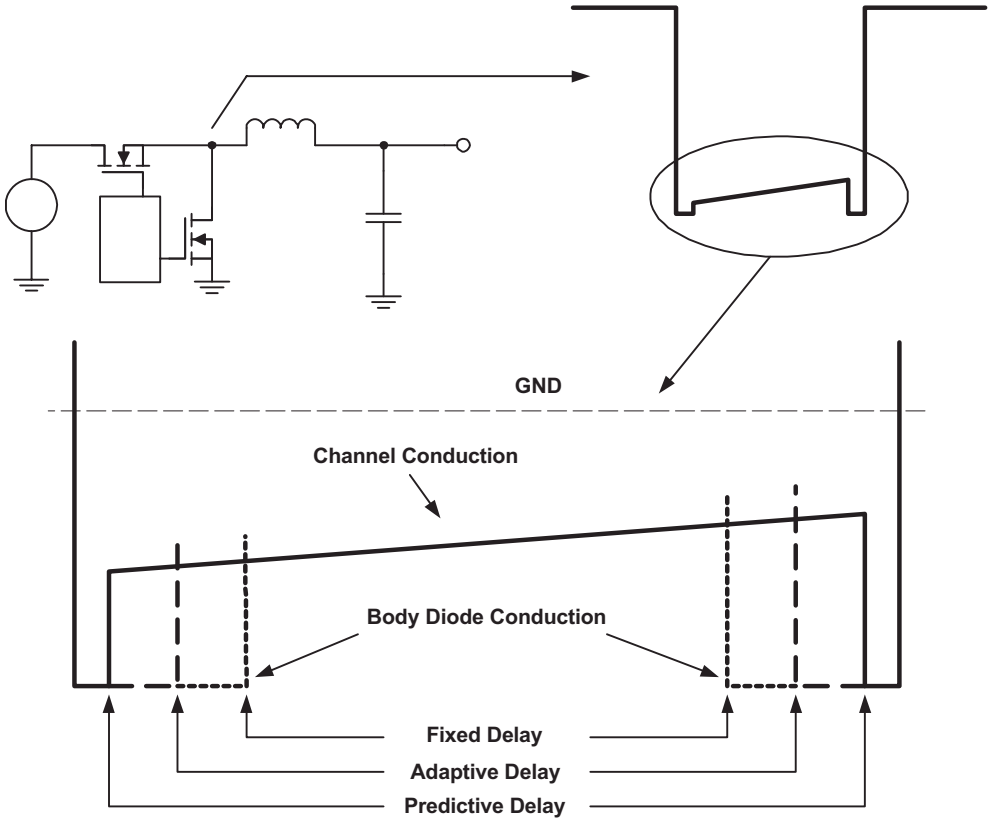


Figure 2. Switch Node Waveforms for Synchronous Buck Converter

Output Short Circuit Protection

Output short circuit protection in the TPS40021 is sensed by looking at the voltage across the main FET while it is on. If the voltage exceeds a pre-set threshold, the current pulse is terminated, and a counter inside the device is incremented. If this counter fills up, a fault condition is declared and the chip disables switching for a period of time and then attempts to restart the converter with a full soft-start cycle. The more detailed explanation follows.

In each switching cycle, a comparator looks at the voltage across the top side FET while it is on. If the voltage across that FET exceeds a programmable threshold voltage, then the current switching pulse is terminated and a 3-bit counter (eight counts) is incremented by one count. If during the switching cycle the top side FET voltage does not exceed a preset threshold, then this counter is decremented by one count. (The counter does not wrap around from seven to zero or from zero to seven). If the counter reaches a full count of seven, the device declares that a fault condition exists at the output of the converter. In this state, switching stops and the soft-start capacitor is discharged. The counter is decremented by one by the soft start cap discharge. When the soft-start capacitor is fully discharged, the discharge circuit is turned off and the cap is allowed to charge up at the nominal charging rate, When the soft-start capacitor reaches approximately 1.3 V, it is discharged again and the overcurrent counter is decremented by one count. The capacitor is charged and discharged, and the counter decremented until the count reaches zero (a total of six times). When this happens, the outputs are again enabled as the soft-start capacitor generates a reference ramp for the converter to follow while attempting to restart. During this soft-start interval (whether or not the controller is attempting to do a fault recovery or starting for the first time), pulse-by-pulse current limiting is in effect, but overcurrent pulses are not counted to declare a fault until the soft-start cycle has been completed. It is possible to have a supply try to bring up a short circuit for the duration of the soft-start period plus seven switching cycles. Power stage designs should take this into account if it makes a difference thermally. Figure 3 shows the details of the overcurrent operation.

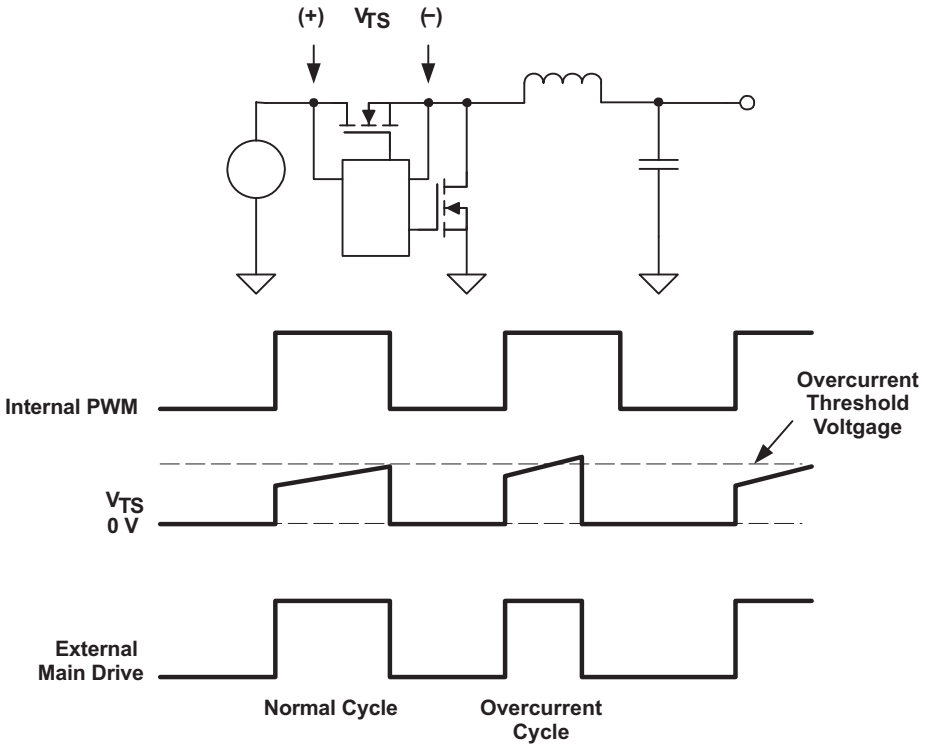


Figure 3. Switch Node Waveforms for Synchronous Buck Converter

Figure 4 shows the behavior of key signals during initial startup, during a fault and a successfully fault recovery. At time t0, power is applied to the converter. The voltage on the soft-start capacitor (VCSS) begins to ramp up At t1, the soft-start period is over and the converter is regulating its output at the desired voltage level. From t0 to t1, pulse-by-pulse current limiting was in effect, and from t1 onward, overcurrent pulses are counted for purposes of determining if a fault exists. At t2, a heavy overload is applied to the converter. This overload is in excess of the overcurrent threshold, the converter starts limiting current and the output voltage falls to some level depending on the overload applied. During the period from t2 to t3, the counter is counting overcurrent pulses and at time t3 reaches a full count of 7. The soft-start capacitor is then discharged, the outputs are disabled, the counter decremented, and a fault condition is declared.

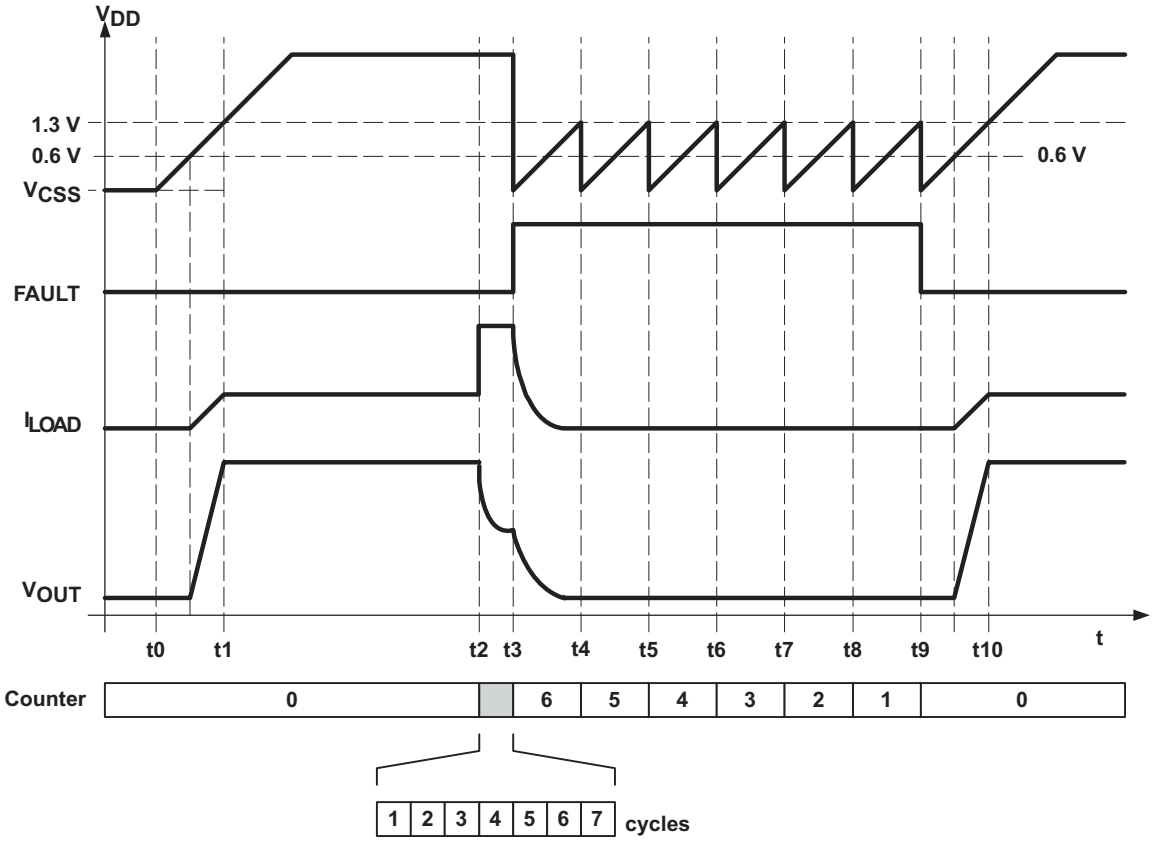


Figure 4. Overcurrent/Fault Waveforms

When the soft-start capacitor is fully discharged, it begins charging again at the same rate that it does on startup, with a nominal 3-µA current source. As the capacitor voltage reaches full charge, it is discharged again and the counter is decremented by one count. These transitions occur at t3 through t9. At t9, the counter has been decremented to zero. Now the fault logic is cleared, the outputs are enabled and the converter attempts to restart with a full soft-start cycle. The converter comes into regulation at t10.

The internal SS signal is a diode drop below V_{CSS}. When V_{CSS} reaches one diode drop above ground, (≅ 0.6 V) the output (V_{OUT}) begins it's soft-start ramp.

Setting the Short Circuit Current Limit Threshold

Connecting a resistor from VDD to ILIM sets the current limit. A current sink in the chip causes a voltage drop across the resistor connected to ILIM. This voltage drop is the short circuit current threshold for the part. The current that the ILIM pin sinks is dependent on the value of the resistor connected to RT and is given by:

$$I_{LIM} = 19 \bullet \frac{0.69\ V}{R_T} \quad (1)$$

The tolerance of the current sink is too loose to do an accurate current limit. The main purpose is for hard fault protection of the power switches. Given the tolerance of the ILIM sink current, and the $R_{DS(on)}$ range for a MOSFET, it is generally possible to apply a load that thermally damages the converter. This device is intended for embedded converters where load characteristics are defined and can be controlled. A small capacitor can be added between ILIM and VDD for filtering. However, capacitors should not be used if the synchronization function is to be used.

Soft-Start and Shutdown

The soft−start and shutdown functions are common to the SS/SD pin. The voltage at this pin over−rides the reference voltage on the error amplifier during startup. This controls the output voltage slew rate and the surge current required to charge the output capacitor at startup, allowing for a smooth startup with no overshoot of the output voltage. Initial HDRV pulse widths during Soft−Start are typically very narrow, likely less than 150ns. As a result, HDRV and LDRV can be on simultaneously, resulting in cross−conduction the MOSFETs of the power stage. To minimize cross−conduction during soft−start, the soft−start time when the pulse widths are less than 150ns should be kept to a minimum. A shutdown feature can be implemented by pulling SS/SD to GND via a transistor as shown in Figure 5.

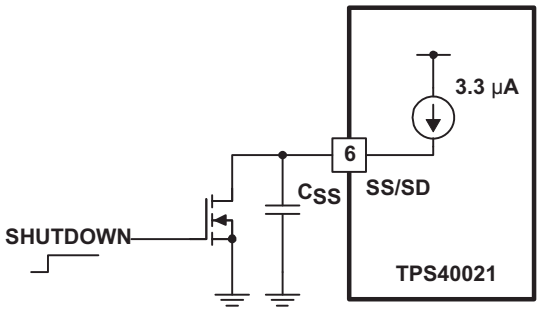


Figure 5. Shutdown Implementation

$$C_{SS} = \frac{I_{SS}}{V_{FB}} \bullet t_{SS}\ (F) \tag{2}$$

where t_{SS} is the start up time in seconds.

Switching Frequency

The switching frequency is programmed by a resistor from RT to SGND. Nominal switching frequency can be calculated by:

$$R_T\ (k\Omega) = \frac{37.736 \bullet 10^3}{f_{OSC}\ (kHz)} - 5.09\ (k\Omega) \tag{3}$$

Synchronization

The TPS40021 can be synchronized to an external reference frequency higher than the free running oscillator frequency. The recommended method is to use a diode and a push pull drive signal as shown in Figure 6.

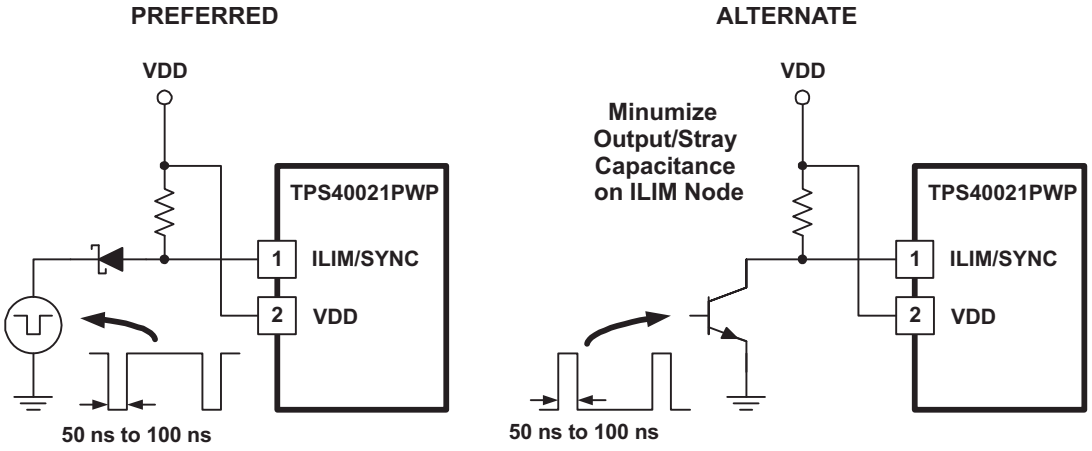


Figure 6. Synchronization Methods

This design allows synchronization up to the maximum operating frequency of 1 MHz. For best results the nominal operating frequency of a converter that is to be synchronized should be kept as close as practicable to the synchronization frequency to avoid excessive noise induced pulse width jitter. A good target is to shoot for the free run frequency to be 80% of the synchronized frequency. This ensures that the synchronization source is the frequency determining element in the system and not to adversely affect noise immunity.

Other methods of implementing the synchronization function include using an open collector or open drain output device directly, or discreet devices to pull the ILIM/SYNC pin down. These do work but performance can suffer at high frequency because the ILIM/SYNC pin must rise to (V_{DD} − 1.0 V) before the next switching cycle begins. Any time that this requires is directly subtracted from the maximum pulse width available and should be considered when choosing devices to drive ILIM/SYNC. Consequently, the lowest output capacitance devices work best.

During a synchronization cycle, the current sink on the ILIM/SYNC pin becomes disabled when ILIM/SYNC is pulled below 1.0 V. The ILIM/SYNC current sink remains disabled until ILIM/SYNC reaches (V_{DD} −1.0 V) This removes the load on the ILIM/SYNC pin to allow the voltage to slew rapidly depending on the ILIM resistor and any stray capacitance on the pin. To maximize this slew rate, minimize stray capacitance on this pin.

The duration of the synchronization pulse pulling ILIM/SYNC low shoud be between 50 ns and 100 ns. Longer durations may limit the maximum obtainable duty cycle.

Transient Comparators and Power Good

The TPS40021 makes use of a separate pin, OSNS, to monitor output voltage for these two functions. In normal operation, OSNS is connected to the output via a resistor divider. It is important to make this divider the same ratio as the divider for the feedback network so that in normal operation the voltage at OSNS is the same as the voltage at FB, 0.69 V nominal.

The PWRGD pin is an open drain output that is pulled low when the voltage at OSNS falls outside 0.69 V ±4.6% (approximately). A delay has been purposely built into the PWRGD pin pulling low in response to an out of band voltage on OSNS, to minimize the need for filtering the signal in the event of a noise glitch causing a brief out of band OSNS voltage. The PWRGD signal returns to high when the OSNS signal returns to approximately ±1% of nominal (0.69 V ±1%).

The transient comparators override the conventional voltage control loop when the output voltage exceeds a ±4.6% window. If the output transition is high (i.e. load steps down from 90% load to 10 % load) then the HDRV gate drive is terminated, 0% duty cycle, the LDRV gate drive is turned on to sink output current until V_{OUT} returns to within 1% of nominal. Conversely when V_{OUT} drops outside the window (i.e. step load increases from 10% load to 90% load) HDRV increases to maximum duty cycle until V_{OUT} returns to within 1% of nominal (see Figure 7).

During start-up, the transient comparators control the state of PWRGD as previously described. However, the operation of the gate drive outputs is not affected (see Figure 8).

The transient comparators provide an improvement in load transient recovery time if used properly. In some situations, recovery time may be one half of the time required without transient comparators. Keep in mind that the transient comparator concept is a double-edged sword. While they provide improved transient recovery time, they can also lead to instability if incorrectly applied. For proper functionality, design a feedback loop for the converter that places the closed loop unity gain frequency at least five times higher than the 0-dB frequency of the output L-C filter. If not, the feedback loop cannot respond to the ring of the L-C on a transient event. The ring is likely to be large enough to disturb the transient comparators and the result is a power oscillator. Another helpful action is to ground the feedback loop divider and the OSNS divider at the SGND pin. Make sure both dividers measure the same physical location on the output bus. These help avoid problems with resistive drops at higher loads causing problems.

Connecting OSNS to VDD disables the transient comparators. This also disables the PWRGD function. Alternatively, OSNS and FB can be tied together. This connection allows a proper PWRGD at startup, though transient performance diminishes.

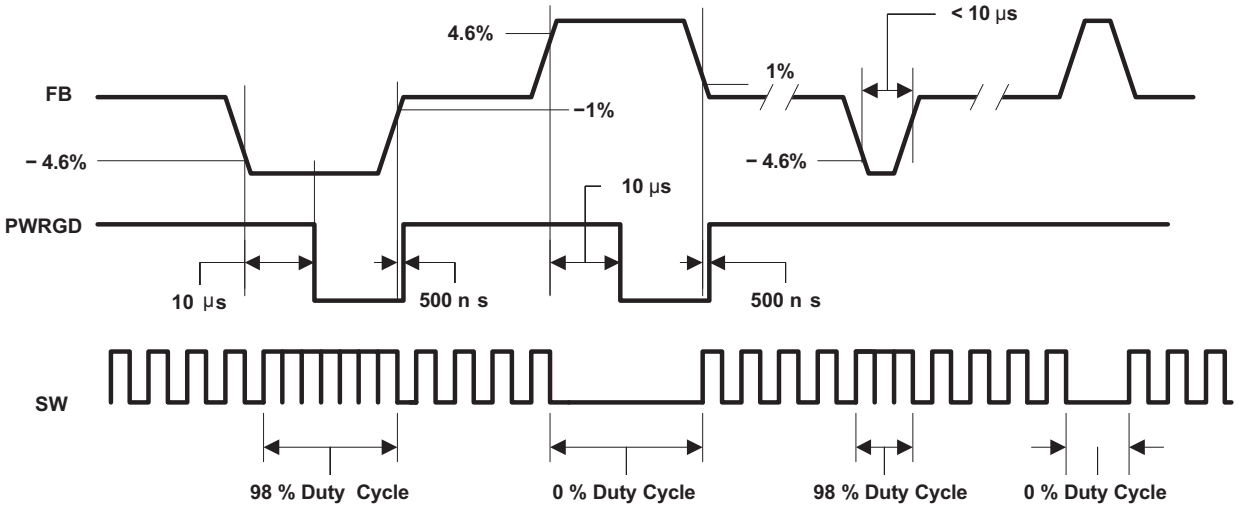


Figure 7. Duty Cycle Waveforms

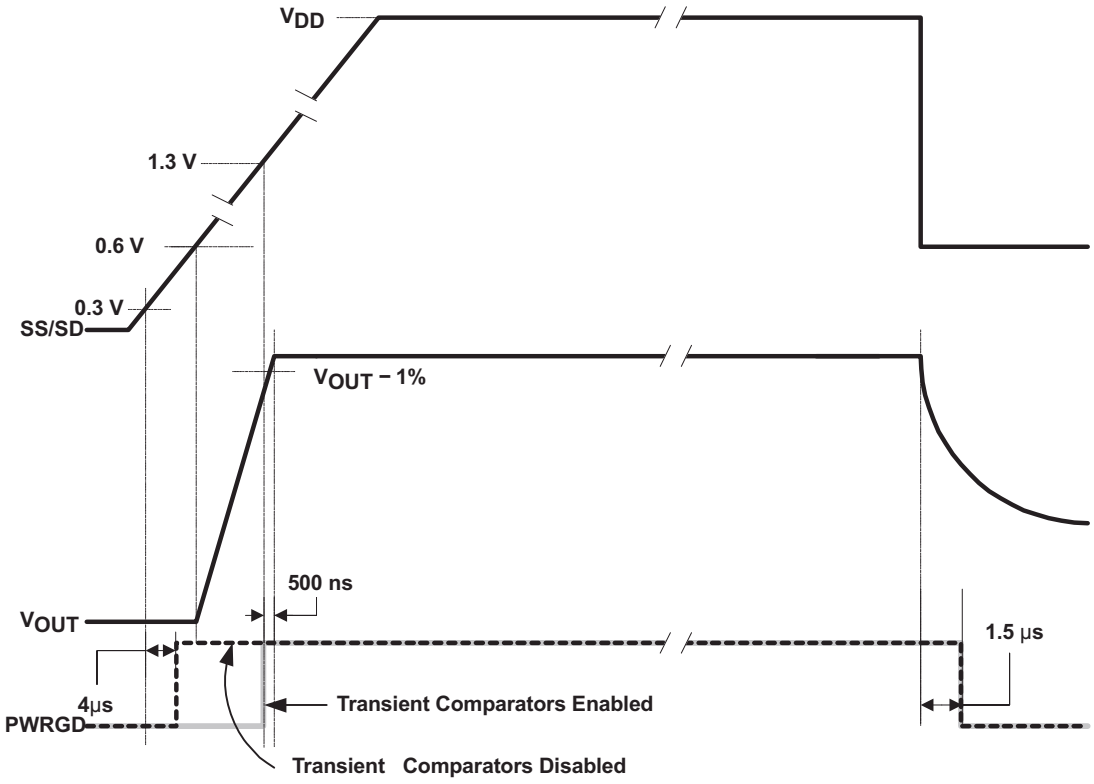


Figure 8. Transient Comparator Waveforms

Layout Considerations

Successful operation of the TPS40021 is dependent upon the proper converter layout and grounding techniques. High current returns for the SR MOSFET's source, input capacitance, output capacitance, PVDD capacitance, and input bypass capacitors (if applicable), should be kept on a single ground plane or wide trace connected to the PGND (pin10) through a short wide trace. Control components connected to signal ground, as well as the PowerPad thermal pad, should be connected to a single ground plane connected to SGND (pin 8) through a short trace. SGND and PGND should be connected at a single point using a narrow trace.

Proper operation of Predictive Gate Drive technology and I_{ZERO} functions are dependent upon detecting low-voltage thresholds on the SW node. To ensure that the signal at the SW pin accurately represents the voltage at the main switching node, the connection from SW (pin 14) to the main switching node of the converter should be kept as short and wide as possible and should ideally be kept on the top level with the power components. If the SW trace must traverse multiple board layers between the TPS40021 and the main switching node, multiple vias should be used to minimize the trace impedance.

Gate drive outputs, LDRV and HDRV (pins 11 and 15, respectively) should be kept as short as possible to minimize inductances in the traces. If the gate drive outputs need to traverse multiple board layers multiple vias should be used.

Charge pump components, BOOT1, BOOT2, PVDD, and any input bypass capacitors (if required), should be kept as close as possible to their respective pins. Ceramic bypass capacitors should be used if the input capacitors are located more than a couple of inches away from the TPS40021. If a bypass capacitor is not needed the trace from the input capacitors to VDD (pin2) should be kept as short and wide as possible to minimize trace impedance. If multiple board layers are traversed multiple vias should be used.

Manufacturer's instructions should be followed for proper layout of the external MOSFETs. Thermal impedances given in the manufacturer's datasheets are for a given mounting technique with a specified surface area under the drain of the MOSFET. PowerPad package information can be found in the APPLICATION INFORMATION section of this datasheet.

Refer to TPS40021 EVM−001 High Efficiency Synchronous Buck Converter with PWM Controller Evaluation Module (HPA009) User's Guide, (Literature No. SLUU144A) for a typical board layout.

The PowerPAD package provides low thermal impedance for heat removal from the device. The PowerPAD derives its name and low thermal impedance from the large bonding pad on the bottom of the device. The circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depends on the size of the PowerPAD package. For a 16-pin TSSOP (PWP) package the area is 5 mm x 3.4 mm [3].

Thermal vias connect this area to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the solder-tinned area under the device during solder reflow. Drill diameters of 0.33 mm (13 mils) works well when 1-oz copper is plated at the surface of the board while simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a diameter equal to the via diameter of 0.1 mm minimum. This capping prevents the solder from being wicked through the thermal vias and potentially creating a solder void under the package. Refer to PowerPAD Thermally Enhanced Package[3] for more information on the PowerPAD package.

REFERENCE DESIGN

This design used the TPS40020 PWM controller to facilitate a step-down application from 3.3-V to 1.5 V (see Figure 11). Design specifications include:

- Input voltage: 2.5 V ≤ V_{IN} ≤ 5.0 V
- Nominal output voltage: 3.3 V
- Output voltage V_{OUT}: 1.5 V
- Output current I_{OUT}: 20 A
- Switching frequency: 300 kHz

Setting the Frequency

Choosing the optimum switching frequency is complicated. The higher the frequency, the smaller the inductance and capacitance needed, so the smaller the size, but then the the switching losses are higher, the efficiency is poorer. For this evaluation module, 300 kHz is chosen for reasonable efficiency and size.

A resistor R4, which is connected from pin 7 to ground, programs the oscillator frequency. The approximate operating frequency is calculated in Equation 3.

Using Equation 2, R_T is calculated to be 120 kΩ and a 118-kΩ resistor is chosen for 300 kHz operation.

Inductance Value

The inductance value can be calculated by Equation 4.

$$L_{(min)} = \frac{V_{OUT}}{f \bullet I_{RIPPLE}} \bullet 3 - \frac{V_{OUT}}{V_{IN(max)}} \tag{4}$$

where I_{RIPPLE} is the ripple current flowing through the inductor, which affects the output voltage ripple and core losses.

Based on 24% ripple current and 300 kHz, the inductance value is calculated to 0.71 µH and a 0.75-µH inductor (part number is CDEP149−0R7) is chosen. The DCR of this inductor is 1.1 mΩ and the loss is 440 mW, which is approximately 1.5% of output power.

$$C_{OUT(min)} = \frac{I_{RIPPLE}}{8 \bullet f \bullet V_{RIPPLE}} \tag{5}$$

$$ESR_{OUT} = \frac{V_{RIPPLE}}{I_{RIPPLE}} \tag{6}$$

With 1.2% output voltage ripple, the needed capacitance is at least 109 µF and its ESR should be less than 3.75 mΩ. Three 2-V, 470-µF, POSCAP capacitors from Sanyo are used. The ESR is 10 mΩ each.

The required input capacitance is calculated in Equation 7. The calculated value is approximately 390 µF for a 100-mV input ripple. Three 6.0-V, 330-µF POSCAP capacitors with 10 mΩ ESR are used to handle 10 A of RMS input current. Additionally, two ceramic capacitors are used to reduce the switching ripple current.

$$C_{IN(min)} = I_{OUT(max)} \bullet D_{(max)} \bullet \frac{1}{f_{OSC} \bullet V_{IN(ripple)}} \tag{7}$$

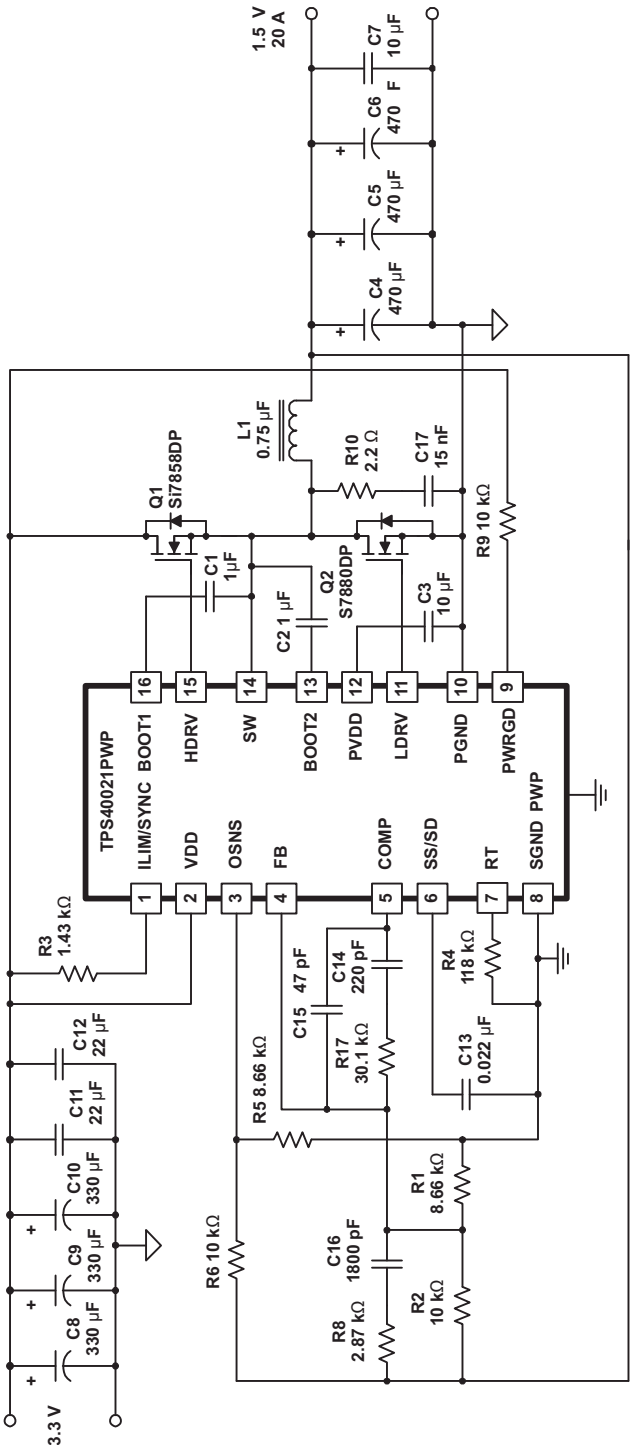


Figure 9. Reference Design Schematic

Input and Output Capacitors

The output capacitance and its ESR needed are calculated in Equation 5 and Equation 6.

Compensation Design

Voltage-mode control is used in this evaluation module, using R2, R7, R8, C14, C15, and C16 to form a Type-III compensator network. The L-C frequency of the power stage is approximately 4.9-kHz and the ESR-zero is around 34 kHz. The overall crossover frequency, f_{0db}, is chosen at 43-kHz for reasonable transient response and stability. Two zeros f_{Z1} and f_{Z2} from the compensator are set at 2.4 kHz and 4 kHz. The two poles, f_{P1} and f_{P2} are set at 34 kHz and 115 kHz. The frequency of poles and zeros are defined by the following equations:

$$f_{Z1} = \frac{1}{2\pi \bullet R7 \bullet C14} \tag{8}$$

$$f_{Z2} = \frac{1}{2\pi \bullet R2 \bullet C16} \quad (assuming\ R2 > R8) \tag{9}$$

$$f_{P1} = \frac{1}{2\pi \bullet R8 \bullet C16} \tag{10}$$

$$f_{P2} = \frac{1}{2\pi \bullet R7 \bullet C15} \quad (assuming\ C14 > C15) \tag{11}$$

The transfer function for the compensator is calculated in Equation 12.

$$A(s) = \frac{(1 + s \bullet C14 \bullet R7) \bullet [1 + s \bullet C16 \bullet (R2 + R3)]}{s \bullet R2 \bullet C14 \bullet [(1 + \frac{C15}{C14}) + s \bullet R7 \bullet C15] \bullet (1 + s \bullet R8 \bullet C16)} \tag{12}$$

Figure 10 shows the close loop gain and phase. The overall crossover frequency is approximately 30 kHz. The phase margin is 57°.

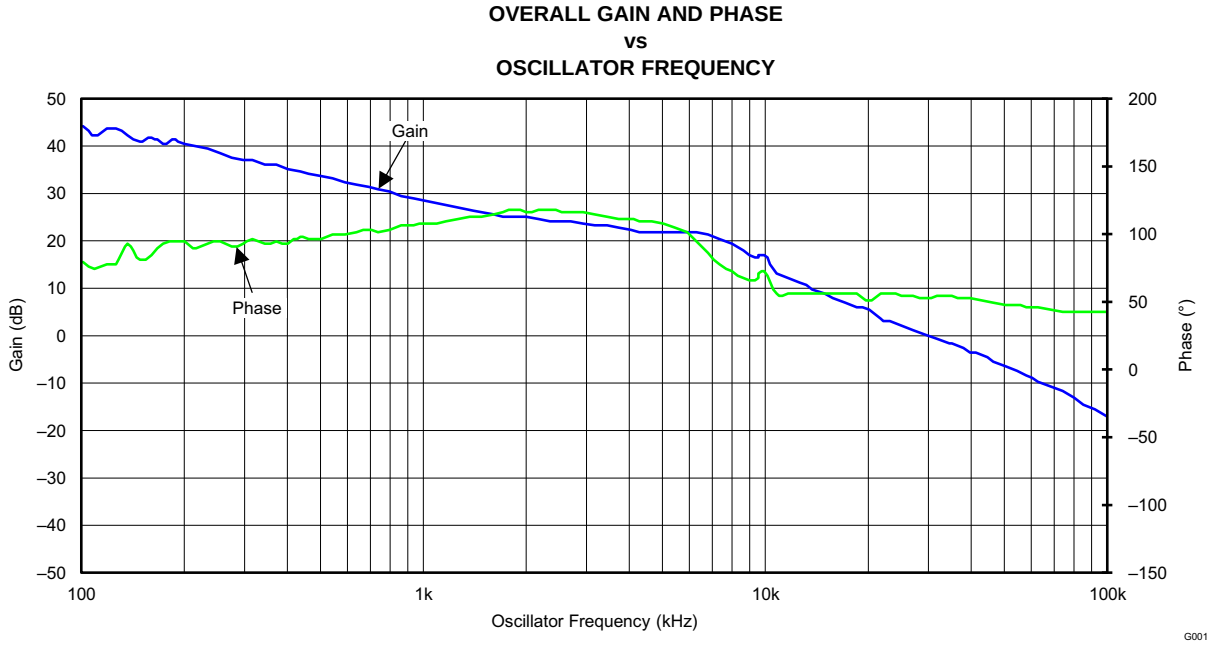


Figure 10.

MOSFETs and Diodes

For a 1.5-V output voltage, the lower the $R_{DS(on)}$ of the MOSFET, the higher the efficiency. Due to the high current and high conduction loss, the MOSFET should have very low conduction resistance ($R_{DS(on)}$) and thermal resistance. Si7858DP is chosen for its low $R_{DS(on)}$ (between 3 mΩ and 4 mΩ) and Power-Pak package.

Current Limiting

Resistor R3 sets the short current limit threshold. The $R_{DS(on)}$ of the upper MOSFET is used as a current sensor. The current limit, $I_{OUT(CL)}$ is initialized at 30% above the maximum output current, $I_{OUT(max)}$, which is 28 A. Then R3 can be calculated in Equation 14 and yields a value of 1.4 kΩ. An R3 of 1.43 kΩ is selected.

$$I_{LIM} = (19 \bullet \frac{V_{FB}}{R4}) = (19 \bullet \frac{0.69\ V}{118\ k\Omega}) = 111.1\ (\mu A) \quad (13)$$

$$R3 = \frac{K \bullet R_{DS(on)} \bullet I_{OUT(CL)}}{I_{LIM}} = \frac{1.5 \bullet 0.004 \bullet 28A}{I_{LIM}} = 1.4\ (k\Omega) \quad (14)$$

where

$R_{DS(on)}$ is the on-resistor of Q1 (4 mΩ)

Temperature coefficient, K=1.5

V_{FB} = 0.69 V

R4 = 118 kΩ

Voltage Sense Regulator

R1 and R2 operate as the output voltage divider. The error amplifier reference voltage (V_{FB}) is 0.69 V. The relationship between the output voltage and divider is described in Equation 15. Using a 10-kΩ resistor for R2 and 1.5-V output regulation, R1 is calculated as 8.52 kΩ, 8.66 kΩ is selected for R1.

$$\frac{V_{FB}}{R1} = \frac{V_{OUT}}{R1 + R2} \rightarrow \frac{0.69V}{R1} = \frac{1.5V}{R1 + 10k\Omega} \rightarrow R1 = 8.52k\Omega \quad (15)$$

Transient Comparator

The output voltage transient comparators provide a quick response, first strike, approach to output voltage transients. The output voltage is sensed through a resistor divider at the OSNS pin, using R5 and R6 shown in Figure 9. If an overvoltage condition is detected, the HDRV gate drive is shut off and the LDRV gate drive is turned on until the output is returned to regulation. Similarly, if an output undervoltage condition is sensed, the HDRV gate drive goes to 95% duty cycle to pump the output back up quickly. The voltage divider should be exactly the same as resistors R1 and R2 discussed previously. Resistor R5 = 8.66 kΩ and R6 = 10 kΩ in this evaluation module.

Efficiency Curves

The tested efficiency at different loads and input voltages are shown in Figure 11. The maximum efficiency is as high as 93% at 1.5-V output. The efficiency is around 88% when the load current (I_{LOAD}) is 20 A.

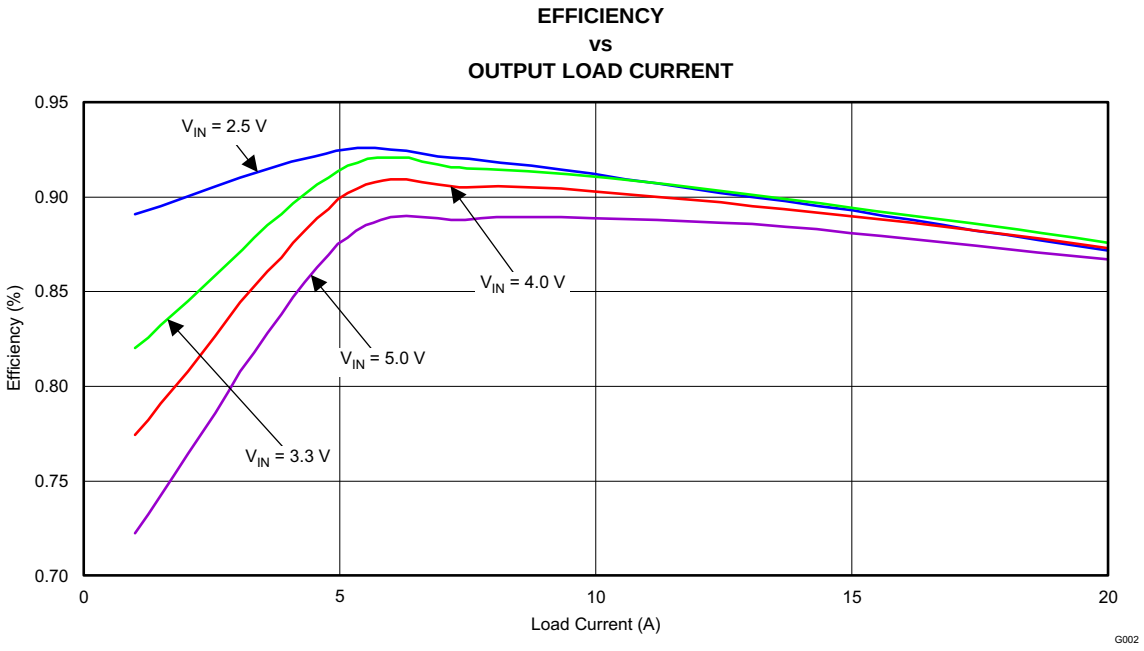


Figure 11.

Typical Operating Waveforms

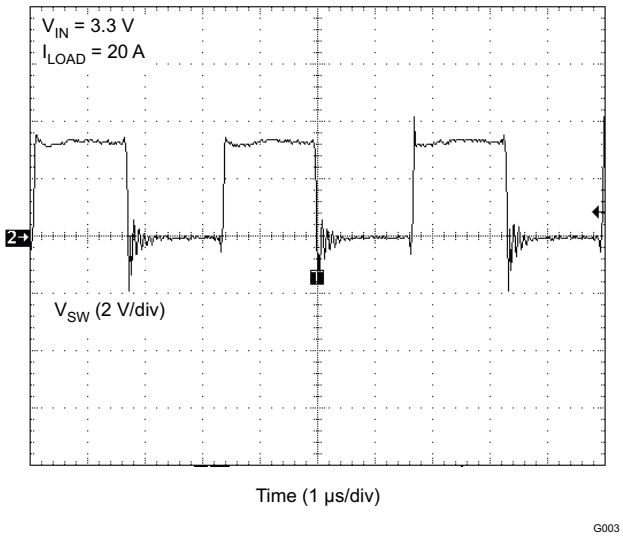


Figure 12.

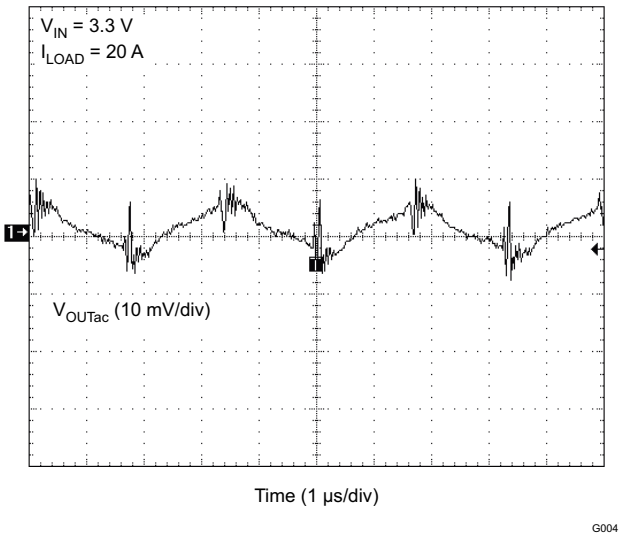


Figure 13.

Transient Response and Output Ripple Voltage

The output ripple is about 15 mV_{P-P} at 20-A output. When the load changes from 4 A to 20 A, the overshooting voltage is about 35 mV.

Figure 14 shows the transient waveform with and without the transient comparator. Using the transient comparator yields a settling time of 10-µs faster than without.

The output ripple is about 15 mV_{P-P} at 20-A output. When the load changes from 0 A to 13 A, the overshoot voltage is approximately 80 mV, and the undershoot is is approximately 60 mV as shown in Figure 15. When the transient comparator is triggered, the powergood (PWRGD) signal goes low.

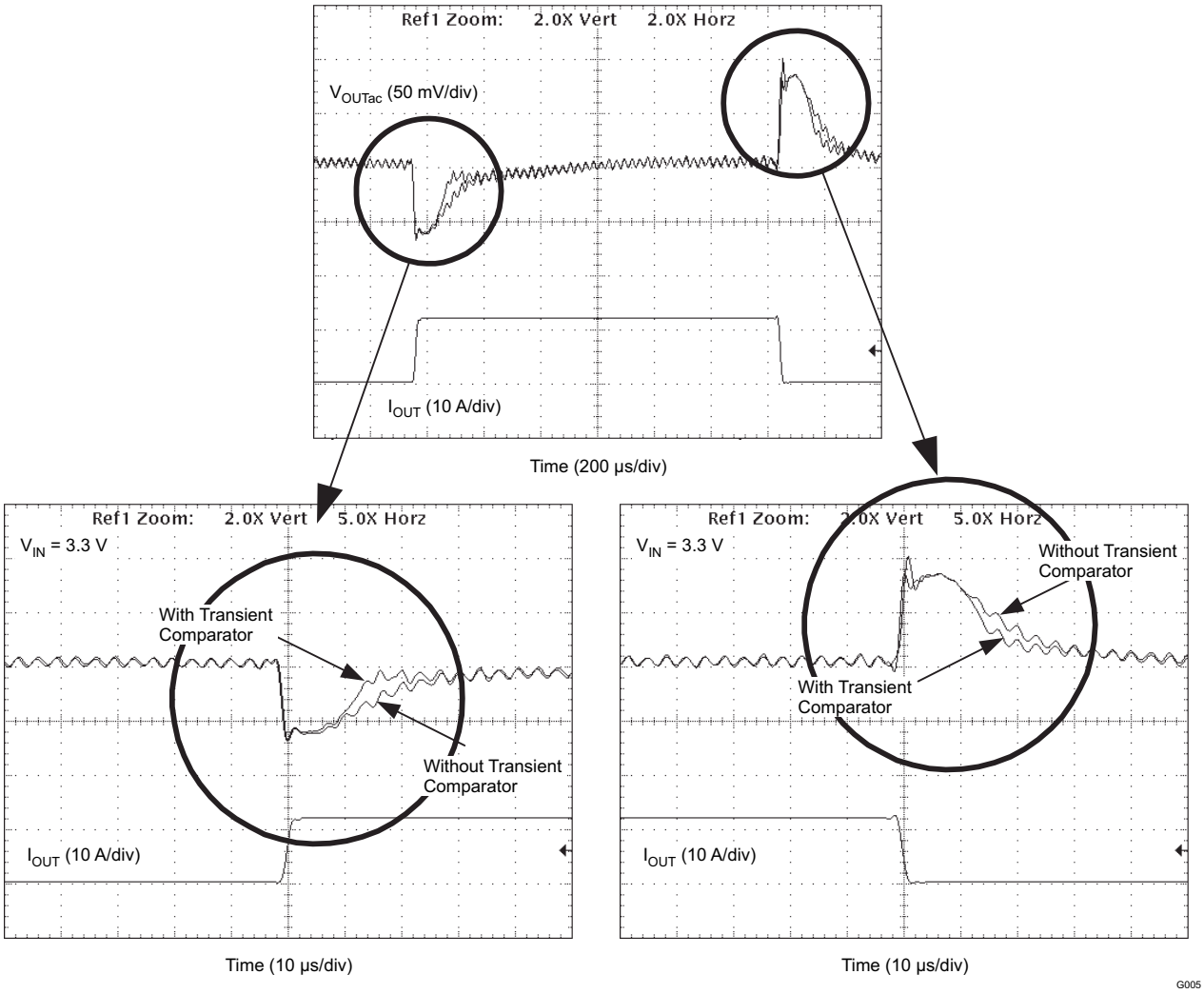


Figure 14. Transient Response Undershoot/Overshoot

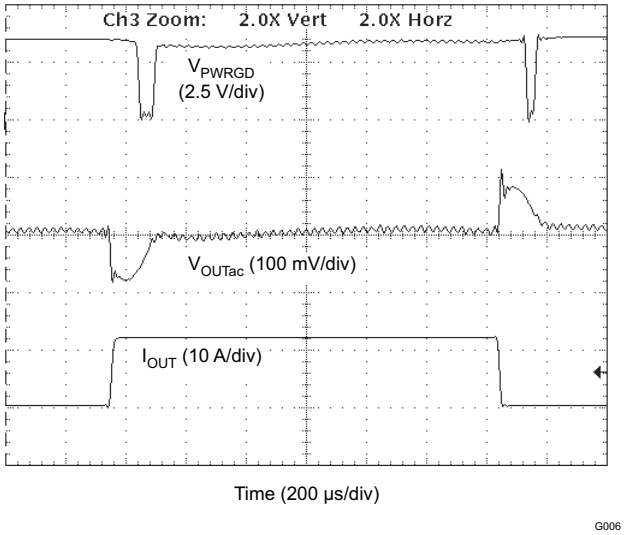


Figure 15. Transient Response

TYPICAL CHARACTERISTICS

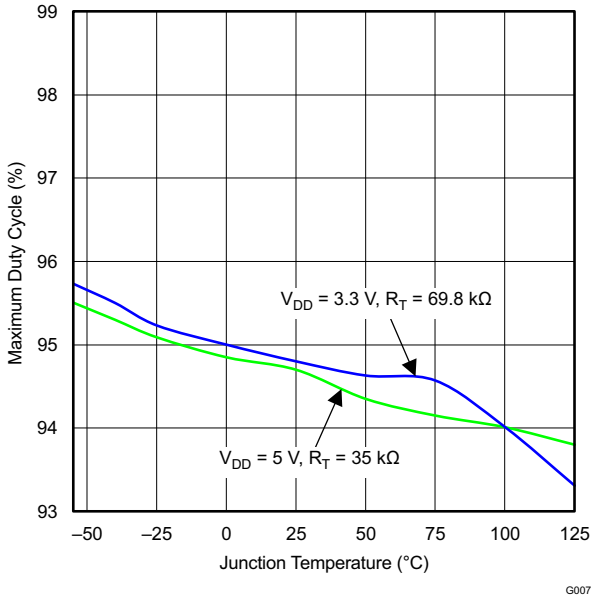


Figure 16.

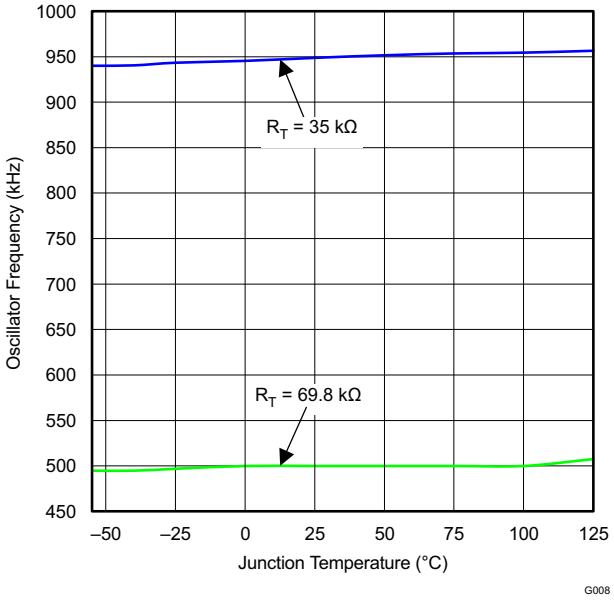


Figure 17.

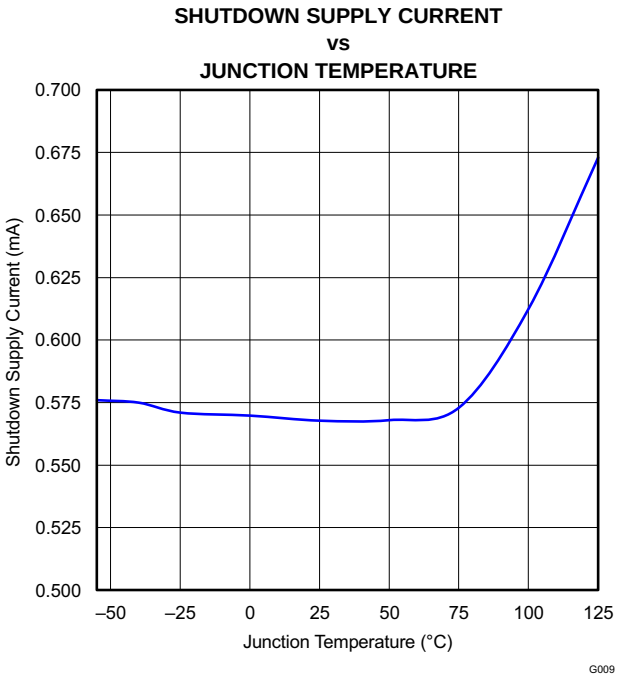


Figure 18.

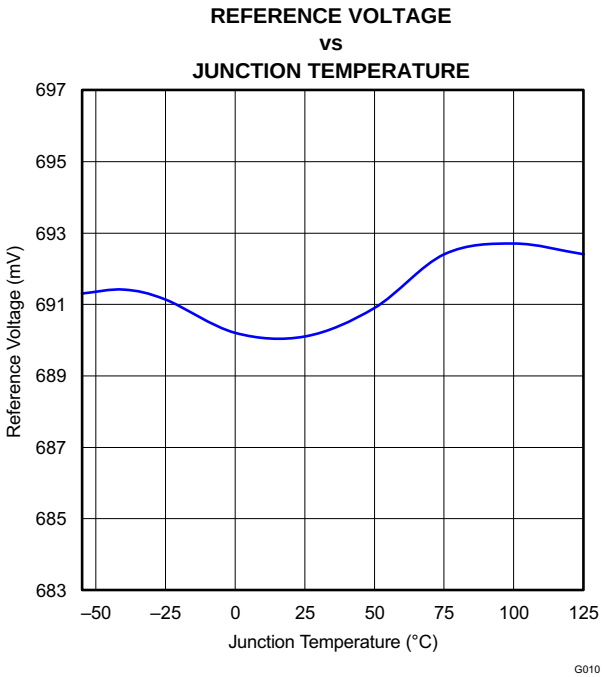


Figure 19.

TYPICAL CHARACTERISTICS (continued)

SWITCHING FREQUENCY vs TIMING RESISTANCE

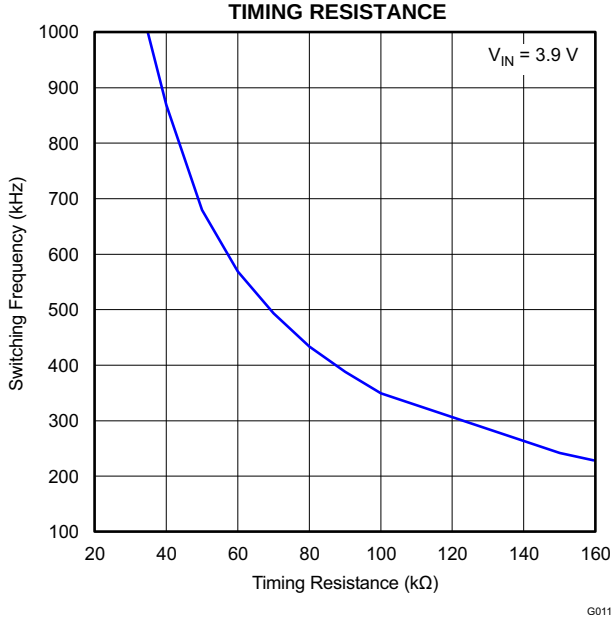


Figure 20.

SOFT-START SOURCING CURRENT vs JUNCTION TEMPERATURE

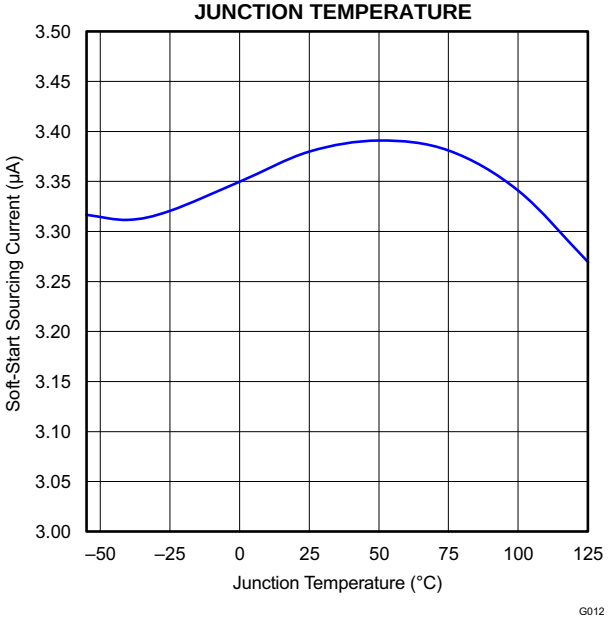


Figure 21.

ILIM OFFSET VOLTAGE vs JUNCTION TEMPERATURE

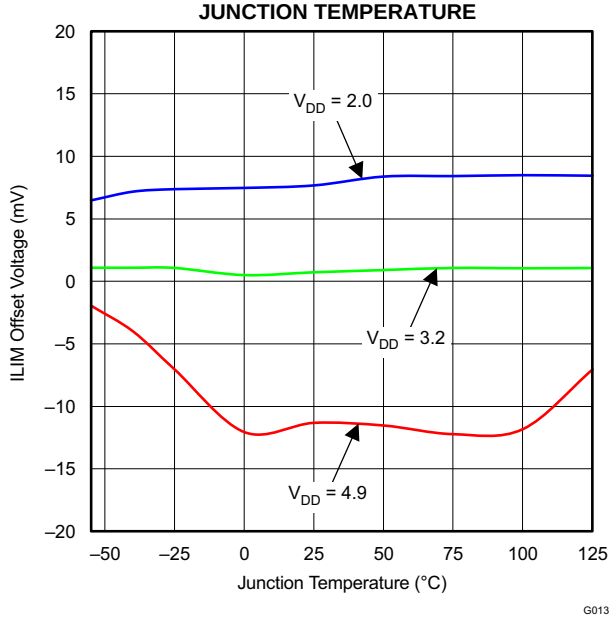


Figure 22.

SHUTDOWN THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

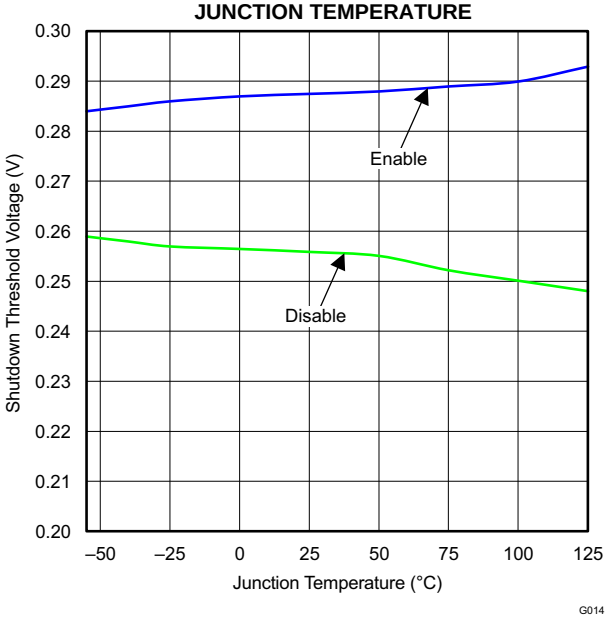


Figure 23.

TYPICAL CHARACTERISTICS (continued)

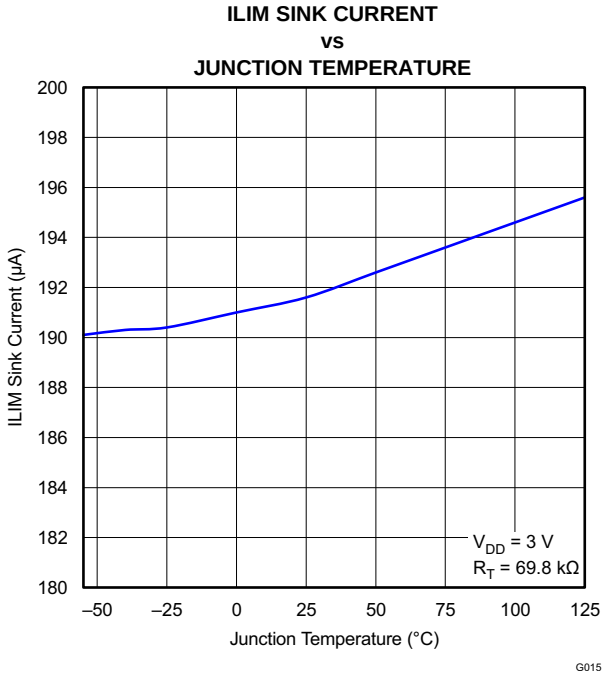


Figure 24.

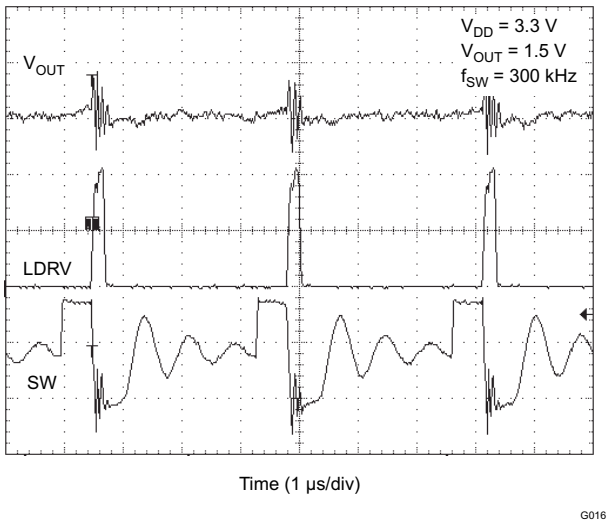


Figure 25. TPS40021 Discontinuous Mode (DCM)

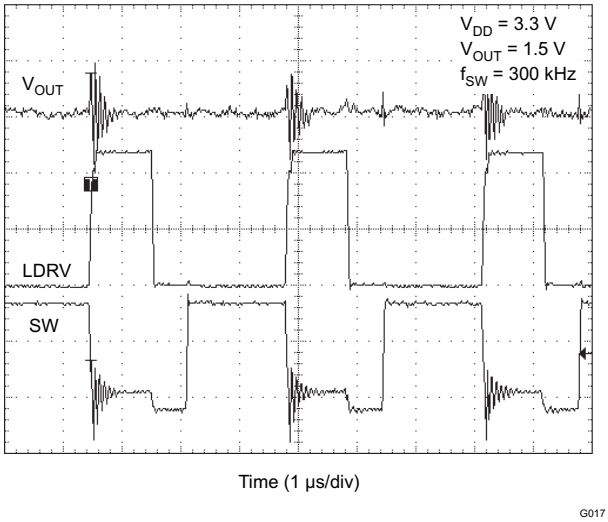


Figure 26. TPS40021 I_{ZERO} Detection – DCM

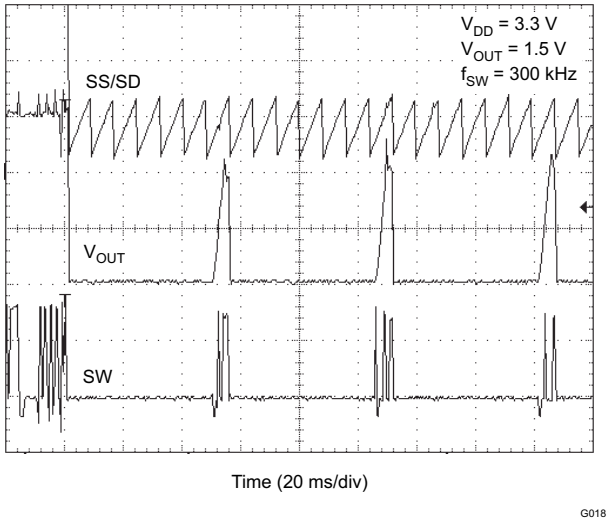


Figure 27. Output Current Fault Operation

TYPICAL CHARACTERISTICS (continued)

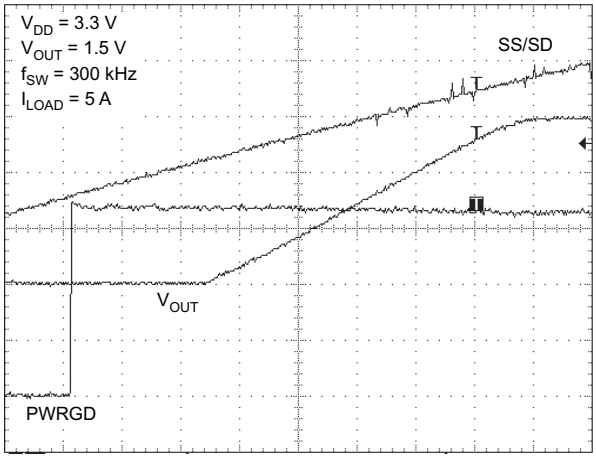


Figure 28. Start-Up Operation Without Transient Comparators

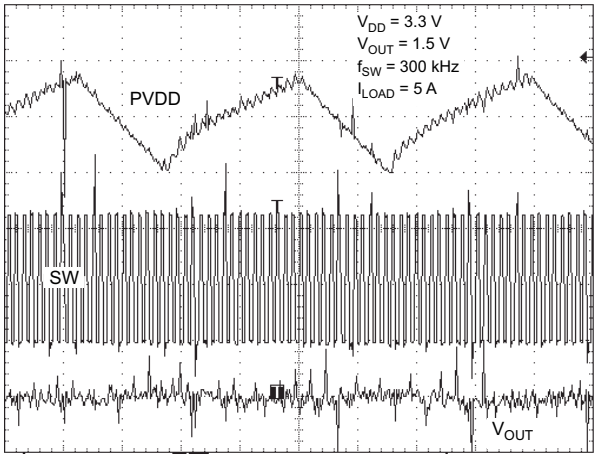


Figure 29. PVDD Hysteresis

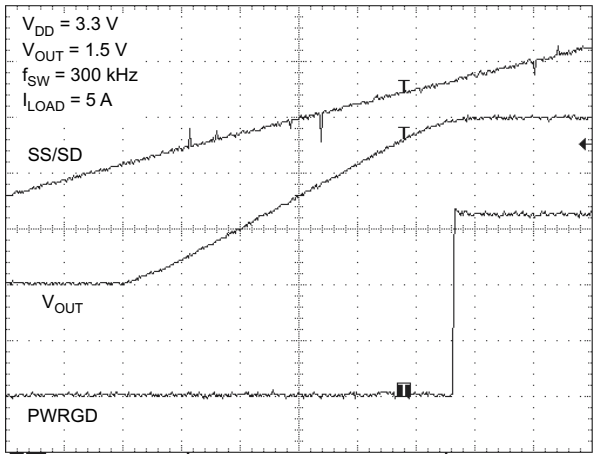


Figure 30. Start-Up Operation With Transient Comparators

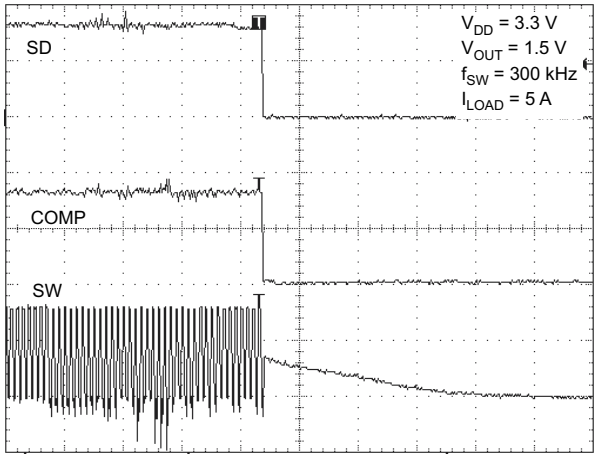


Figure 31. COMP Shutdown Operation

TYPICAL CHARACTERISTICS (continued)

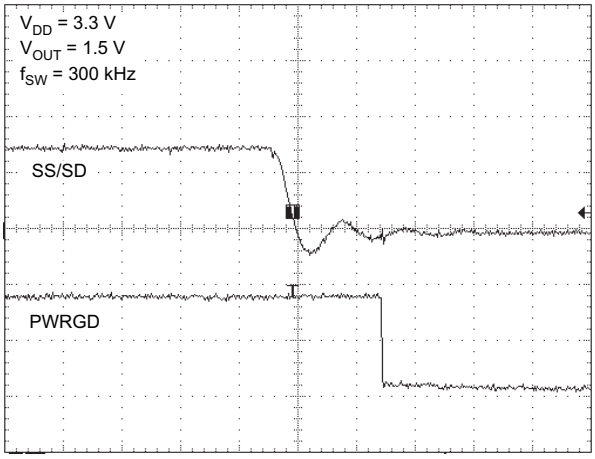


Figure 32. PWRGD Shutdown Operation

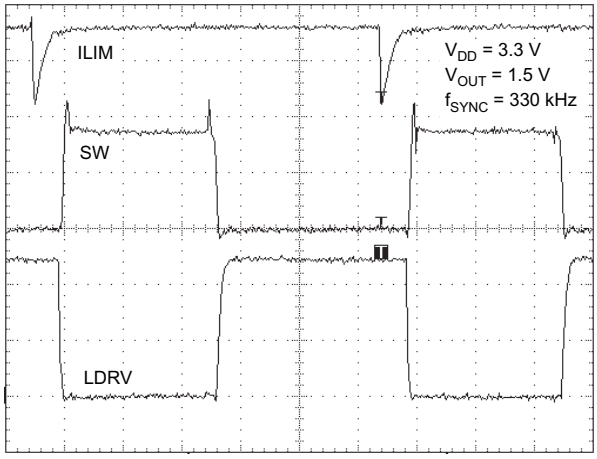


Figure 33. External Synchronization

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40021MPWPEP	ACTIVE	HTSSOP	PWP	16	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	40021M	Samples
TPS40021MPWPREP	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	40021M	Samples
V62/12601-01XE	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	40021M	Samples
V62/12601-01XE-T	ACTIVE	HTSSOP	PWP	16	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	40021M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS40021-EP :

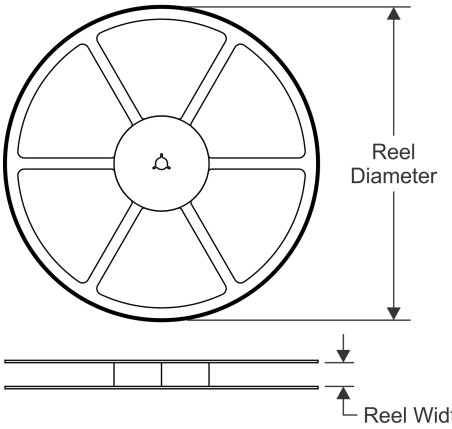
- Catalog: TPS40021

NOTE: Qualified Version Definitions:

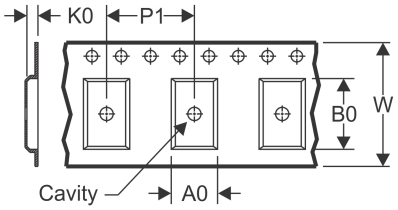
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

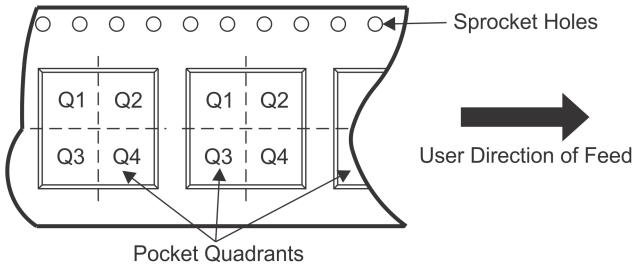


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

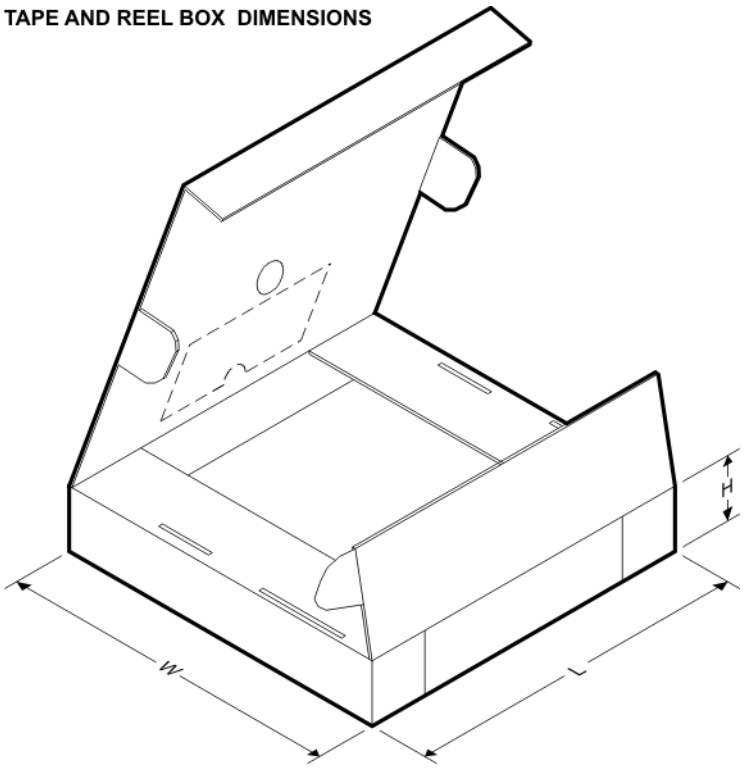
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40021MPWPREP	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

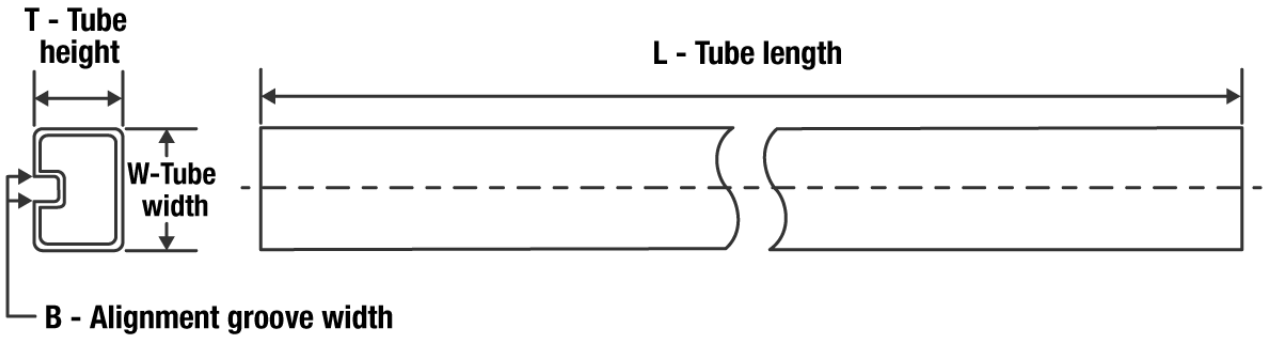
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40021MPWPREP	HTSSOP	PWP	16	2000	350.0	350.0	43.0

TUBE

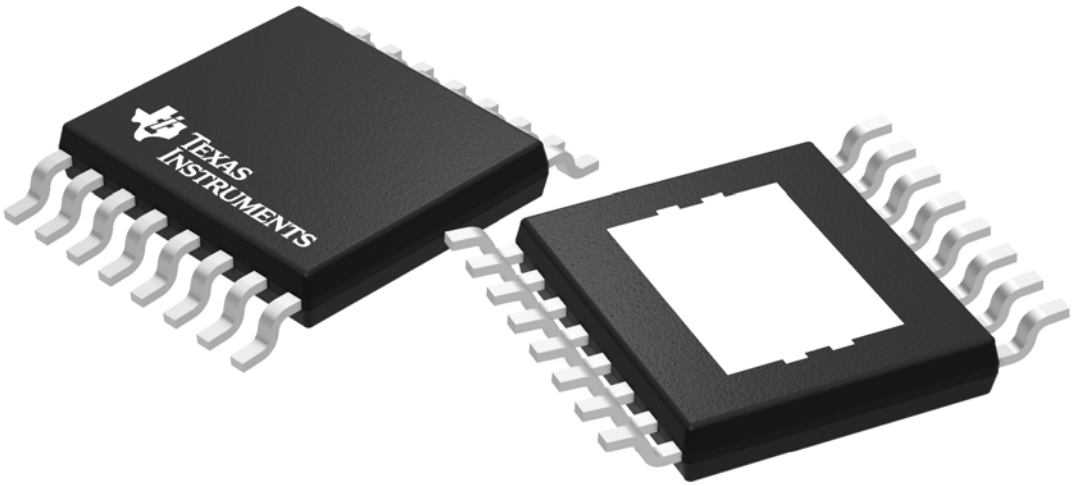


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS40021MPWPEP	PWP	HTSSOP	16	70	530	10.2	3600	3.5
V62/12601-01XE-T	PWP	HTSSOP	16	70	530	10.2	3600	3.5

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

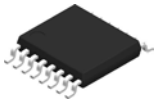
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

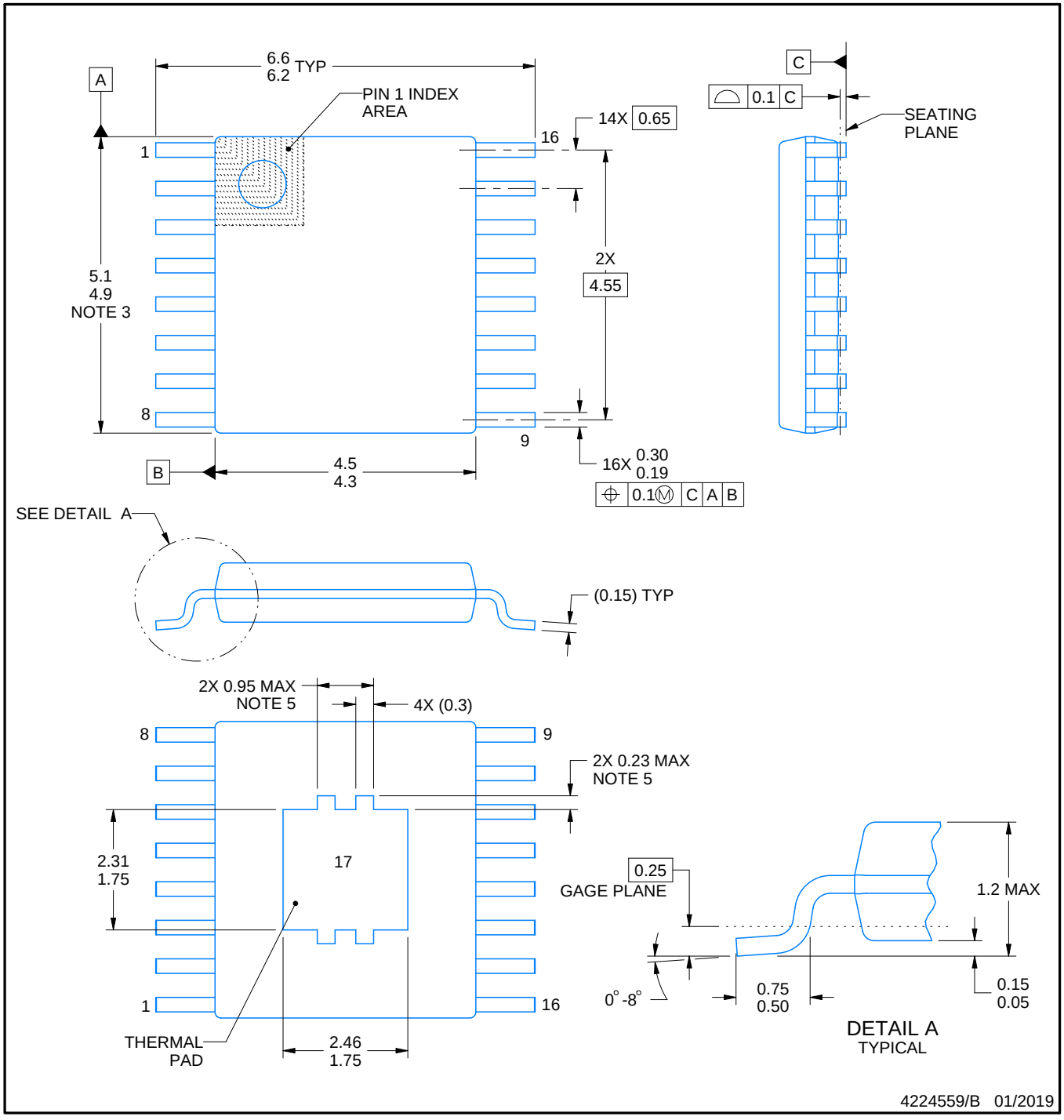
PACKAGE OUTLINE

PWP0016C



PowerPAD™ TSSOP - 1.2 mm max height

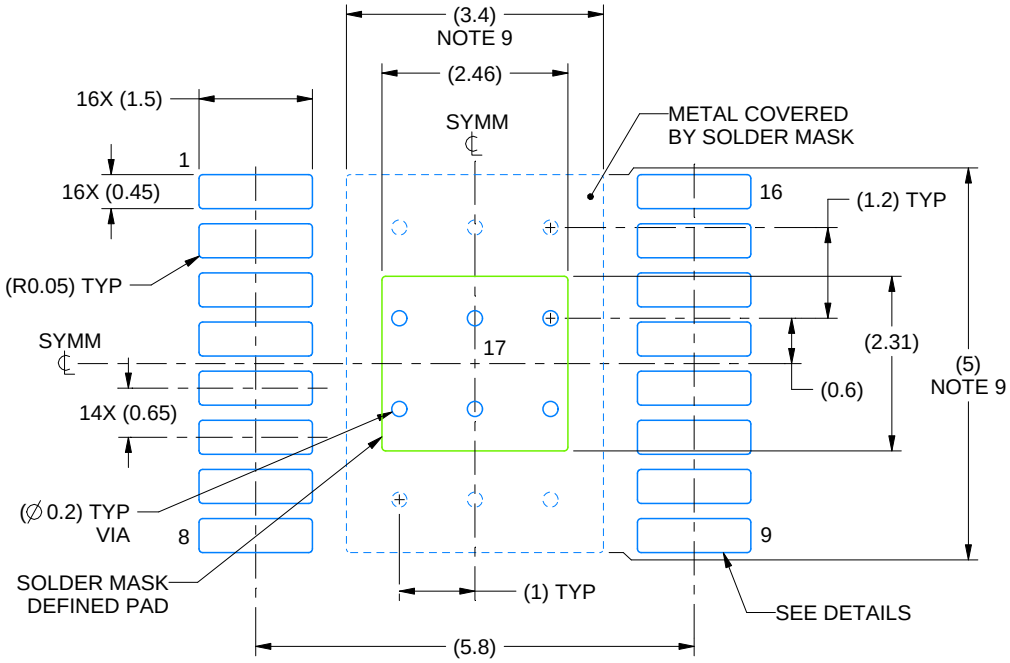
SMALL OUTLINE PACKAGE



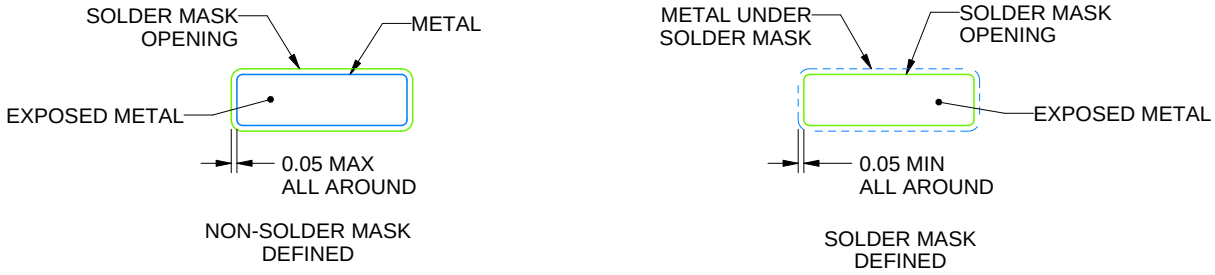
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

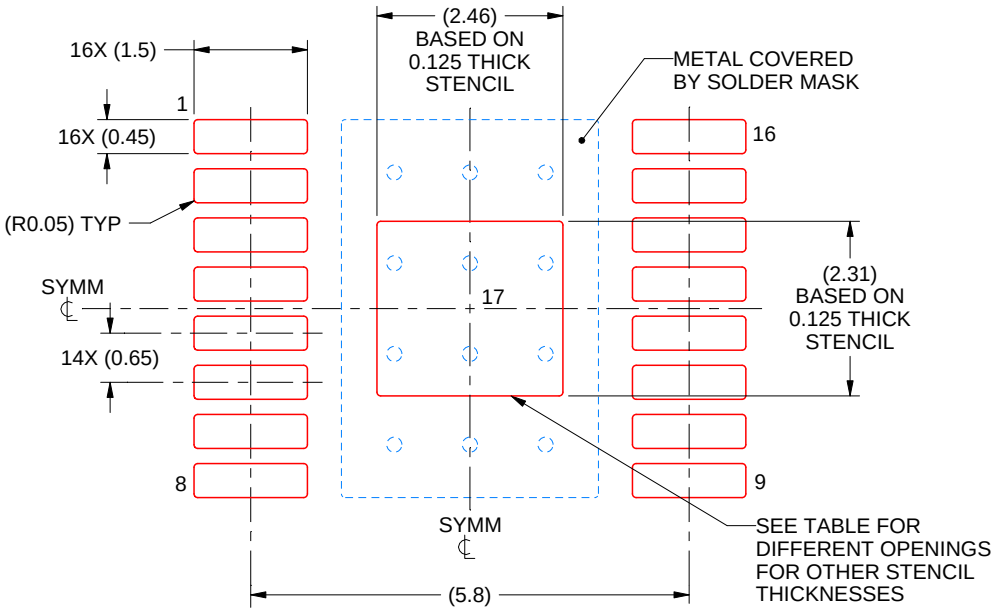


SOLDER MASK DETAILS

4224559/B 01/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 2.58
0.125	2.46 X 2.31 (SHOWN)
0.15	2.25 X 2.11
0.175	2.08 X 1.95

4224559/B 01/2019

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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