Application Report
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TI Space Rated Power Solution for Microsemi® RTG4™ FPGA

Zak Kaye
Javier Valle

ABSTRACT

As aerospace technology continues to develop, the industry has seen a dramatic increase in the lifetime of satellites. With this increase, the operational lifetime of many satellites now surpasses that of the telecom standards they were developed around. Because of this, the need for re-programmability in space applications has also risen [1]. Microsemi® is one company that addresses this need with their SRAM based FPGA, the RTG4™. Modern FPGAs tend to operate at lower voltages and higher currents than their predecessors, and the RTG4 is no exception. FPGA power supply requirements have become more demanding and features such as soft-start and sequencing are required to avoid large inrush currents that could potentially create problems in the regulators upstream. This report demonstrates how TI's space qualified power portfolio can be used to power RTG4 based designs.

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1 RTG4 Electrical Specifications

All specifications for the RTG4 are taken from Microsemi datasheet (Rev. 4) and application reports [2].

Table 1. RTG4 Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Units
VDD	DC FPGA core supply voltage. Must always power this pin.	1.14	1.2	1.26	V
VPP	Power supply for charge pumps (for normal operation and programming). Must always power this pin.	3.15	3.3	3.45	V
VDDPLL	Power for eight corner PLLs, PLLs in SERDES PCIe/PCS blocks, and FDDR PLL.	3.15	3.3	3.45	V
SERDES_x_Lyz_VDDAIO	Tx/Rx analog I/O voltage. Low voltage power for lane-y and Lane-z of SERDES_x. It is a +1.2-V SERDES PMA supply.	1.14	1.2	1.26	V
SERDES_x_Lyz_VDDAPLL	Analog power for SERDES_x PLL lanes yz. It is a +2.5-V SERDES internal PLL supply.	2.375	2.5	2.625	V
SERDES_VDDI	Power for SERDES reference clock receiver 1.8-V supply. Must always power this pin.	1.71	1.8	1.89	V
	Power for SERDES reference clock receiver 2.5-V supply. Must always power this pin.	2.375	2.5	2.625	
	Power for SERDES reference clock receiver 3.3-V supply. Must always power this pin.	3.15	3.3	3.45	
SERDES_VREF	Reference voltage for SERDES receiver reference clocks.	0.49 × SERDES_VDDI	0.5 × SERDES_VDDI	0.51 × SERDES_VDDI	V

Table 1. RTG4 Electrical Specifications (continued)

Symbol	Parameter	Min	Typ	Max	Units
VDDIx	1.2-V DC supply voltage for FPGA I/O banks.	1.14	1.2	1.26	V
	1.5-V DC supply voltage for FPGA I/O banks.	1.425	1.5	1.575	
	1.8-V DC supply voltage for FPGA and JTAG I/O banks.	1.71	1.8	1.89	
	2.5-V DC supply voltage for FPGA and JTAG I/O banks.	2.375	2.5	2.625	
	3.3-V DC supply voltage for FPGA and JTAG I/O banks.	3.15	3.3	3.45	
	DC supply voltage for LVDS25 differential I/O banks.	2.375	2.5	2.625	
	DC supply voltage for LVDS33 differential I/O banks.	3.15	3.3	3.45	
	DC supply voltage for BLVDS, MLVDS, Mini-LVDS, RSDS differential I/O banks.	2.375	2.5	2.625	
	DC supply voltage for LVPECL differential I/O banks.	3.15	3.3	3.45	

2 RTG4 Power-Up and Power-Down Requirements

The power-up requirements are based on the VDDPLL and the SERDES_x_Lyz_VDDAIO voltage rails. The only way to not have any power-up sequencing requirements are to hold the RTG4 in reset (by asserting DEVRST_N) until the VDDPLL supply reaches its minimum recommended level and to have the SERDES_x_Lyz_VDDAIO supplies tied to VDD. If this cannot be done however, then the RTG4 voltage rails need to be properly sequenced. In this case, the following requirements apply:

1. VDDPLL must not be the last supply to ramp up and must reach its minimum recommended level before the last supply (VDD or VDDIx) starts ramping up.
2. VDD core and SERDES IO must be powered up in parallel.

There is no power-down requirement if an external 1-kΩ pull-down resistor is used for each critical output that cannot tolerate an output glitch during power-down or DEVRST_N assertion.

Microsemi has a development kit intended to demonstrate the capabilities of the RTG4 and expedite software development. The power distribution for this development board is shown in Figure 1. In this design, Microsemi uses a reset supervisor that holds the FPGA in reset for approximately 150 ms after the 3.3-V, 10-A regulator comes up. This allows sufficient time for all rails to reach regulation before the device begins operation bypassing the need for a power-up sequence. The oscilloscope plot in Figure 2 shows the main rails on startup while the device is held in reset. All of the voltage rails come up at the same time and reach their recommended operating points before the reset supervisor releases the active low reset.

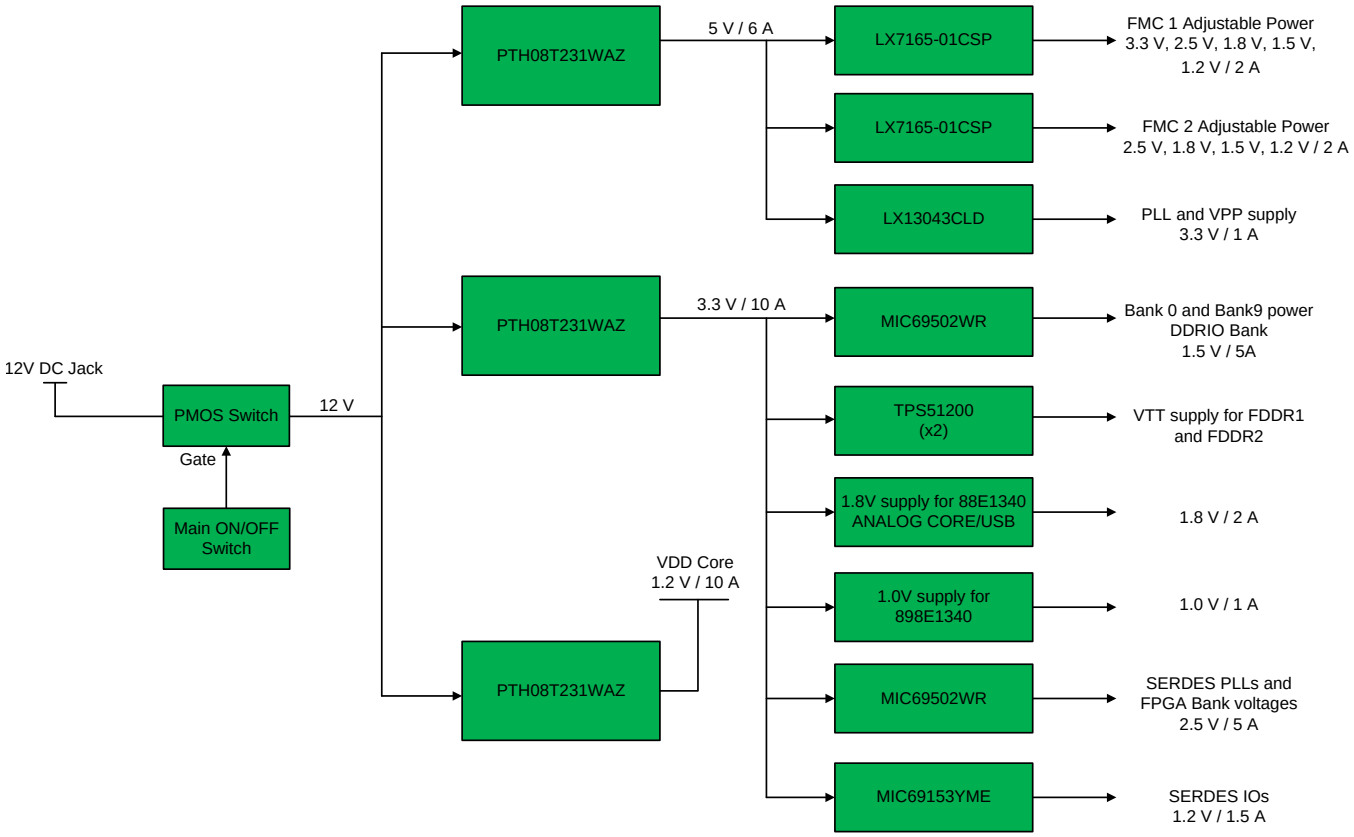

Figure 1. RTG4 Development Board Power Distribution

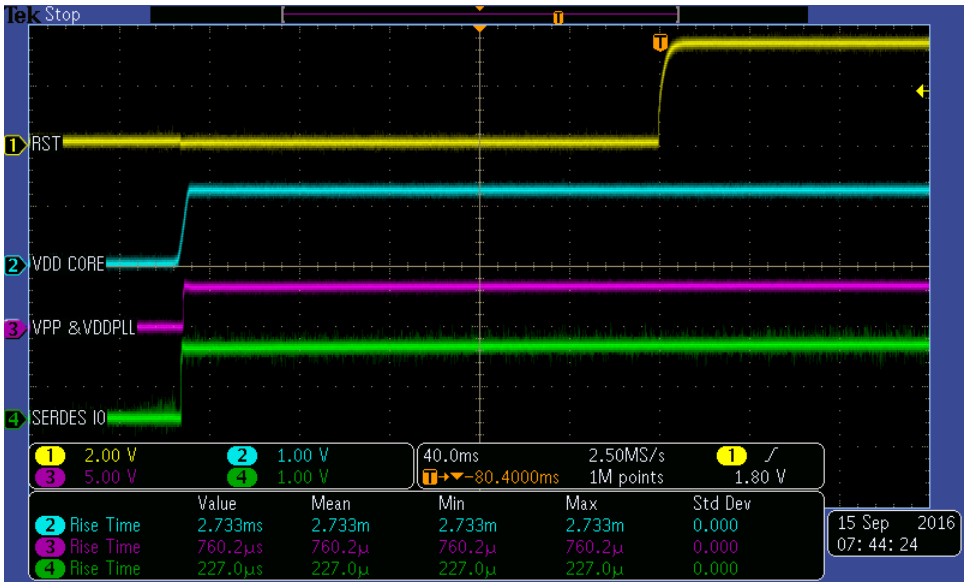

Figure 2. RTG4 Development Board Start-up Sequence

3 Demonstrating Space Rated TI Solutions

3.1 Setup

To demonstrate the applicability of TI's space portfolio to this design, an RTG4 development kit was modified such that the voltage rails associated with power-up requirements were replaced with Evaluation Modules (EVM) ofour space qualified power devices (TPS50601SPEVM-S, TPS50601SPEVM-D and TPS7H1101SPEVM). To demonstrate successful functionality under heavy load, the RTG4 was flashed with a high current design that resulted in a core current consumption of approximately 5 A at 1.2 V. The test setup can be seen in Figure 3.

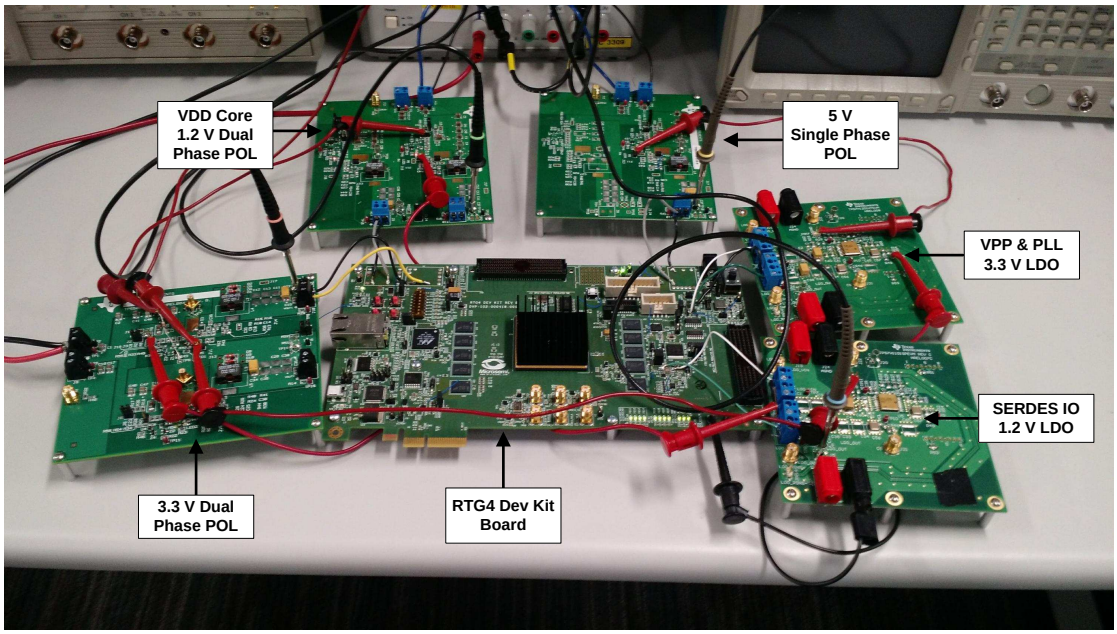

Figure 3. RTG4 Modified Development Board Connected to TI Evaluation Modules

The reset supervisor on the development board was then removed and the voltage rails were sequenced using the power good and enable pins of each device as shown in Figure 5. The 12-V input source to the development board was changed to a 6-V source to satisfy the input requirements of the TI space power devices. The power tree for the modified development board is shown in Figure 4. The new components are shown in orange.

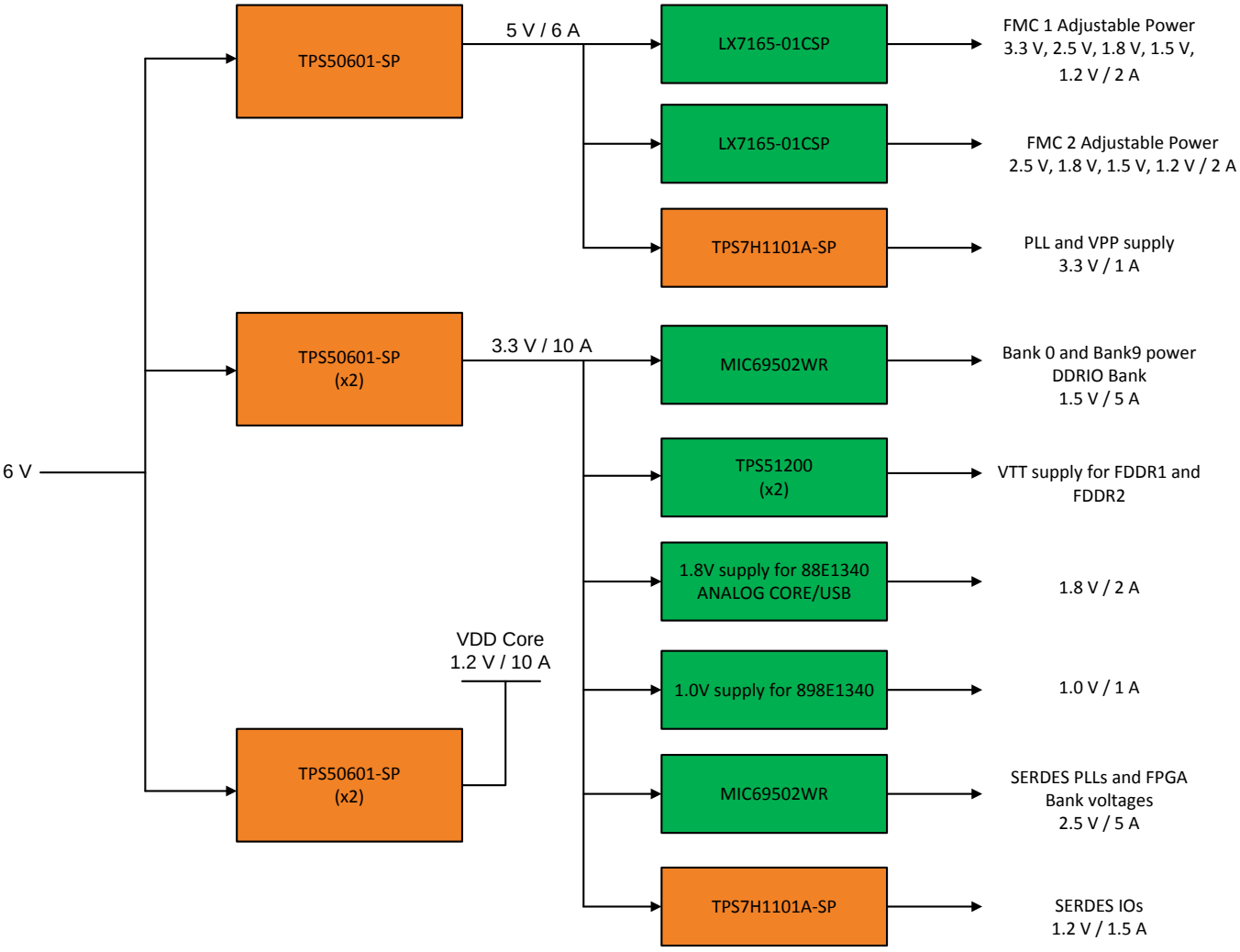

Figure 4. RTG4 Modified Development Board Power Distribution Using TI Space Qualified Components

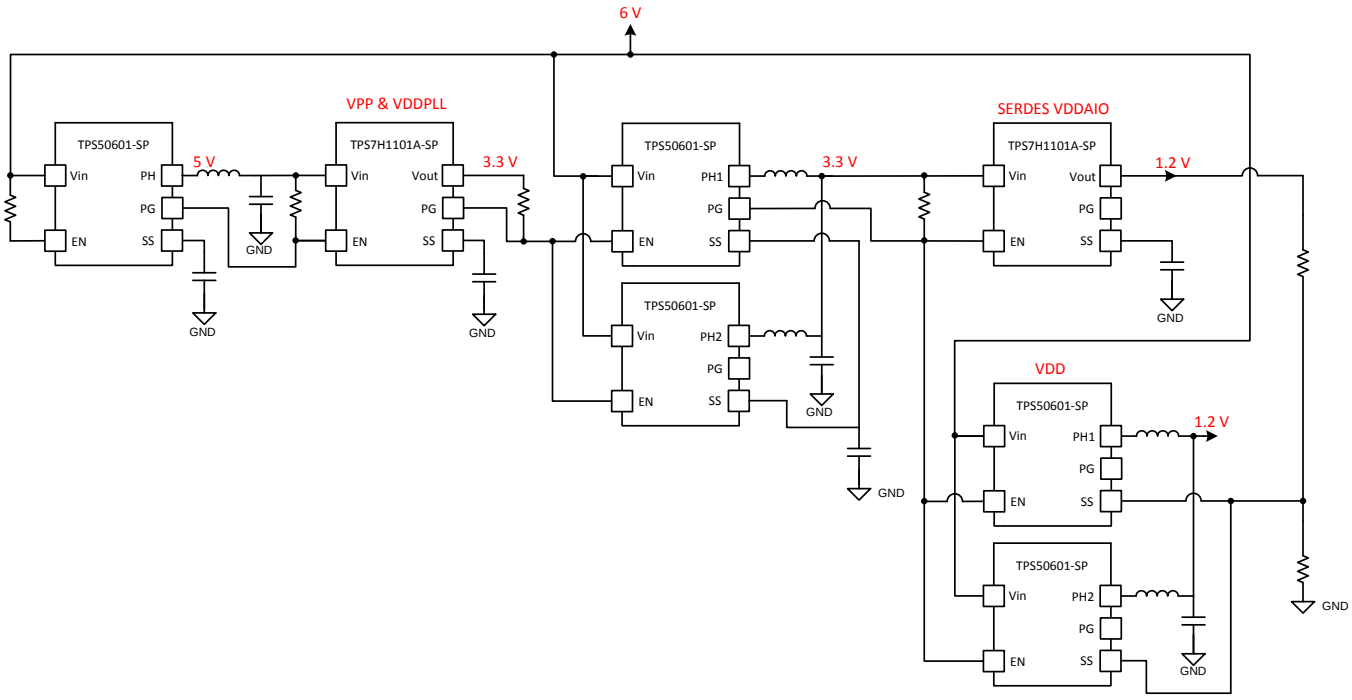

Figure 5. RTG4 Modified Development Board Power Sequence

The rise times of all devices were configured to be at least 1 ms to avoid inrush currents. The core rail, VDD, is ratiometrically sequenced with the SERDES IO rail to ensure both voltage rails rise at the same time as required by the RTG4.

3.2 Results

The oscilloscope plots in Figure 6 and Figure 7 show the start-up behavior of each of these voltage rails while connected to the RTG4 development kit fulfilling the 2 requirements discussed in Section 2.

Figure 6. RTG4 Modified Development Board Fulfilling the First Power-Up Requirement

Figure 7. RTG4 Modified Development Board Fulfilling the Second Power-Up Requirement

As shown in Figure 6 and Figure 7, both power sequencing requirements have been met and a clean monotonic power-up behavior is observed. Once the voltage rails come up, the RTG4 begins executing its software and the core starts to draw approximately 5-A of current. The software is the SERDES EPCS demo software (DG0624) provided by Microsemi.

3.3 Suggested Grounds-Up Implementation

The solution presented in Figure 3, Figure 4 and Figure 5 was based on modifications to the RTG4 development board. In a new RTG4 design, TI recommends a power distribution as the one shown in Figure 8. In this case, an isolated DC-DC converter using TI's portfolio of UC18xx-SP controllers is used to generate the 5-V input voltage to the switching and linear point of load regulators. The recommended power-up sequence for this power distribution is shown in Figure 9. Since the RTG4 supports DDR memories, a DDR termination regulator will be needed as part of the power distribution as shown in Figure 1. For such device, the TPS7H3301-SP has been included in this grounds-up recommended power distribution. The TPS7H3301-SP is TI's radiation hardened double data rate (DDR) 3-A termination regulator that supports all standard DDR memory configurations and incorporates a built-in reference voltage buffer, eliminating the need for an additional supply to produce the DDR reference. In addition, as it is a linear device, it provides significant area savings and simplicity when compared to switching devices that require inductor and more components for the device to operate. For more information, please refer to the TPS7H3301-SP product page. Notice the 1.5-V input voltage to the TPS7H3301-SP shown in Figure 8 is the high current supply providing the output current for the DDR termination voltage.

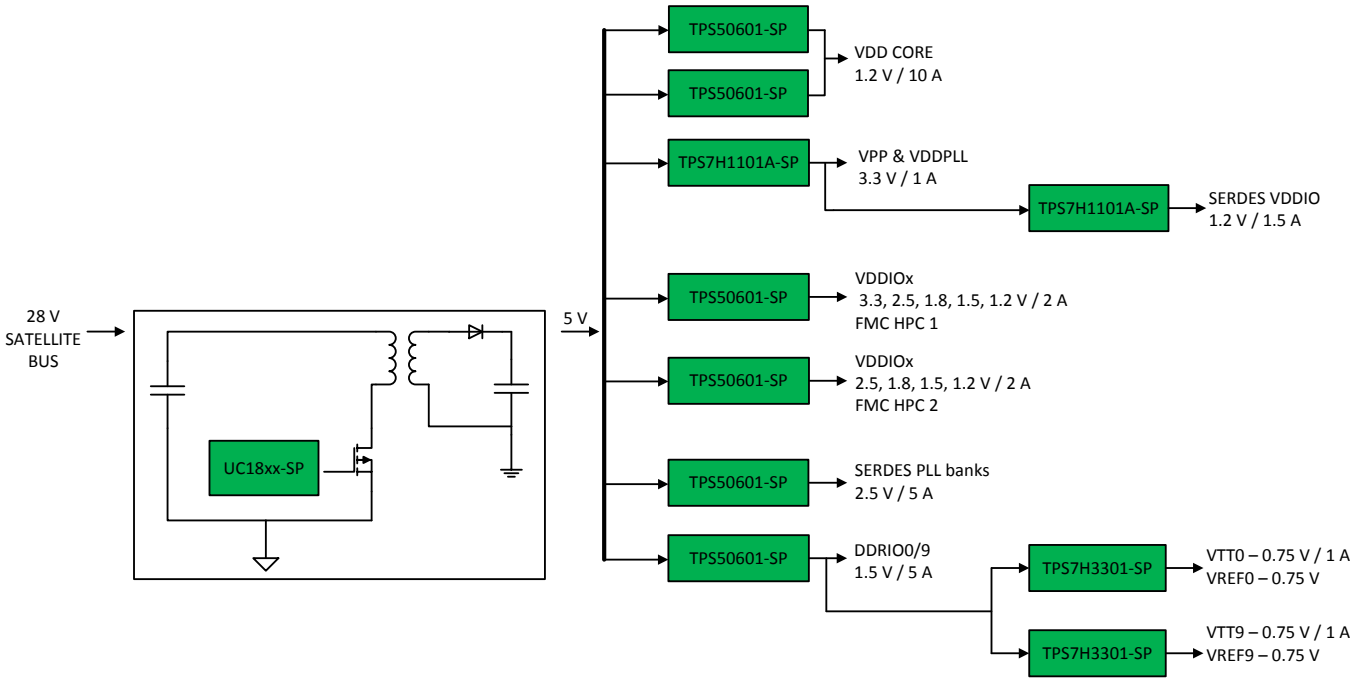

Figure 8. Recommended Grounds-Up RTG4 Power Distribution

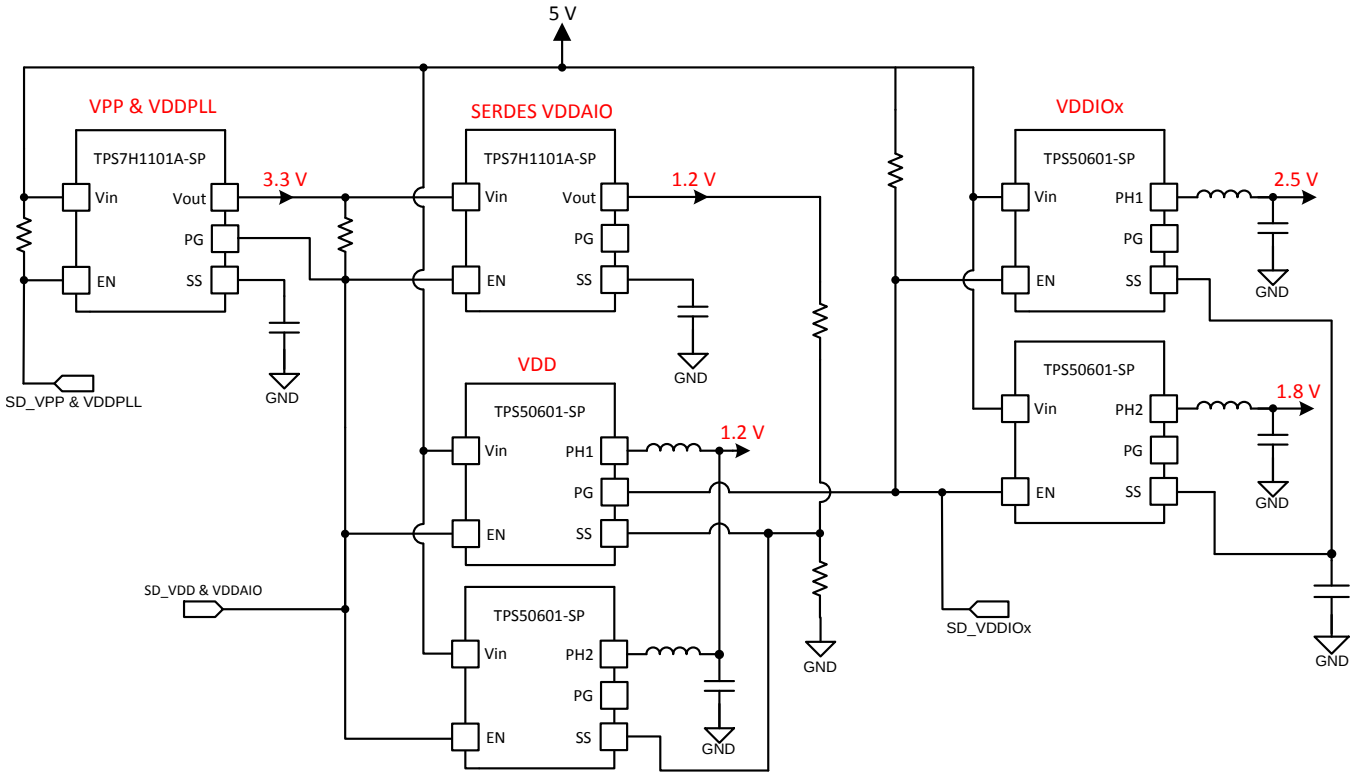

Figure 9. Recommended Grounds-Up RTG4 Power-Up Sequencing. The SD_Vxx Signals Can Be Used for Power-Down Sequences as Needed.

This implementation ensures all power-up sequencing requirements are met as well as providing board area savings as TI offers the smallest, thermally enhanced radiation hardened DC-DC converter and LDO packages in the industry (TPS7H1101A-SP: 11.00 mm × 9.60 mm, TPS50601-SP: 12.70 mm × 7.38 mm).

4 Conclusion

The TPS50601-SP, TPS7H1101A-SP and TPS7H3301-SP are TI's flagship radiation tolerant power devices with features such as soft-start, power good, and tracking that make them particularly well suited for powering modern FPGA applications. This report has demonstrated how to implement these features with the RTG4 to achieve successful operation. Similar configurations can also be applied to other FPGAs to satisfy their specific power requirements.

5 References

(1) A. Fernandez-Leon, A. Pouponnot, S. Habinc. "The Use of Reprogrammable FPGAs in Space", European Space Agency. 29 April 2014. http://www.esa.int/Our_Activities/Space_Engineering_Technology/Microelectronics/The_use_of_reprogrammable_FPGAs_in_space

(2) Microsemi Documentation:

a. UG0617: RTG4 FPGA Development Kit User Guide
b. DS0131: RTG4 FPGA Datasheet
c. AC439: Board Design Guidelines for RTG4 FPGA Application Note
d. RTG4 Power Estimator

6 Additional Resources

- TPS50601-SP Datasheet (SLVSD45)
- TPS7H1101-SP Datasheet (SLVSD81)
- Advanced Topics in Powering FPGAs (SNVA592)
- Power Supply Design Considerations for Modern FPGAs (SNOA864)

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