Application Report
SLVAEO1–April 2020

TPS50601A-SP Small Form Factor Buck Converter

Daniel Hartung

ABSTRACT

The TPS50601A-SP is one of the smallest space-grade buck converters for point-of-load applications. With special attention to the form factor during layout, the overall system design can be made quite small. This application report summarizes a design using the TPS50601A-SP that adheres to a form factor of 25 mm × 27 mm.

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

The TPS50601A-SP small form factor buck converter is a 5-V to 0.95-V buck converter that adheres to creating the smallest form factor possible while still maintaining electrical performance. The circuit is optimized for providing up to 6 A of current in less than 7 cm^2 of area. This document explains the justification for the values chosen as well as waveforms of basic operation.

2 Design Values

Table 1. Design Parameters

Parameter	Design Value
Output Voltage	0.95 V
Input Voltage	5 V
Output Current	6 A
Switching Frequency	500 kHz
Inductor Current Ripple	10%
Output Voltage Ripple	10 mV
Transient Overshoot and Undershoot	40 mV
Soft-Start Time	4 ms
Crossover Frequency	20 kHz
Gain Margin	Approximately –20 dB
Phase Margin	Approximately 50°

The following subsections go through the process of calculating components based on the design specifications in Table 1. All equations are taken from the *TPS50601A-SP Radiation Hardened 3-V to 7-V Input, 6-A Synchronous Buck Converter Data Sheet*.

2.1 Switching Frequency

A 500-kHz switching frequency was selected to ensure the design could be used for master slave mode for the TPS50601A-SP. Using Equation 1 a resistor for pin RT can be found to set the desired frequency.

$$RT(F_{SW}) = 67009 \times F_{SW}^{-1.0549} \quad (1)$$

$$RT(F_{SW}) = 67009 \times (500)^{-1.0549} = 95.3 \ k\Omega$$

A 95.3-kΩ resistor was used in the final design.

2.2 Output Voltage

Using a starting value of 10.1 kΩ for the top resistor of the resistor divider, the bottom resistor can be calculated using Equation 2 to set the correct output voltage.

$$R_{BOTTOM} = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_{TOP} \quad (2)$$

$$R_{BOTTOM} = \frac{0.804 \ V}{0.95 \ V - 0.804 \ V} \times 10.1 \ k\Omega = 55.6 \ k\Omega$$

A 55.6-kΩ resistor was used in the final design.

2.3 Inductor Current Ripple

The inductor current ripple will affect how large the output voltage ripple of the design will be. An increase in the inductor current ripple will lead to a corresponding increase in the output voltage ripple. If too little ripple is allowed in a design, the inductor values may be unobtainable which can cause problems with procurement. A 10% inductor current ripple was picked for this design as a trade off between the two factors. Equation 3 shows how to calculate the proper inductor value for this level of inductor ripple current.

$$L = \frac{V_{INMAX} - V_{OUT}}{I_o \times K_L} \times \frac{V_{OUT}}{V_{INMAX} \times f_{SW}} \tag{3}$$

$$L = \frac{5\ V - 0.95\ V}{6\ A \times 0.1} \times \frac{0.95\ V}{5 \times 500\ kHz} = 2.57\ \mu H$$

A value of 2.2 µH was used for the calculated number in the design.

The value in the design as close to the calculated number was 22 µH.

2.4 Output Capacitance

There are two parameters to consider when choosing output capacitance, allowable overshoot and undershoot during transients and contribution to output voltage ripple. An output capacitance must be chosen that is higher than the values calculated in Equation 4 and Equation 5.

$$C_{OUT} \geq \frac{2 \times I_O}{f_{SW} \times \Delta V_{OUT}} \tag{4}$$

$$C_{OUT} \geq \frac{2 \times 6\ A}{500\ kHz \times 40\ mV} = 600\ \mu F$$

$$C_{OUT} \geq \frac{I_{ripple}}{8 \times f_{SW} \times V_{OUTripple}} \tag{5}$$

$$C_{OUT} \geq \frac{0.6\ A}{8 \times 500\ kHz \times 10\ mV} = 15\ \mu F$$

An output capacitance of 660 µF was used as an appropriate amount based on calculations and part availability.

The maximum ESR of the chosen output capacitors must also be calculated to adhere to the maximum output voltage ripple. An ESR of less than the value calculated in Equation 6 must be chosen.

$$R_{ESR} \leq \frac{V_{OUTripple}}{I_{ripple}} \tag{6}$$

$$R_{ESR} \leq \frac{10\ mV}{0.6\ A} = 16.7\ m\Omega$$

The ESR value chosen is 5 mΩ which is much smaller than the calculated resistance.

2.5 Compensation

Starting values for the compensation of the design can be calculated, but based on measurements and optimizations often final design values will change. The starting values can be calculated using Equation 7, Equation 8, and Equation 9.

$$R_{COMP} = \frac{2\pi \times f_{CO} \times V_{OUT} \times C_{OUT}}{gm_{EA} \times V_{REF} \times gm_{PS}} \tag{7}$$

$$R_{COMP} = \frac{2\pi \times 20\ kHz \times 5\ V \times 660\ \mu F}{1400\ \mu s \times 0.804\ V \times 22\ s} = 16.7\ k\Omega$$

$$C_{COMP} = \frac{C_{OUT} \times \frac{V_{OUT}}{I_{OUT}}}{R_{COMP}} \tag{8}$$

$$C_{COMP} = \frac{660\ \mu F \times \frac{0.95\ V}{6\ A}}{16.7\ k\Omega} = 6.3\ nF$$

$$C_{HF} = \frac{C_{OUT} \times R_{ESR}}{R_{COMP}} \tag{9}$$

$$C_{HF} = \frac{660\ \mu F \times 5\ m\Omega}{16.7\ k\Omega} = 198\ pF$$

Final design values changed slightly based on measurements and part availability to 16.7 kΩ, 6.8 nF, and 10 pF. The largest change was C_{HF} decreasing as the purpose of the capacitor is to cancel the ESR zero caused by the buck topology. It was determined that the ESR zero was sufficiently canceled out by the poles caused by the switching frequency and the gain margin was enough for the design. Since a small capacitor is recommended to help with high-frequency noise on that node, a small 10-pF capacitor was added.

2.6 Soft-Start Capacitor

The soft-start capacitor needed to allow for the appropriate soft-start time can be calculated using Equation 10.

$$C_{ss} = \frac{t_{ss} \times I_{SS}}{V_{REF}}$$
$$C_{ss} = \frac{4\ ms \times 2\ \mu A}{0.805\ V} = 9.94\ \ nF \quad (10)$$

A capacitor of 10 nF was used based on being a close value to the calculated capacitance.

3 Results

The results obtained during testing were close to the expected value. Figure 1 shows a block diagram for the overview of the important passives.

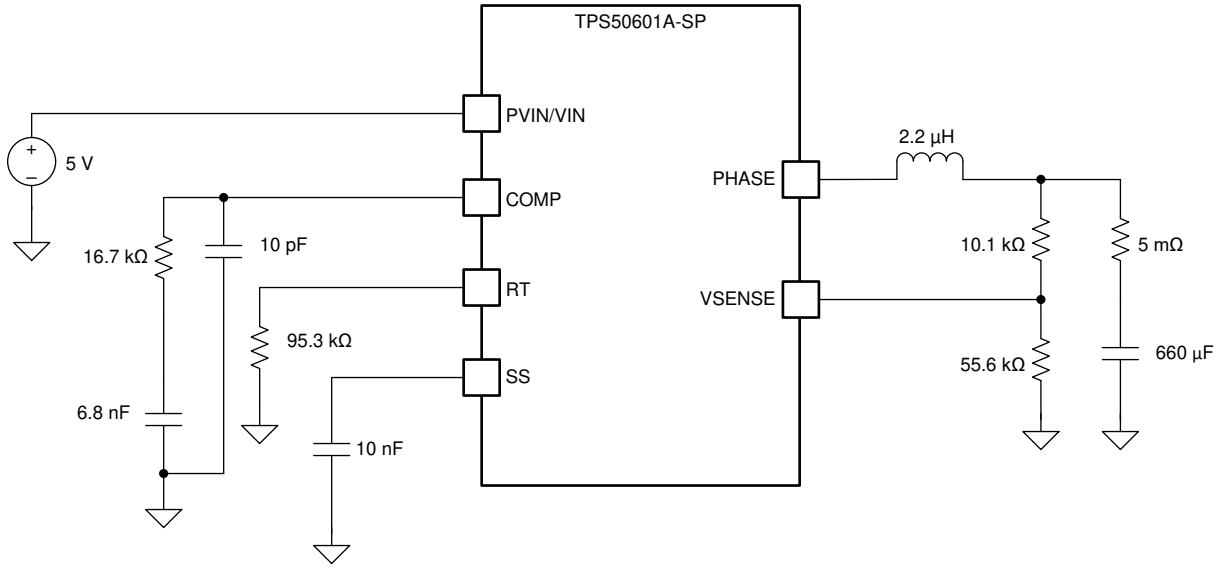

Figure 1. Block Diagram of Circuit

3.1 Phase Node

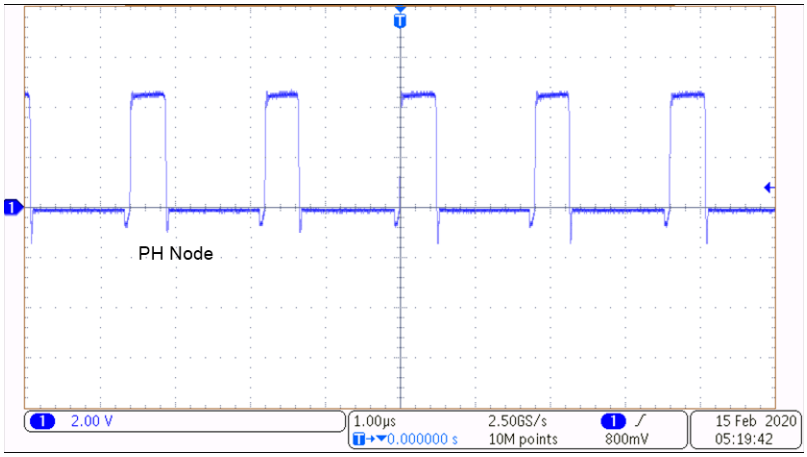

Figure 2. Picture of Phase Node

The test for Figure 2 was taken with 6 A of output current and 5 V on the input.

3.2 Start-up

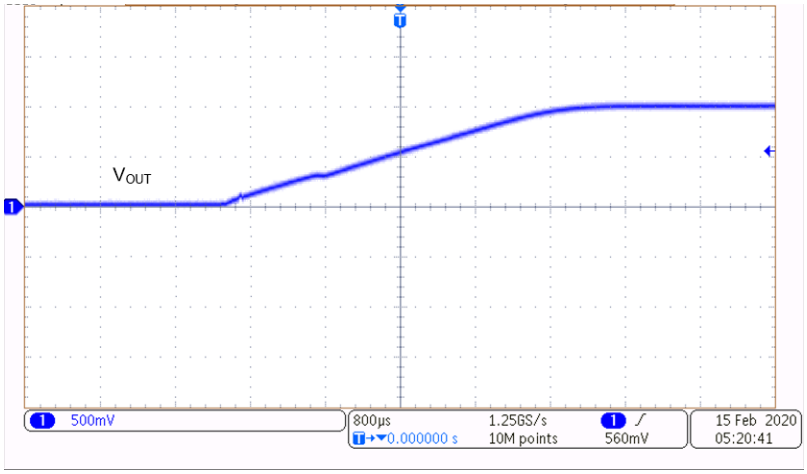

Figure 3. Start-up With Full Load

The test for Figure 3 was taken with 6 A of output current as the input voltage ramped up to 5 V.

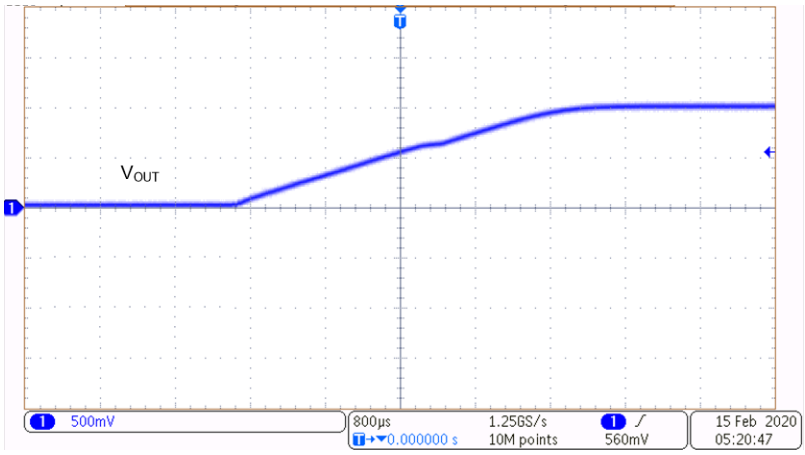

Figure 4. Start-up With No Load

The test for Figure 4 was taken with no output current as the input voltage ramped up to 5 V.

3.3 Shutdown

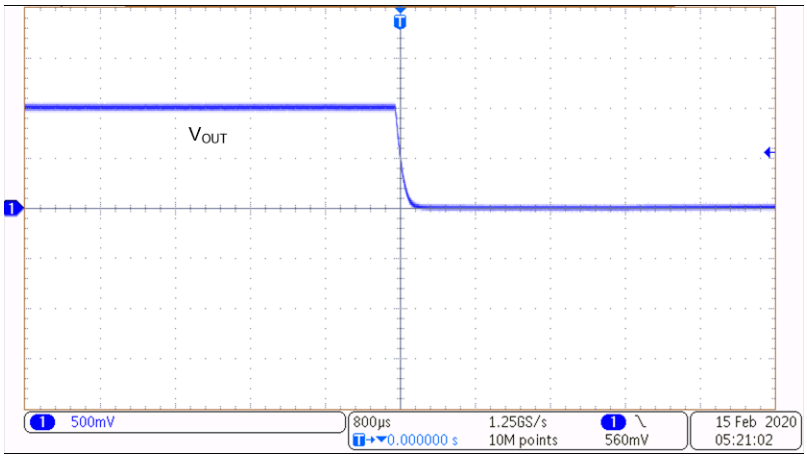

Figure 5. Shutdown With Full Load

The test for Figure 5 was taken with 6 A of output current as the input voltage ramped down from 5 V to 0 V.

3.4 Frequency Response

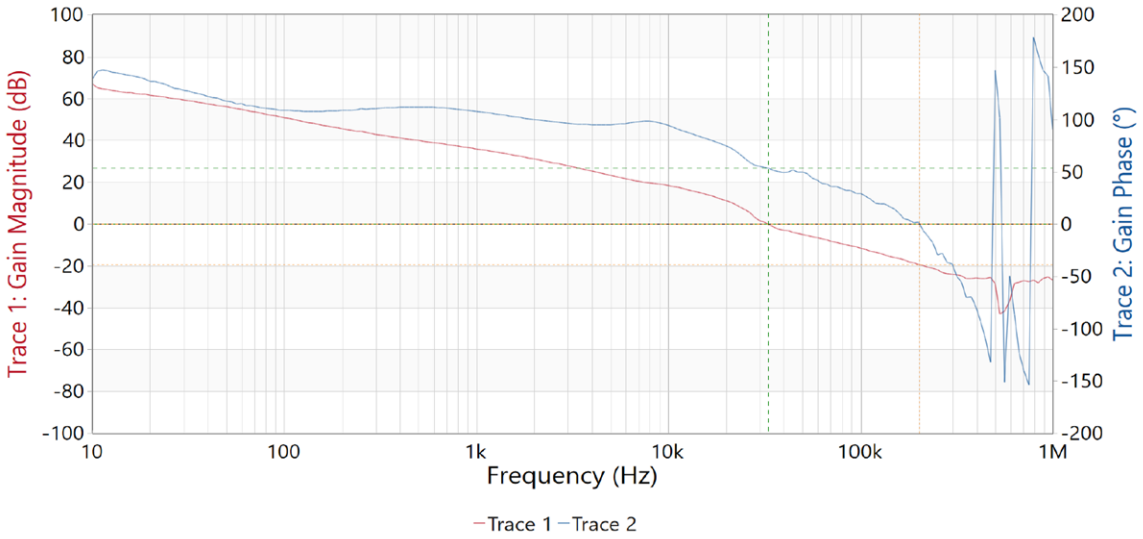

Figure 6. Frequency Response of Circuit

The test for Figure 6 was taken with 6 A of output current and 5 V on the input.

Table 2. Relevant Measured Parameters From Figure 6

Parameter	Value
Phase Margin	53.56°
Crossover Frequency	33.24 kHz
Gain Margin	–19.43
Gain Crossover	202.2 kHz

3.5 Transient Performance

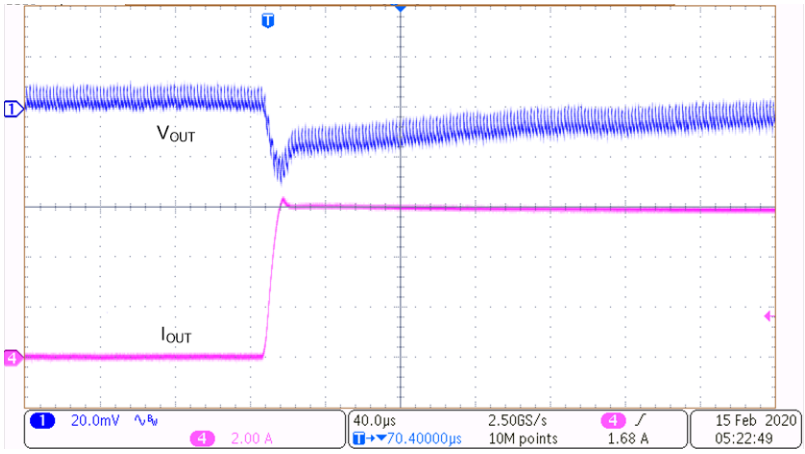

Figure 7. Step Up Transient

The test for Figure 7 was taken with a step from 0 A to 6 A of output current with 5 Volts on the input. There is approximately 16 mV of undershoot.

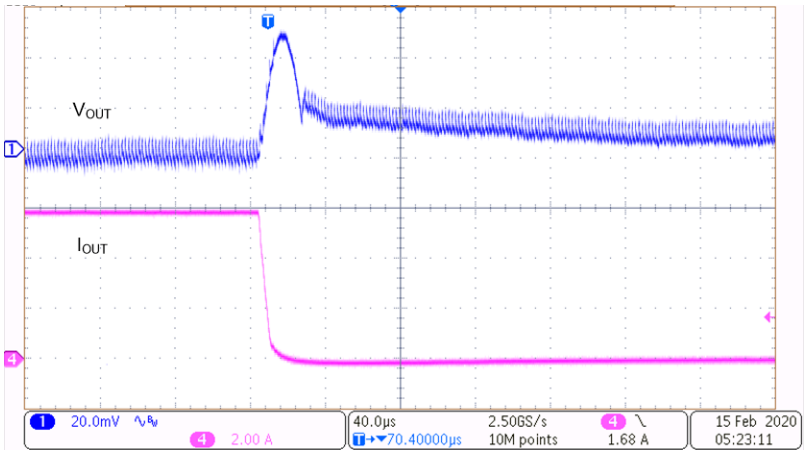

Figure 8. Step Down Transient

The test for Figure 8 was taken with a step from 6 A to 0 A output current with 5 V on the input. There is approximately 26 mV of overshoot.

3.6 Output Voltage Ripple

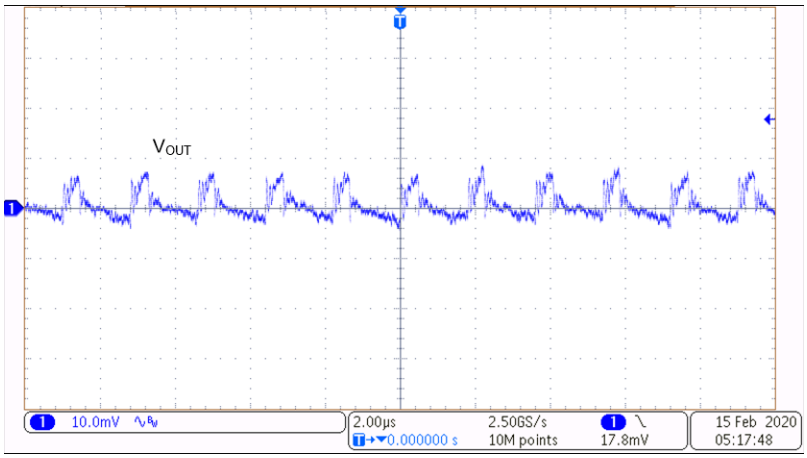

Figure 9. Output Voltage Ripple

The test for Figure 9 was taken with 6 A of output current and Volts on the input. The voltage ripple is approximately 10 mV peak to peak.

4 PCB Layouts

Figure 10 through Figure 13 illustrate the TPS50601A PCB layouts.

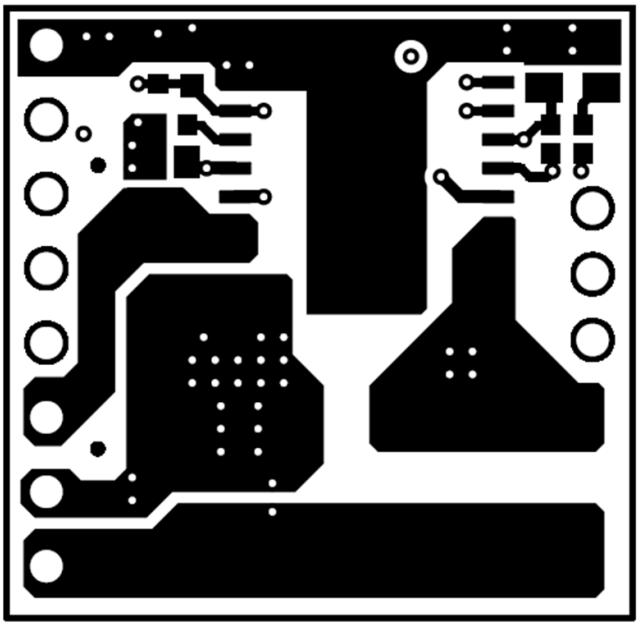

Figure 10. TPS50601A PCB Top Layer

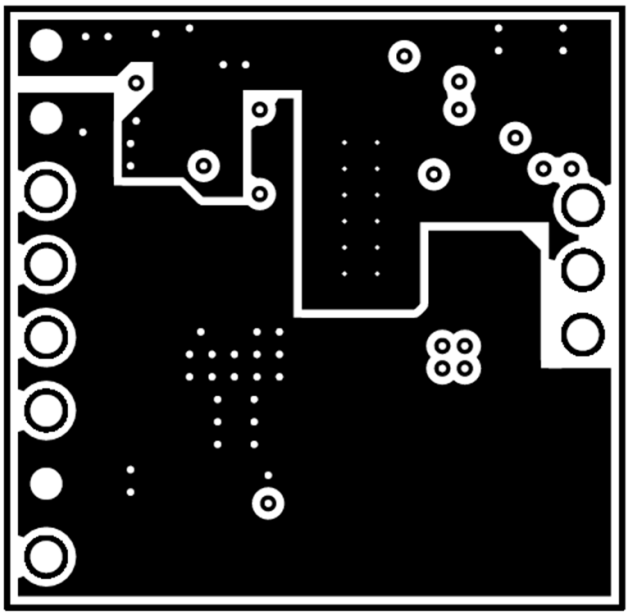

Figure 11. TPS50601A PCB Layer 2

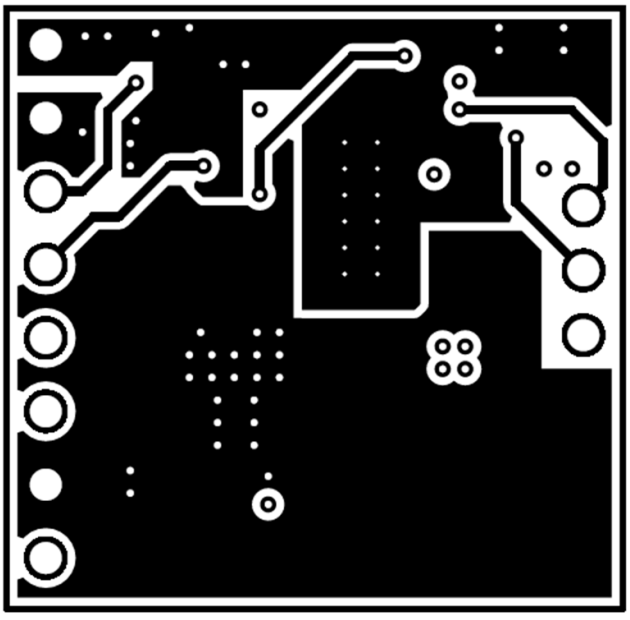

Figure 12. TPS50601A PCB Layer 3

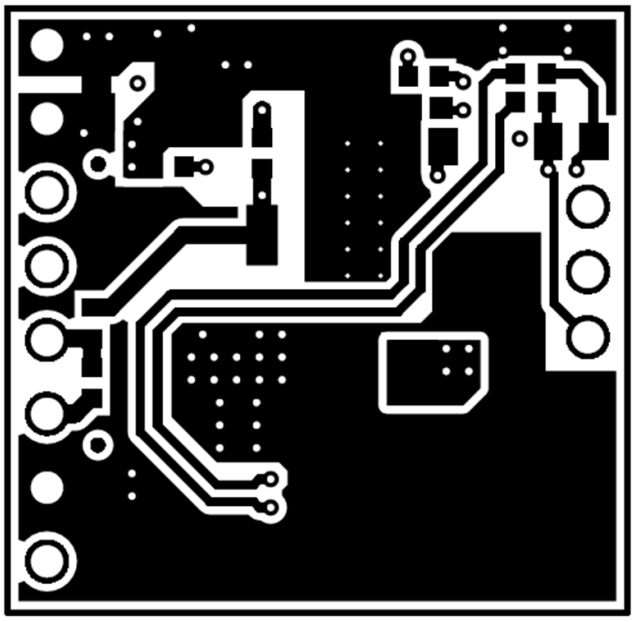

Figure 13. TPS50601A PCB Bottom Layer

5 Schematic

Figure 14 illustrates the TPS50601AHKH schematic.

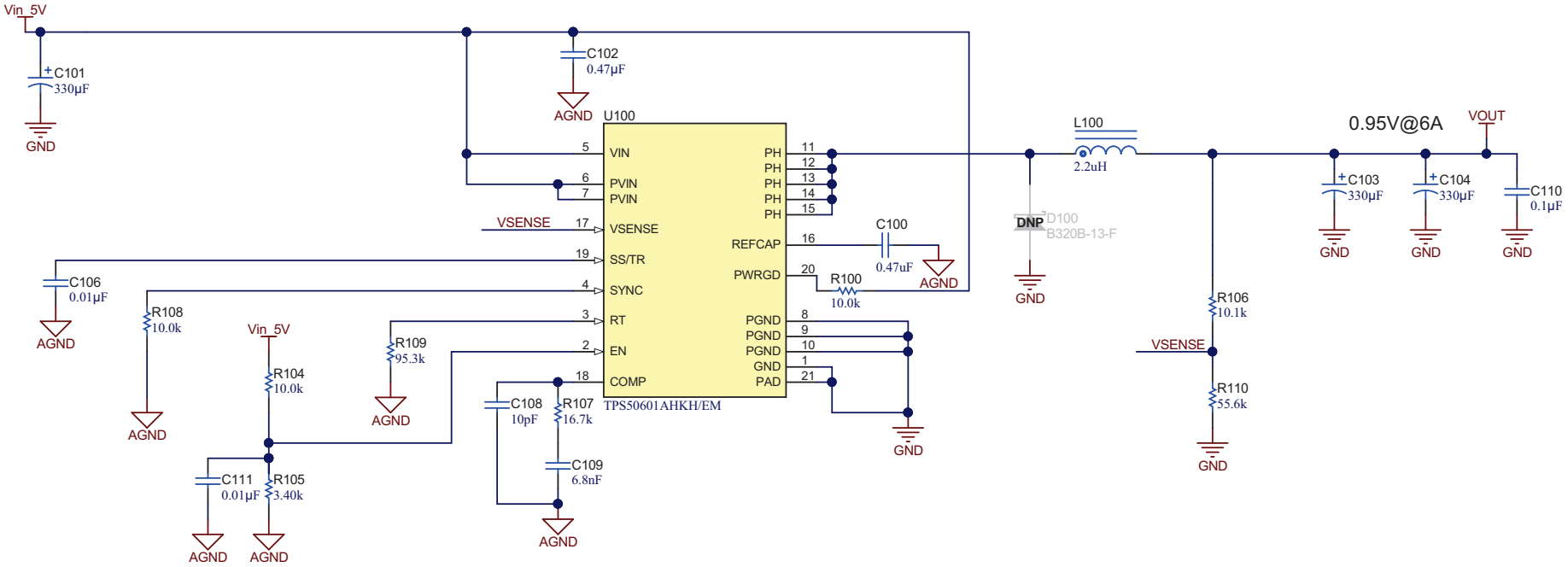

Figure 14. TPS50601A Revision E1 Schematic

6 Bill of Materials

Table 3 details the TPS50601AE1 schematic.

Table 3. TPS50601A Revision E1 Bill of Materials

Item #	Designator	QTY	Value	Part Number	Manufacturer	Description	Package Reference
1	C100	1	0.47 µF	GCM21BR71H474KA55L	MuRata	CAP, CERM, 0.47 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 0805	0805
2	C101, C103, C104	3	330 µF	T541X337M010AH6720	Kemet	CAP, Tantalum Polymer, 330 µF, 10 V, ±20%, 7343-43 SMD	7343-43
3	C102	1	0.47 µF	SR1209X7R474K1NT95(F)#M123A	Presidio Components	CAP, CERM, 0.47 µF, 25 V, ±10%, X7R, 1209	1209
4	C106, C111	2	0.01 µF	SR0603X7R103K1NT95(F)#M123A	Presidio Components	CAP, CERM, 0.01 µF, 25 V, ±10%, X7R, 0603	0603
5	C108	1	10 pF	0402N100J500CT	Walsin	CAP, CERM, 10 pF, 50 V, ±5%, C0G/NP0, 0402	0402
6	C109	1	6800 pF	C0603C682J5RACTU	Kemet	CAP, CERM, 6800 pF, 50 V, ±5%, X7R, 0603	0603
7	C110	1	0.1 µF	SR0805X7R104K1NT95(F)#M123A	Presidio Components	CAP, CERM, 0.1 µF, 25 V, ±10%, X7R, 0805	0805
8	L100	1	2.2 µH	AE611PYA222MSZ	Coilcraft CPS	Inductor, Composite, 2.2 µH, 18.4 A, 0.0028 Ω, SMD	11.3 × 10 × 10 mm
9	R100, R104, R108	3	10.0 kΩ	M55342K12B10E0T	TT Electronics/IRC	RES, 10.0 kΩ, 1%, 0.1 W, 0603	0603
10	R105	1	3.40 kΩ	M55342K12B3E40T	TT Electronics/IRC	RES, 3.40 kΩ, 1%, 0.1 W, 0603	0603
11	R106	1	10.1 kΩ	M55342E12B10B1T	TT Electronics/IRC	RES, 10.1 kΩ, 0.1%, 0.1 W, 0603	0603
12	R107	1	16.7 kΩ	RT0603DRE0716K7L	Yageo America	RES, 16.7 kΩ, 0.5%, 0.1 W, 0603	0603
13	R109	1	95.3 kΩ	CRCW040295K3FKED	Vishay-Dale	RES, 95.3 kΩ, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
14	R110	1	55.6 kΩ	RT0603DRE0755K6L	Yageo America	RES, 55.6 kΩ, 0.5%, 0.1 W, 0603	0603
15	U100	1		TPS50601AHKH/EM	Texas Instruments	Radiation Hardened 3.0- to 6.3-V Input, 6-A Synchronous Buck Converter, HKH0020A (CFP-20)	HKH0020A
16	D100	0	20 V	B320B-13-F	Diodes Inc.	Diode, Schottky, 20 V, 3 A, SMB	SMB

7 References

1. Texas Instruments, *TPS50601A-SP Radiation Hardened 3-V to 7-V Input, 6-A Synchronous Buck Converter Data Sheet*

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265