User's Guide

TPS53125 Buck Controller Evaluation Module User's Guide

ABSTRACT

The TPS53125EVM-599 evaluation module presents an easy-to-use reference design for a common dual output power supply using the TPS53125 controller in cost-sensitive applications. Also included are the schematic, board layout, and bill of materials.

Table of Contents

Trademarks

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1 Description

The TPS53125EVM-599 evaluation board provides the user with a convenient way to evaluate the TPS53125 dual synchronous step-down controller in a realistic cost-sensitive application. Providing both a low core-type 1.05-V and I/O-type, 1.8-V outputs at up to 4 A from a loosely regulated 12-V (8-V to 22-V) source, the TPS53125EVM-599 includes switches and test points to assist users in evaluating the performance of the TPS53125 controller in their applications.

1.1 Applications

- Digital television
- Set-top box
- DSL and cable modems
- Cost-sensitive digital consumer products

1.2 Features

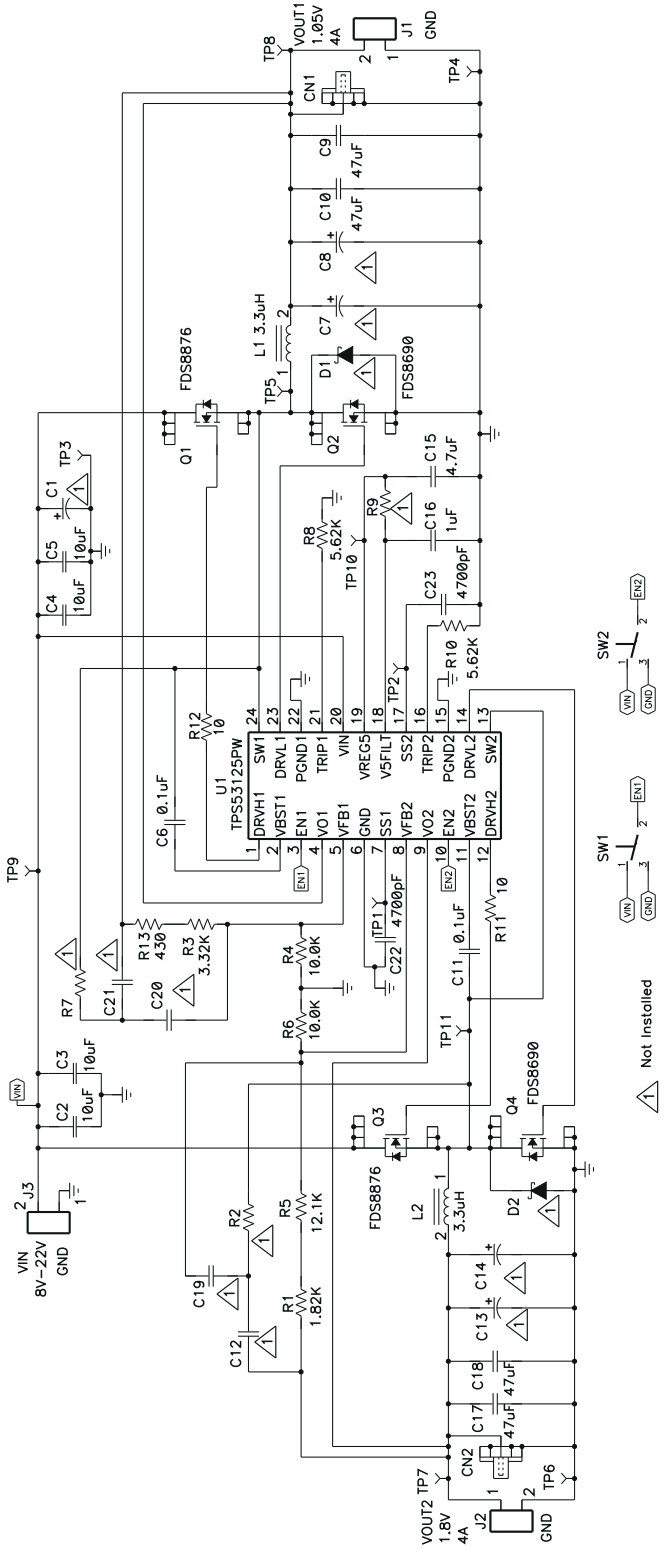
- 8-V to 22-V input
- 1.05-V and 1.8-V outputs
- Up to 4 A per channel output
- 350-kHz pseudo-fixed frequency D-CAP2™ mode control
- Independent enable switches for power-on/power-off testing

2 TPS53125EVM-599 Electrical Performance Specifications

Table 2-1. TPS53125EVM-599 Electrical and Performance Specifications

Parameter		Notes and Conditions	Min	Typ	Max	Unit
Input Characteristics						
V_{IN}	Input Voltage		8	12	22	V
I_{IN}	Input Current	V_{IN} = 12 V, I_{OUT1} = 4 A, I_{OUT2} = 4 A	–	1.2	1.5	A
	No Load Input Current	V_{IN} = 12 V, I_{OUT} = 0 A	–	20	35	mA
V_{IN_UVLO}	Input UVLO	I_{OUT} = 4	4.0	4.2	4.5	V
Output Characteristics						
V_{OUT1}	Output Voltage 1	V_{IN} = 12 V, I_{OUT} = 2 A	1.03	1.05	1.07	V
	Line Regulation	V_{IN} = 8 to 22	–	–	1%	
	Load Regulation	I_{OUT} = 0 A to 4 A	–	–	1%	
V_{OUT1_rip}	Output Voltage Ripple	V_{IN} = 12 V, I_{OUT} = 4 A	–	–	30	mVpp
I_{OUT1}	Output Current 1	V_{IN} = 8 V to 22 V	0		4	A
V_{OUT2}	Output Voltage 2	V_{IN} = 12 V, I_{OUT} = 2 A	1.78	1.80	1.82	V
	Line Regulation	V_{IN} = 8 V to 22 V	–	–	1%	
	Load Regulation	I_{OUT} = 0 A to 4 A	–	–	1%	
V_{OUT2_rip}	Output Voltage Ripple	V_{IN} = 12 V, I_{OUT2} = 4 A	–	–	30	mVpp
I_{OUT2}	Output Current 2	V_{IN} = 8 V to 22 V	0		4	A
Systems Characteristics						
F_{SW}	Switching Frequency		200	350	400	kHz
ηpk	Peak Efficiency	V_{IN} =12	–	88%	–	
η	Full Load Efficiency	V_{IN} = 12, I_{OUT1} = I_{OUT2} = 4 A	–	80%	–	

3 TPS53125EVM-599 Schematic



For reference only; see Table 8-1 for specific values.

Figure 3-1. TPS53125EVM-599 Schematic

4 Connector and Test Point Descriptions

4.1 Enable Jumpers/Switches – SW1 and SW2

The TPS53125EVM-599 board includes independent enable switches for each of the two outputs. When the switch is in the DIS position, the channel is disabled and discharged per the internal discharge characteristics of the TPS53125.

To enable VOUT1, place SW1 in the EN position. To enable VOUT2, place SW2 in the EN position.

4.2 Test Point Descriptions

Table 4-1 lists the test points, their labels, uses, and where additional information is located.

Table 4-1. Test Point Description

Test Point	Label	Use	Section
TP1	TEST1	Monitor Channel 1 Soft-Start Voltage	Section 4.2.4
TP2	TEST2	Monitor Channel 2 Soft-Start Voltage	Section 4.2.4
TP3	GND	Ground for Input Voltage	Section 4.2.1
TP4	GND	Ground for Channel 1 Output Voltage	Section 4.2.2
TP5	SW1	Monitor Switching Node for Channel 1	Section 4.2.5
TP6	GND	Ground for Channel 2 Output Voltage	Section 4.2.3
TP7	VO2	Monitor Output Voltage for Channel 2	Section 4.2.3
TP8	VO1	Monitor Output Voltage for Channel 1	Section 4.2.2
TP9	VIN	Monitor Input Voltage	Section 4.2.1
TP10	VREG5	Monitor Output of VREG5 Regulator	Section 4.2.6
TP11	SW2	Monitor Switching Node for Channel 2	Section 4.2.5
CN1	VOUT1	Monitor Output Voltage for Channel 1	Section 4.2.2
CN2	VOUT2	Monitor Output Voltage for Channel 2	Section 4.2.3

4.2.1 Input Voltage Monitoring – TPS and TP9

The TPS53125EVM-599 provides two test points for measuring the voltage applied to the module. This allows the user to measure the actual module voltage without losses from input cables and connectors. Measure all input voltage measurements between TP9 and TP3. To use TP9 and TP3, connect a voltmeter positive terminal to TP9 and negative terminal to TP3.

4.2.2 Channel 1 Output Voltage Monitoring – TP4 and TP8 or CN1

The TPS53125EVM-599 provides two test points for measuring the voltage generated at the VO1 output by the module. This allows the user to measure the actual output voltage without losses from output cables and connectors. Measure all DC output voltage between TP8 and TP4. To use TP8 and TP4, connect a voltmeter positive terminal to TP8 and negative terminal to TP4.

The TPS53125EVM-599 also provides a shielded oscilloscope jack to allow AC measurements of the output ripple. Insert an oscilloscope probe with exposed ground barrel into CN1 for all output 1 ripple measurements.

4.2.3 Channel 2 Output Voltage Monitoring – TP6 and TP7 or CN2

The TPS53125EVM-599 provides two test points for measuring the voltage generated at the VO1 output by the module. This allows the user to measure the actual output voltage without losses from output cables and connectors. Measure all DC output voltage measurements between TP7 and TP6. To use TP7 and TP6, connect a voltmeter positive terminal to TP7 and negative terminal to TP6.

The TPS53125EVM-599 also provides a shielded oscilloscope jack to allow ac measurements of the output ripple. Insert an oscilloscope probe with exposed ground barrel into CN2 for all output 2 ripple measurements.

4.2.4 Soft-Start Voltage Monitoring – TP1, TP2, and TP3

The TPS53125EVM-599 provides two test points for measuring the soft-start ramp voltages. TP1 monitors the soft-start ramp of Channel 1. TP2 monitors the soft-start ramp of Channel 2. To use TP1 or TP2, connect an oscilloscope probe between TP1 or TP2 and TP3.

4.2.5 Switching Node Monitoring – TP3, TP5, and TP11

The TPS53125EVM-599 provides two test points for measuring the switching node waveform voltages. TP5 monitors the switching node of Channel 1. TP2 monitors the switching node of Channel 2. To use TP5 or TP11, connect an oscilloscope probe between TP5 or TP11 and TP3.

4.2.6 5-V Regulator Output Monitoring – TP3 and TP10

The TPS53125EVM-599 provides a test point for measuring the output of the internal 5-V regulator. TP10 monitors the output voltage of the internal 5-V regulator. To use TP10, connect a voltmeter positive terminal to TP10 and negative terminal to TP3.

5 Test Setup

5.1 Equipment

The following equipment is recommended for testing the TPS53125EVM-599 evaluation board.

5.1.1 Voltage Source

The input voltage source, V_{VIN}, must be a 0-V to 15-V, variable DC source capable of supplying 3 A_{DC} minimum.

5.1.2 Meters

A1: 0-A_{DC} to 4-A_{DC} ammeter

V1: VIN, 0-V to 22-V voltmeter

V2: VOUT1, 0-V to 2-V voltmeter

V3: VOUT2, 0-V to 2-V voltmeter

5.1.3 Loads

LOAD1: One output load is an electronic load set for constant current mode capable of 0 A_{DC} to 4 A_{DC} at 1.05 V_{DC}.

LOAD2: The other output load is an electronic load set for constant current mode capable of 0 A_{DC} to 4 A_{DC} at 1.8 V_{DC}.

5.1.4 Oscilloscope and Probe

The oscilloscope, analog or digital, must be set for ac-coupled measurement with a 20-MHz bandwidth limiting. Use 20-mV/division vertical resolution and 1.0-µs/division horizontal resolution for the output ripple voltage test. Set cursors at +20 mV and –20 mV.

The oscilloscope probe must be a Tektronix P6138 or equivalent oscilloscope probe with exposed conductive ground barrels.

5.1.5 Recommended Wire Gauge

V_{VIN} to J3 – The connection between the source voltage, V_{VIN}, and J1 of thTPS53125EVM-599 can carry as much as 2 A_{DC}. The minimum recommended wire size is AWG #16 with the total length of wire less than two feet (1-foot input, 1-foot return).

J1 to LOAD1 and J2 to LOAD2 – The connection between J1 and LOAD1 and J2 and LOAD2 of the TPS53125EVM-599 can carry as much as 4 A_{DC} each. The minimum recommended wire size is AWG #14, with the total length of wire less than two feet (1-foot input, 1-foot return).

5.1.6 Other Test Equipment

Fan – The TPS53125EVM-599 evaluation module includes components that can become hot to the touch. Because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200–400 lfm is required to reduce component temperatures when operating.

5.2 Equipment Setup

Figure 5-1 shows the basic test setup that is recommended to evaluate the TPS53125EVM-599. Note that although the return for J3 and J1 and JP2 are the same system ground, the connections must remain separate as shown in Figure 5-1.

5.2.1 Test Procedure

1. When working at an ESD workstation, ensure that wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses are also recommended.
2. Prior to connecting the DC input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 3 A_{DC} maximum. Ensure that V_{IN} is initially set to 0 V and connected as shown in Figure 5-1.
3. Verify SW1 and SW2 are in the desired position.
4. Increase VIN from 0 V to 12 V_{DC}.
5. Vary VIN between 8 V_{DC} and 22 V_{DC}.
6. Vary LOAD1 between 0 A and 4 A_{DC}.
7. Vary LOAD2 between 0 A and 4 A_{DC}.
8. Adjust SW1 between EN and DIS.
9. Adjust SW2 between EN and DIS.
10. Set SW1 to DIS.
11. Set SW2 to DIS.
12. Decrease LOAD1 to 0 A.
13. Decrease LOAD2 to 0 A.
14. Decrease VIN to 0 V.

5.2.2 Test Setup Diagram

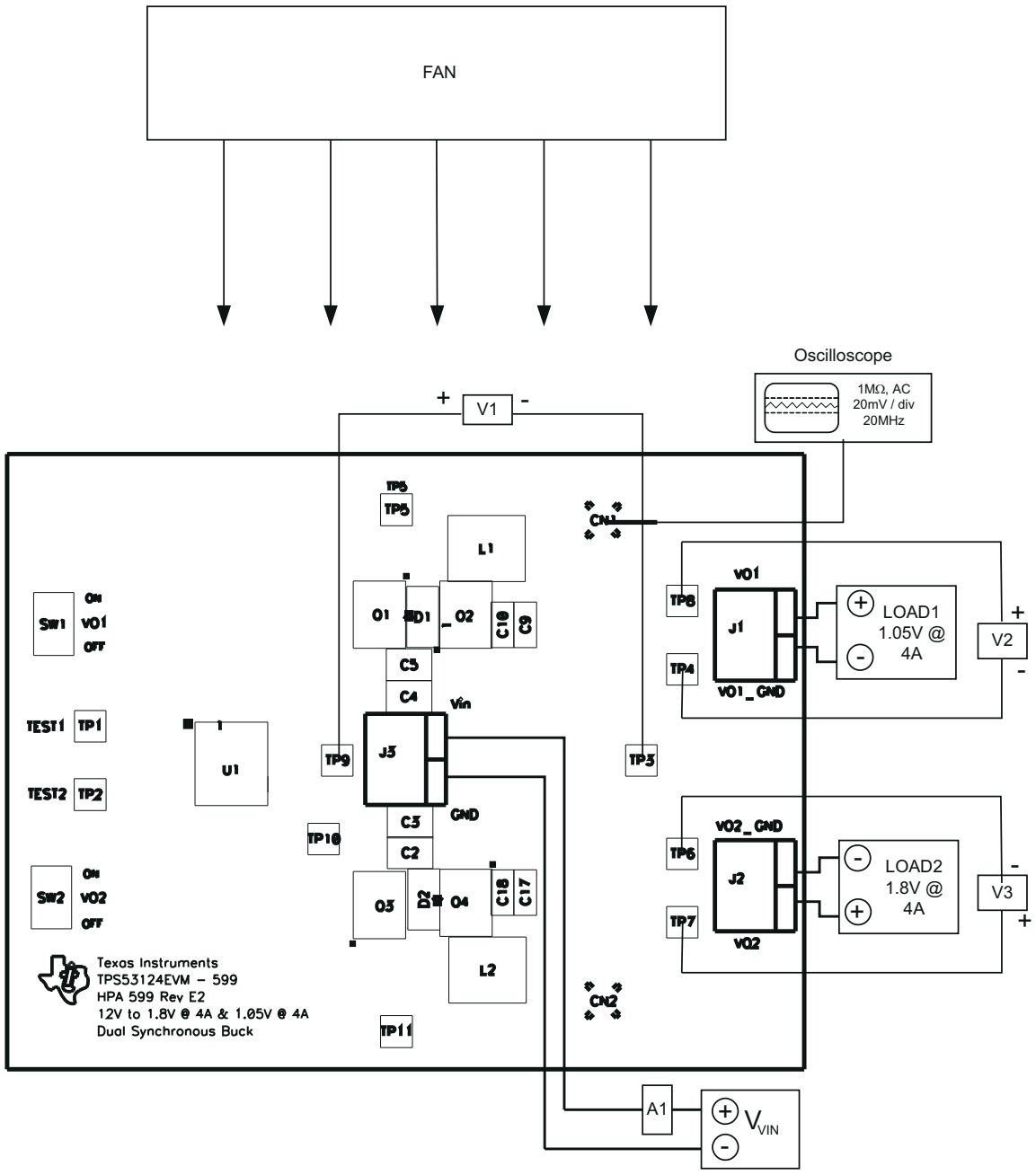


Figure 5-1. TPS53125EVM-599 Recommended Test Setup

5.3 Start-Up/Shutdown Procedures

Perform the start-up and shutdown procedures in the following manner.

1. Increase V_{IN} from 0 V to 12 V_{DC}.
2. Vary LOAD1 from 0 A–4 A_{DC}.
3. Vary LOAD2 from 0 A–4 A_{DC}.
4. Vary V_{IN} from 8 V_{DC} to 22 V_{DC}.
5. Decrease V_{IN} to 0 V_{DC}.
6. Decrease LOAD1 to 0 A.
7. Decrease LOAD2 to 0 A.

5.4 Output Ripple Voltage Measurement Procedure

Perform the output ripple voltage measurement procedure in the following manner.

1. Increase V_{IN} from 0 V to 12 V_{DC}.
2. Adjust LOAD1 to desired load between 0 A_{DC} and 4 A_{DC}.
3. Adjust LOAD2 to desired load between 0 A_{DC} and 4 A_{DC}.
4. Adjust V_{IN} to desired load between 8 V_{DC} and 22 V_{DC}.
5. Connect an oscilloscope probe to CN1 or CN2 shown in Figure 5-1.
6. Measure the output ripple.
7. Decrease V_{IN} to 0 V_{DC}.
8. Decrease LOAD1 to 0 A.
9. Decrease LOAD2 to 0 A.

5.5 Equipment Shutdown

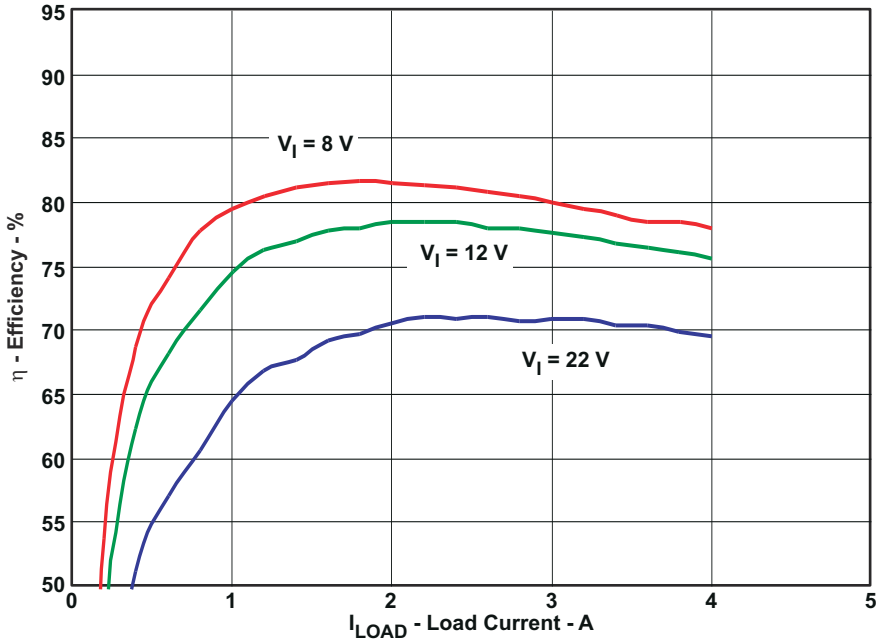
Shut down the equipment in the following manner.

1. Shut down the oscilloscope.
2. Shut down V_{IN}.
3. Shut down LOAD1.
4. Shut down LOAD2.
5. Shut down FAN.

6 TPS53125EVM-599 Test Data

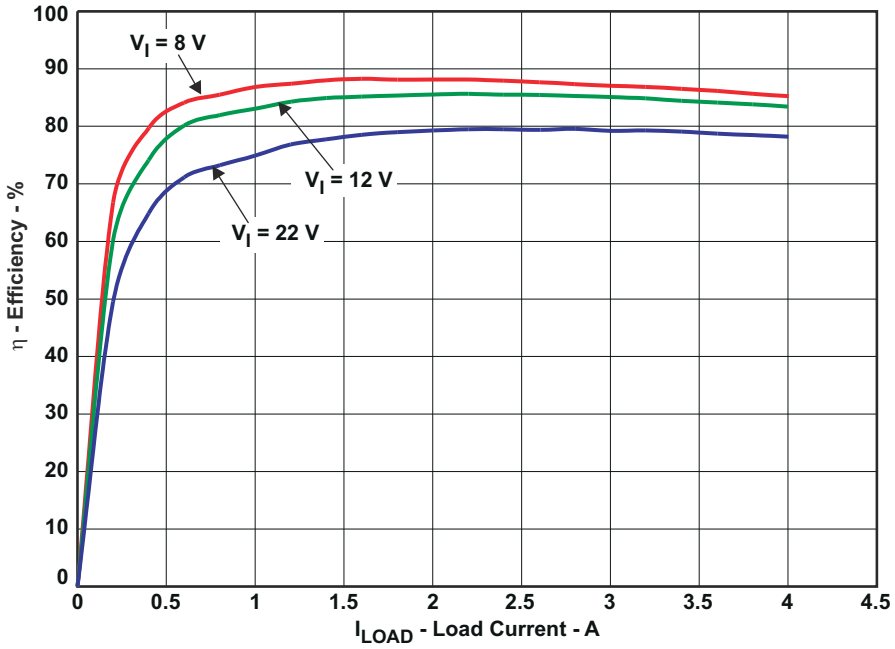
Figure 6-1 through Figure 6-8 present typical performance curves for the TPS53125EVM-599. Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

6.1 Efficiency



V_{IN} = 8 V – 22 V, V_{OUT1} = 1.05 V, I_{OUT1} = 0 A – 4 A

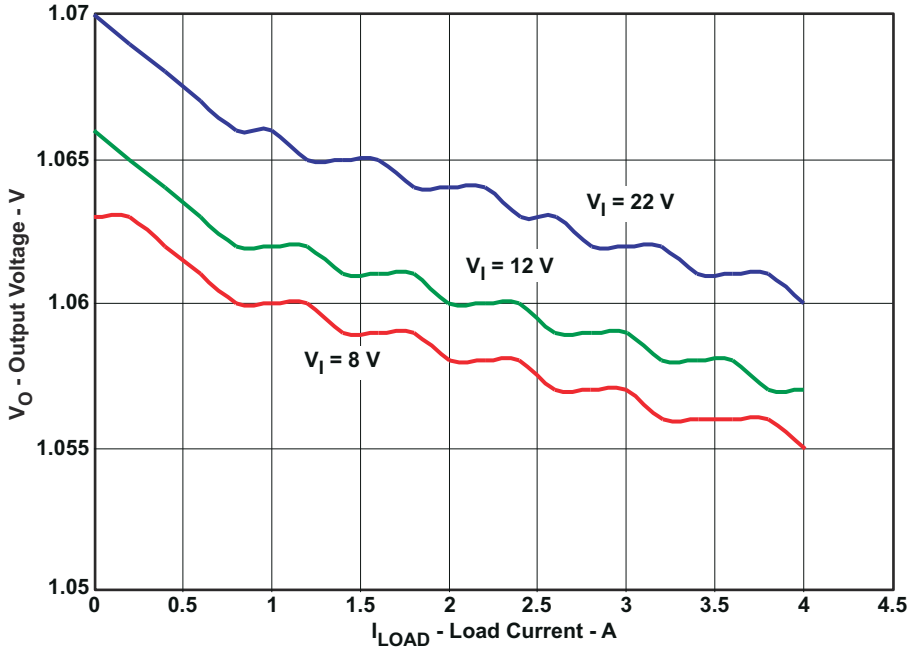
Figure 6-1. TPS53125EVM-599 Efficiency vs Load Current



V_{IN} = 8 V – 22 V, V_{OUT2} = 1.80 V, I_{OUT2} = 0 A – 4 A

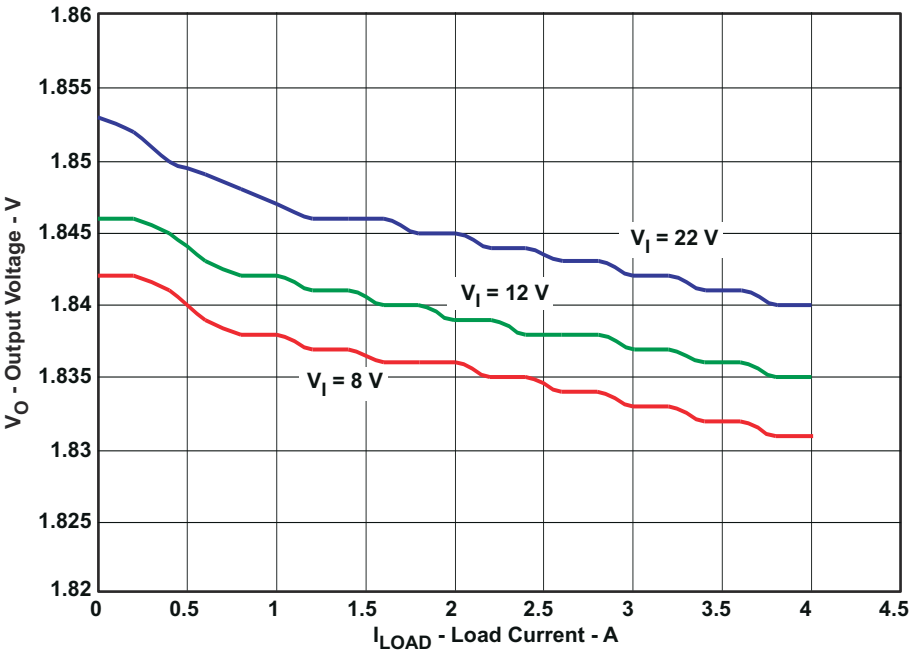
Figure 6-2. TPS53125EVM-599 Efficiency vs Load Current

6.2 Line and Load Regulation



V_{IN} = 8 V – 22 V, V_{OUT1} = 1.05 V, I_{OUT} = 0 A – 4 A

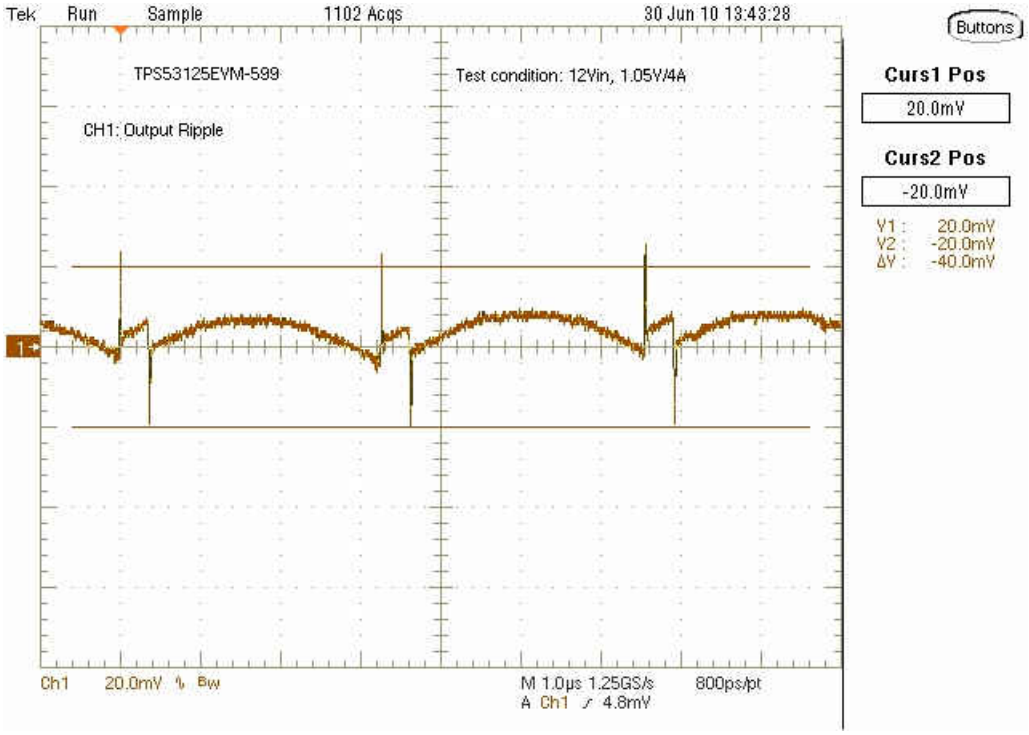
Figure 6-3. TPS53125EVM-599 Output Voltage vs Load Current



V_{IN} = 8 V – 22 V, V_{OUT1} = 1.80 V, I_{OUT} = 0 A – 4 A

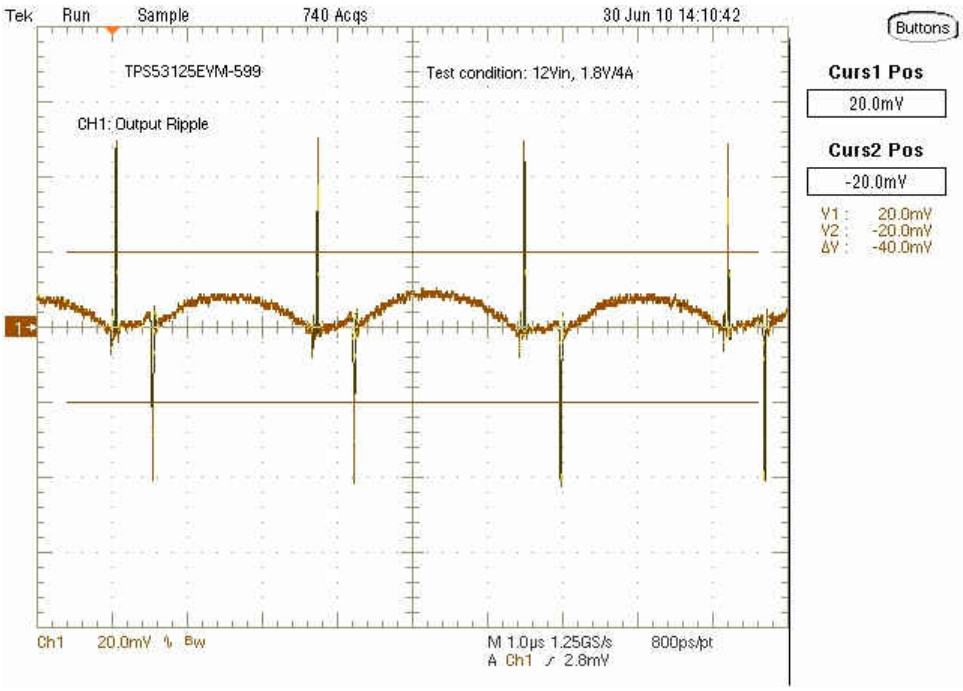
Figure 6-4. TPS53125EVM-599 Output Voltage vs Load Current

6.3 Output Voltage Ripple and Switching Node Waveforms



V_{IN} = 12, V_{OUT1} = 1.05, I_{OUT1} = 4 A

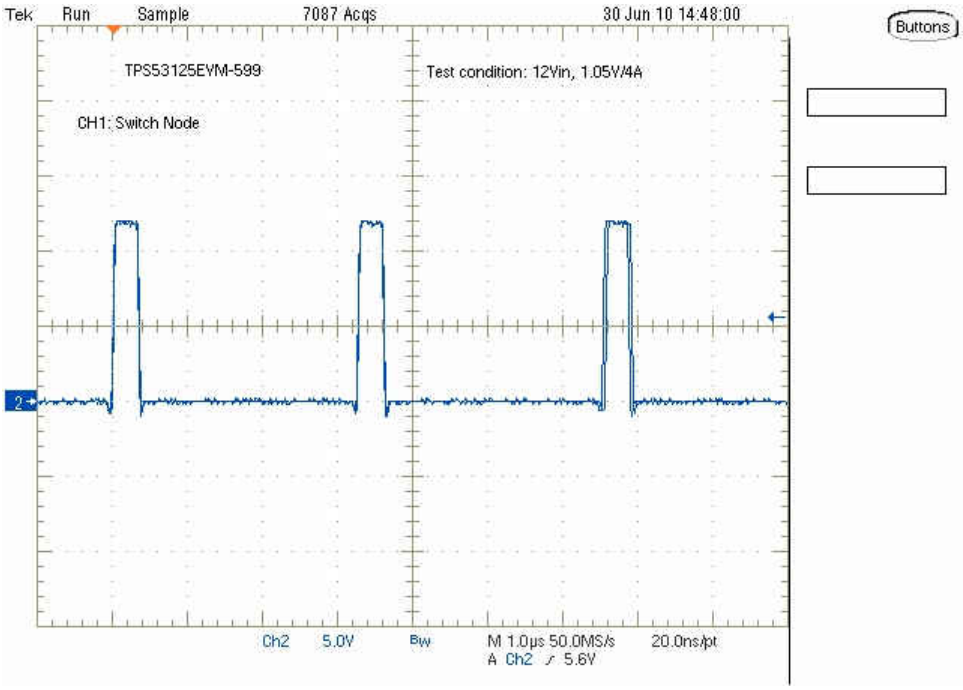
Figure 6-5. TPS53125EVM-599 Output Voltage Ripple and Switching Waveform



V_{IN} = 12, V_{OUT2} = 1.80, I_{OUT2} = 4 A

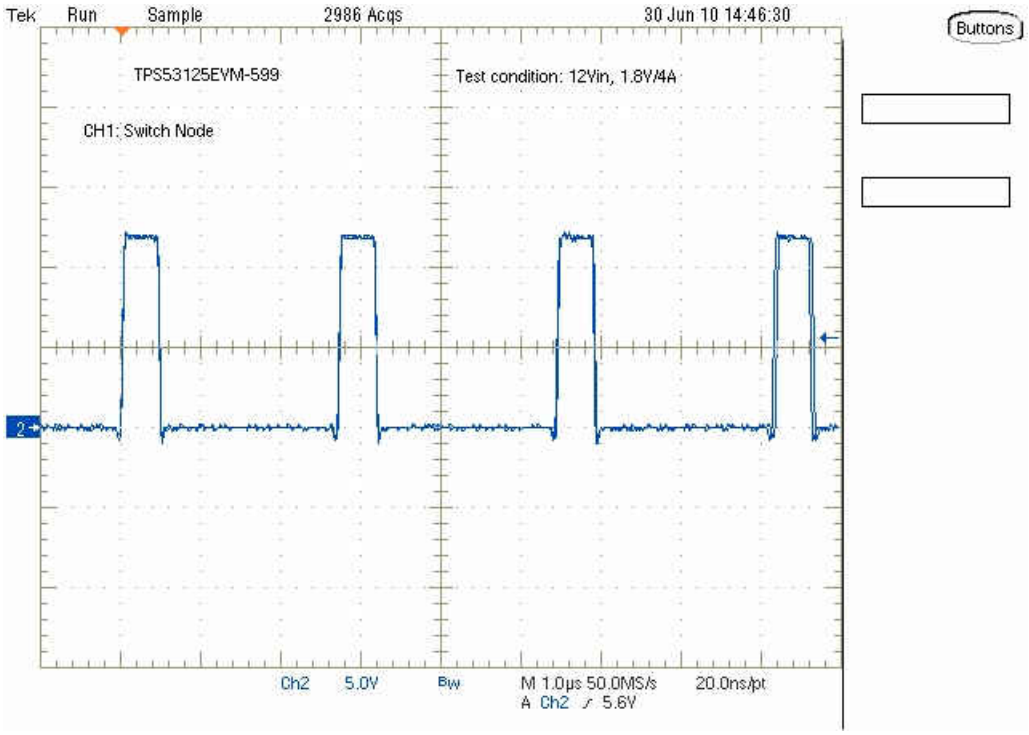
Figure 6-6. TPS53125EVM-599 Output Voltage Ripple

6.4 Switch Node



tV_{IN} = 12, V_{OUT1} = 1.05, I_{OUT1} = 4A, Ch1: TP5 (SW1)

Figure 6-7. TPS53125EVM-599 Switching Waveforms



V_{IN} = 12, V_{OUT2} = 1.80, I_{OUT2} = 4A Ch1: TP11 (SW2)

Figure 6-8. TPS53125EVM-599 Switching Waveforms

7 TPS53125EVM-599 Assembly Drawings and Layout

Figure 7-1 through Figure 7-5 show the design of the TPS53125EVM-599 printed-circuit board. The EVM has been designed using a 4-layer, 2-oz copper-clad circuit board 3.5 in 2.7 to allow the user to easily view, probe, and evaluate the TPS53125 control IC in a practical application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space-constrained systems.

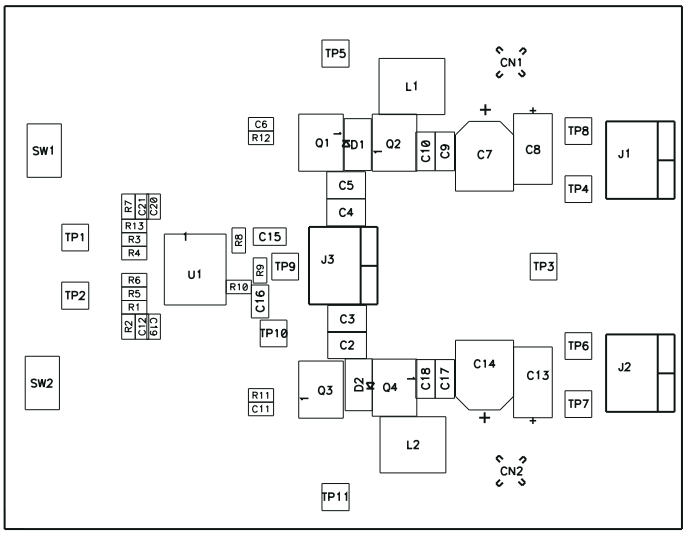


Figure 7-1. TPS53125EVM-599 Component Placement, Viewed From Top

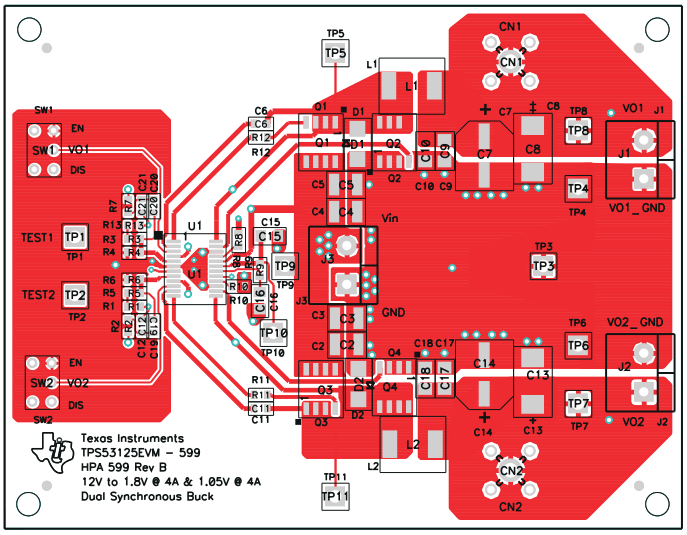


Figure 7-2. TPS53125EVM-599 Top Copper, Viewed From Top

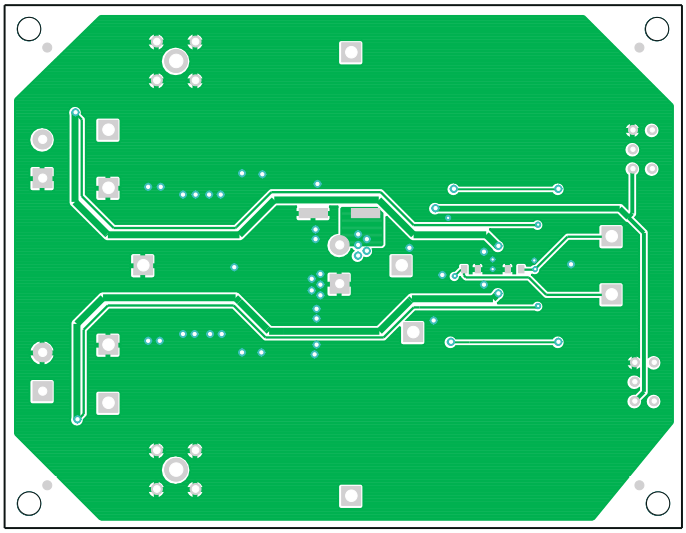


Figure 7-3. TPS53125EVM-599 Bottom Copper, Viewed From Bottom

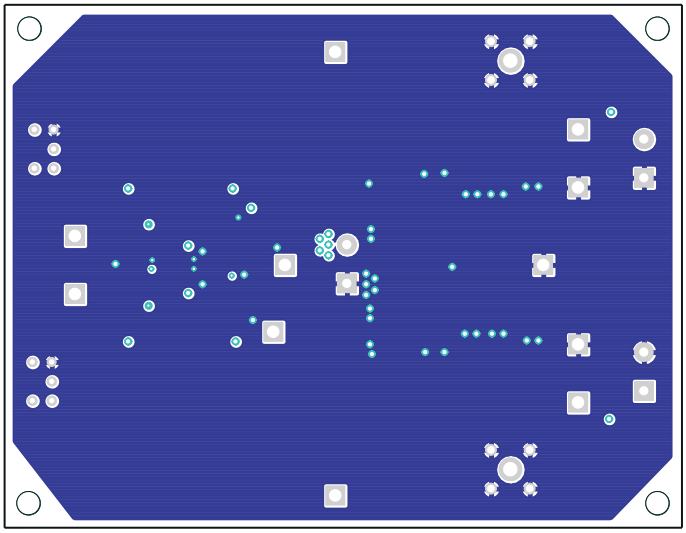


Figure 7-4. TPS53125EVM-599 Internal 1, X-Ray View From Top

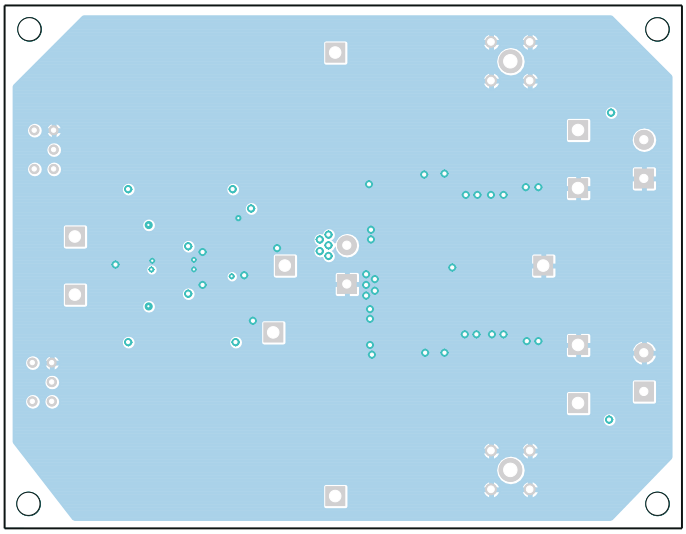


Figure 7-5. TPS53125EVM-599 Internal 2, X-Ray View From Top

8 TPS53125EVM-599 Bill of Materials

Table 8-1 contains the bill of materials for TPS53125EVM-599. The reference designators reference the schematic in Figure 3-1 and assembly locations in Figure 7-1. The components listed with a quantity of 0 are not populated on the PCB but are provided for reference.

Table 8-1. TPS53125EVM-599 Bill of Materials

QTY	RefDes	Value	Description	Size	Part Number	MFR
0	C1		Capacitor, Aluminum, 25 V, 20%	0.328 × 0.390 inch	Std	Std
0	C12, C19, C20, C21		Capacitor, Ceramic,	0603	Std	Std
0	C14, C7		Capacitor, OS CON, 6.3 V, 20%	0.260 Sq inch	Std	Std
1	C15	4.7 µF	Capacitor, Ceramic, 10 V, X5R, 20%	0805	Std	Std
1	C16	1 µF	Capacitor, Ceramic, 16 V, X5R, 20%	0805	Std	Std
4	C9, C10, C17, C18	47 µF	Capacitor, Ceramic, 6.3 V, X5R, 20%	1206	Std	Std
4	C2, C3, C4, C5	10 µF	Capacitor, Ceramic, 25 V, X5R, 20%	1210	Std	Std
2	C22, C23	4700 pF	Capacitor, Ceramic, Low Inductance, 16 V, X7R, 20%	0603	Std	Std
2	C6, C11	0.1 µF	Capacitor, Ceramic, 50 V, X7R, 10%	0603	Std	Std
0	C8, C13	330 µF	Capacitor, PXE, 330-µF, 4.0-V, 15-mΩ, 20%	7343 (D)	APXE4R0ARA331MF61G	NIPPON CHEMI-CON
2	CN1, CN2	131-5031-00	Adaptor, 3.5-mm probe clip (or 131-5031-00)	0.2	131-4244-00	Tektronix
0	D1, D2		Diode, Schottky, 1-A, 30-V	SMA	Std	Std
3	J1, J2, J3	ED120/2DS	Terminal Block, 2-pin, 15-A, 5.1 mm	0.40 × 0.35 inch	ED120/2DS	OST
2	L1, L2	3.3 µH	Inductor, SMT, 5.6 A, 29.7 mΩ	0.256 × 0.280 inch	SPM6530T-3R3M	TDK
2	Q1, Q3	FDS8876	MOSFET, N-ch, 30-V, 10.2-A, 14-mΩ	SO8	FDS8876	Fairchild
2	Q2, Q4	FDS8690	MOSFET, N-ch, 30-V, 11.4-A, 11.4-mΩ	SO8	FDS8690	Fairchild
1	R1	1.82 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R11, R12	10	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R13	430	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R2, R7, R9		Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	3.32 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R4, R6	10.0 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	12.1 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R8, R10	5.62 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	SW1, SW2	G12AP-R0	Switch, ON-ON Mini Toggle	0.28 × 0.18 inch	G12AP-R0	Nikkai
4	TP1, TP2, TP5, TP11	5012	Test Point, White, Thru Hole	0.125 × 0.125 inch	5012	Keystone
1	TP10	5013	Test Point, Orange, Thru Hole	0.125 × 0.125 inch	5013	Keystone
3	TP3, TP4, TP6	5011	Test Point, Black, Thru Hole	0.125 × 0.125 inch	5011	Keystone
2	TP7, TP8	5014	Test Point, Yellow, Thru Hole	0.125 × 0.125 inch	5014	Keystone
1	TP9	5010	Test Point, Red, Thru Hole	0.125 × 0.125 inch	5010	Keystone
1	U1	TPS53125PW	IC, Dual Synchronous Step-Down Controller For Low-Voltage Power Rails	TSSOP	TPS53125PW	TI

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2010) to Revision A (January 2022) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2
- Updated the user's guide title..... 2

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