Application Report
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Minimizing Switch Ringing on TPS53318 and TPS53319 Family of Devices

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ABSTRACT

The system reliability of a high-efficiency DC/DC converter with a fast slew rate is improved when switch node ringing is reduced. This document describes switching ringing reduction methods and lab bench test results with the 14-A TPS53319 and also applies to the pin compatible 8-A TPS53318. Both devices are well-suited for rack-server, single-board-computer, and hardware-accelerator applications that benefit from the fast transient response time of D-CAP™control, or when multi-layer ceramic capacitors are undesirable for the output filter.

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1 Introduction

Due to high-voltage changes (dv/dt) and current changes (di/dt) at the high-speed switching MOSFETs, a significant amount of ringing and overshoot voltage can be observed at the switch node of the synchronous buck converter while the high-side MOSFET is turned on. Even though fast-switching speeds help reduce the switching loss, buck converter efficiency still suffers. This application note focuses on minimizing switch ringing on the TPS53k family of devices of SWIFT™ synchronous step-down converters. First, this document describes switching ringing measurement methods. Next the application report describes how to minimize switching ringing by adding an RC snubber circuit and bootstrap resistor. Lastly, the application report describes the effect of the snubber on efficiency performance of the synchronous buck converter.

2 Proper Measurement Method of Switch Ringing

How and where to measure fast switching ringing at buck regulators is crucial. TI highly recommends using a 1-GHz differential probe and it must be probed as close as possible to the switching node and thermal pad-GND. The voltage probe must have a bandwidth of 500 MHz or more. Figure 1 and Figure 2 show two different probing methods used on TPS53k family devices. Figure 1 shows the single-ended, P6139B device, with a 500-MHz passive probe.

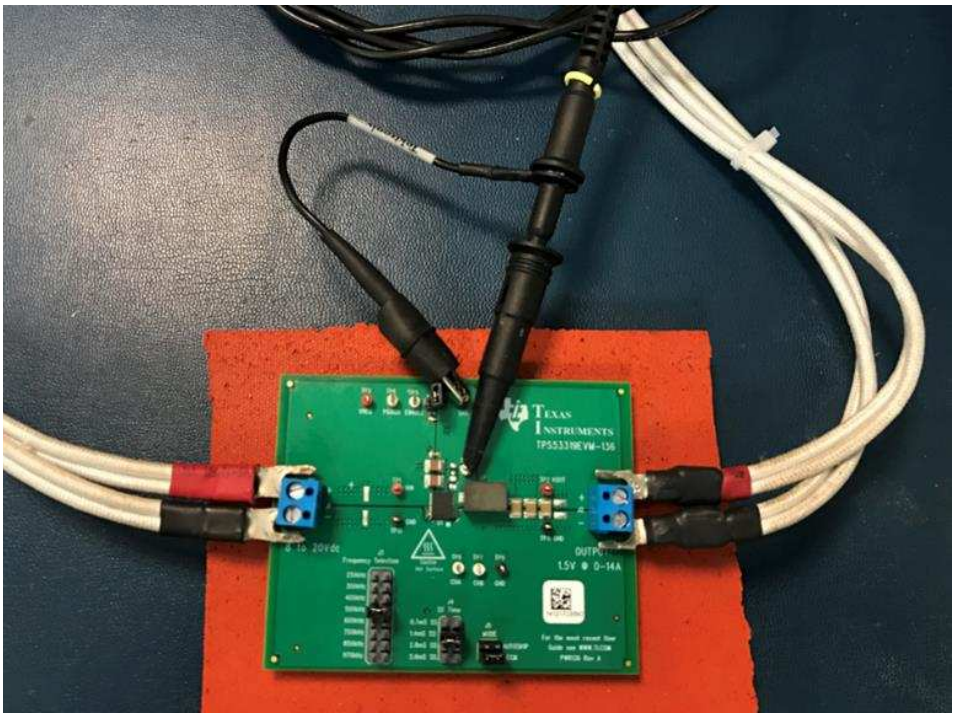


Figure 1. Single–Ended Probing

Figure 2 shows the TDP1000 device, with a 1-GHz differential probe.

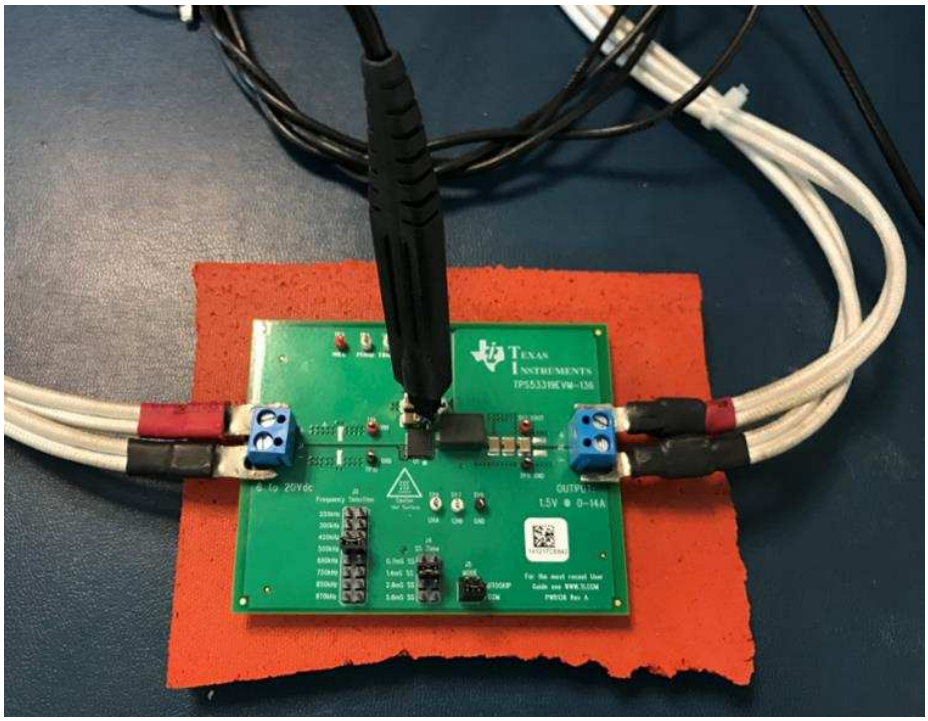


Figure 2. 1-GHz Differential Probing

These probing techniques result in different ringing peak voltages. Because the single-ended probe has 6.5-inch ground wire loop, the probe can pick noises generated from neighboring devices of the system board, which can couple to the switch node voltage. By placing the differential probe close to the IC with two short leads reduces the measurement loop results with less noise coupling to the switch node. Optimal switch ringing can be obtained using this measurement method.

Figure 3 shows a typical switch ringing waveform of the TPS53319 device using a single-ended, 6.5-inch, ground wire loop. The waveform was taken using a single-ended probe at the TPS53319EVM-136 evaluation module (EVM) with 12-V input voltage, 1.5-V output voltage, 14-A load, and 500-kHz switching frequency. The switching peak voltage is 21.76 V; whereas, at the same test condition, using differential probes, the peak switching voltage is 18.4 V. Therefore, improper measurement can result in inaccurate ringing voltage.

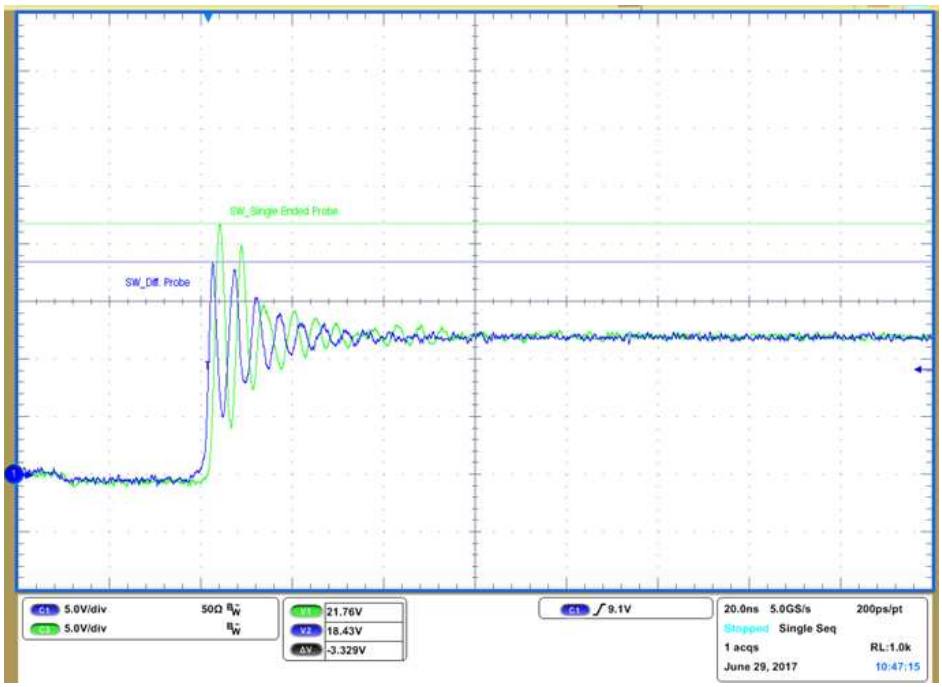


Figure 3. Typical Switch Ringing Waveform of TPS53319 Device

3 Minimizing Switch Ringing by Adding RC Snubber and Bootstrap Circuit

The addition of the RC snubber reduces the switch ringing voltage with a small impact on overall efficiency. This RC snubber is needed to avoid excessive ringing which can cause damage to the devices and high-frequency EMI radiation. The RC snubber must be placed as close as possible to the switch-to-ground pins. Figure 4 and Figure 5 shows the placement of the RC snubber with the parasitic components.

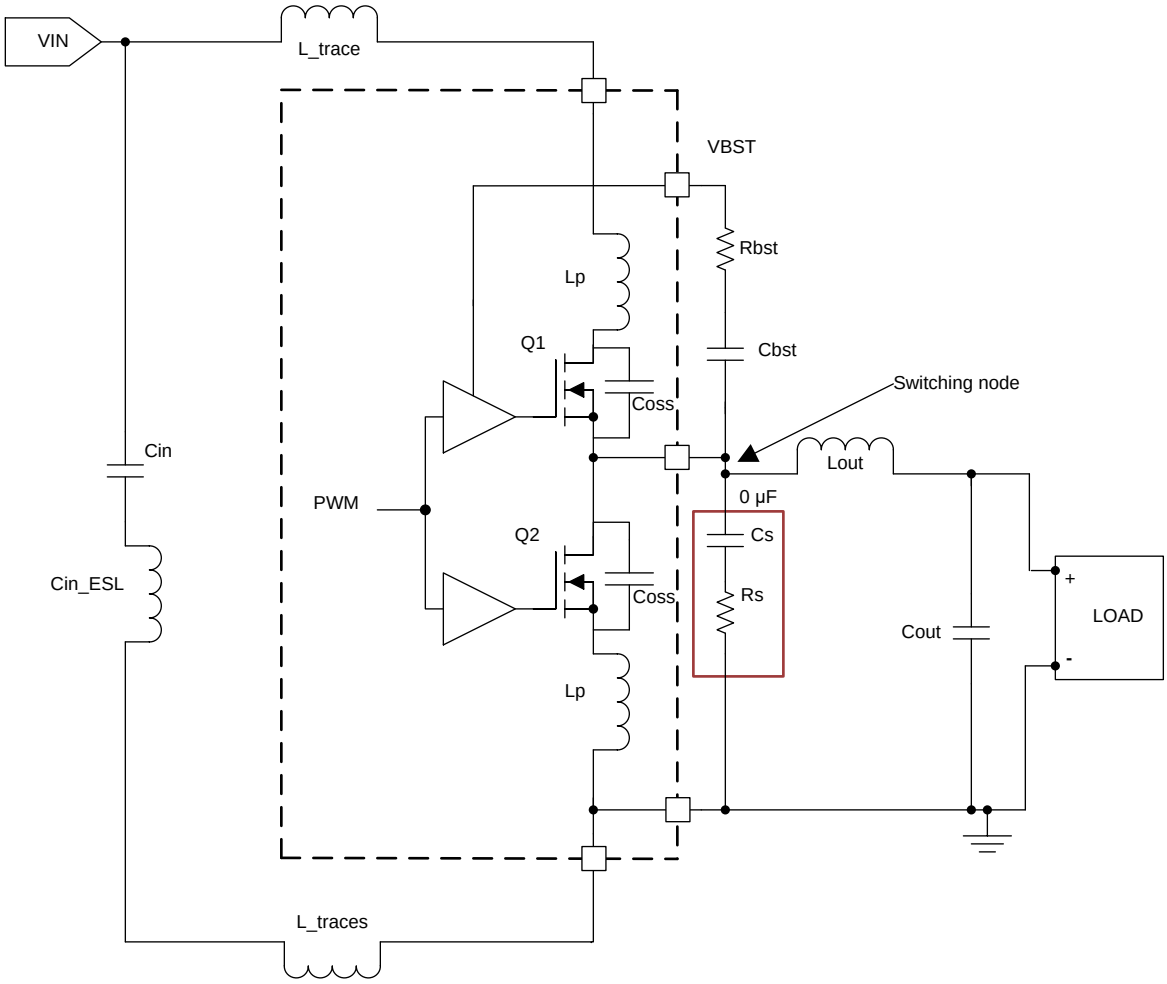


Figure 4. RC Snubber Added Circuit With Parasitic Components

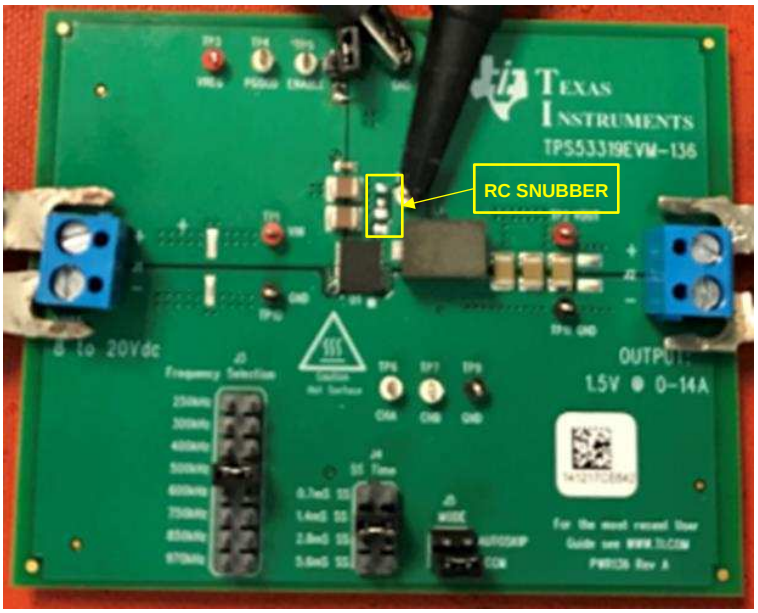


Figure 5. TPS53319EVM-136 RC Snubber Placements

Switch ringing occurs when the high-side MOSFET is on, the low-side MOSFET is off, and with parasitic capacitance and inductance of the internal MOSFETs, which creates a resonance circuit, result in high-frequency switch ringing. Figure 6 shows the rising edge of the switch-on ringing, which is mostly determined by the COSS of the low-side FET and the total parasitic inductance of both FETs switching loop (Lp on both MOSFETs, L_traces, and Cin_ESL).

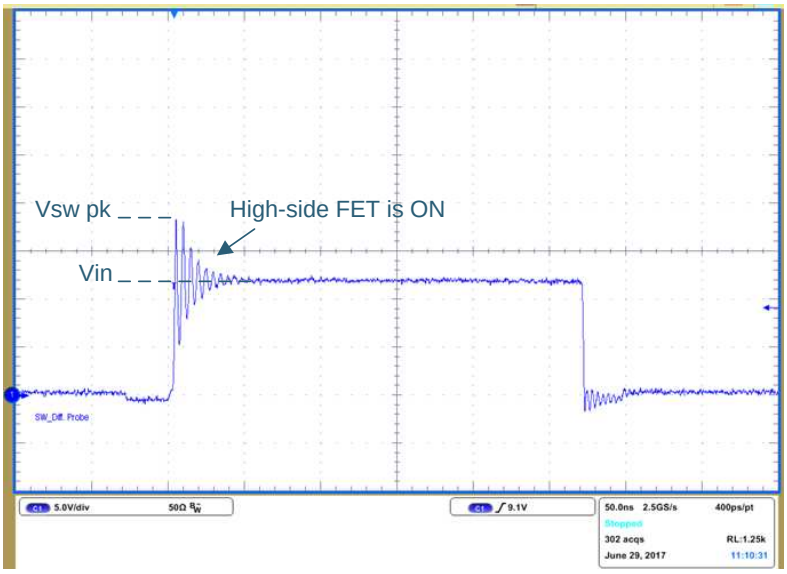


Figure 6. Switch Ringing Waveform Rising and Falling Edges

The parasitic inductance, capacitance, and Rs-snubber values depend on the parasitic inductance and parasitic capacitance, Cp, components of the network. Because of the parasitic value for integrated MOSFETs, the layout parasitic and packaging parasitic, such as wire bond, are unknown. A quick and easy way to determine snubber component values is to measure the ringing frequency (*F*_ring) at the lab bench, then characterize the impedance of the circuit.

3.1 Method of RC Snubber Designing

The following method is used to estimate the RC snubber components.

1. Measure the switch node ringing frequency (*F*_ring) of original circuit without the snubber. Reduce the original ringing frequency in half by adding a small capacitor from the switch to GND.

NOTE: Usually, the added capacitance, which is snubber capacitor, Cs, is chosen to be approximately three times larger than the total parasitic capacitance, Cp. Therefore, the total resonance parasitic capacitor is approximately 1/3 of the added capacitance.

2. Estimate parasitic inductance, Lp, using the original ringing frequency and the ringing frequency after adding the snubber capacitor and two capacitances (Cp and Cp + Cs).
3. Estimate the parasitic switch node capacitance, Cp.
4. Finally, determine the snubber resistor, Rs, that is required for optimal damping.

To estimate Lp, the parasitic inductance of the circuit, first measure the switch ringing frequency, Fring_1 (T1), of the original circuit without the snubber. Next, add the external snubber capacitor, Cs, in the circuit (from the switch to GND) and increase the value of the capacitor until the frequency of the ringing to be damped has been reduced by half (Fring_2). This means the change of the period (T2) doubled when changing the original parasitic capacitance, Cp, to Cp + Cs.

Estimate parasitic capacitance, Cp, and parasitic inductance, Lp, to calculate the snubber resistor, Rs, that is required for optimal damping. The damping factor, ξ, for the damping response of the LC circuit usually ranges from $\xi < 1$ (under damped) to $\xi = 1$ (critically damped). The value of the snubber resistor is equal to the characteristic impedance of the parasitic resonant circuit and that provides damping near $\xi = 1$.

The characteristics of impedances of the LC circuit can be expressed as follows. Equation 1 shows the natural resonate of the LC frequency.

$$\omega_n = \frac{1}{\sqrt{LPCp}} \tag{1}$$

Equation 2 shows the resonate ringing frequency or period without adding an external capacitor.

$$F\_ring\_1 = \frac{1}{2\pi\sqrt{LPCp}} \quad T_1 = 2\pi\sqrt{LpCp} \rightarrow T_1^2 = 4\pi^2 LpCp \tag{2}$$

Equation 3 shows the reduced ringing frequency by half (the period doubled) after adding a small capacitor, Cs.

$$F\_ring\_2 = \frac{1}{2\pi\sqrt{LP\left(Cp + Cs\right)}} \quad T_2 = 2\pi\sqrt{Lp\left(Cp + Cs\right)} \rightarrow T_2^2 = 4\pi^2 LP\left(Cp + Cs\right) \tag{3}$$

Subtract Equation 2 from Equation 3, then manipulate the two equations to find Lp then Cp (see Equation 4 and Equation 5).

$$Lp = \frac{T_2^2 - T_1^2}{4\pi^2 Cs} \text{ or } Lp = \frac{1}{4\pi^2\left(Fring_2 - Fring1\right)^2 Cs} \tag{4}$$

$$Cp \approx \frac{1}{4\pi^2\left(Fring1\right)^2 Lp} \tag{5}$$

After calculating Lp and Cp, determine the snubber resistor, Rs, that is required for optimal damping. By setting $\xi = 1$, the value of the snubber resistor can be calculated as follows in Equation 6.

$$\xi = \frac{1}{2Rs}\sqrt{Lp/Cp} \text{ Damping Factor } RS = \frac{1}{2\xi}\sqrt{Lp/Cp} \tag{6}$$

4 Practical Design

Figure 7 shows an example of a typical, unsnubbed, Rbst = 0 Ω, switch ringing waveform of the TPS53319 D-CAP™ mode, with a 14-A synchronous buck converter that provides a fixed 1.5-V output at up to 14 A from a 12-V input bus. The board is operated at 500-kHz switching frequency, 12 V_{in} and 1.5 V/14 A load. This design example uses the *High Efficiency 14A Synchronous Buck Converter with Eco-Mode™* user's guide.

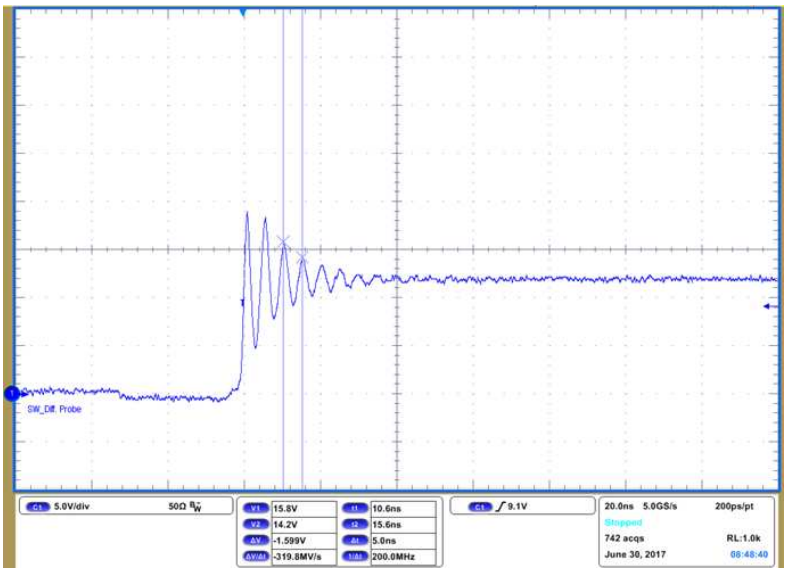
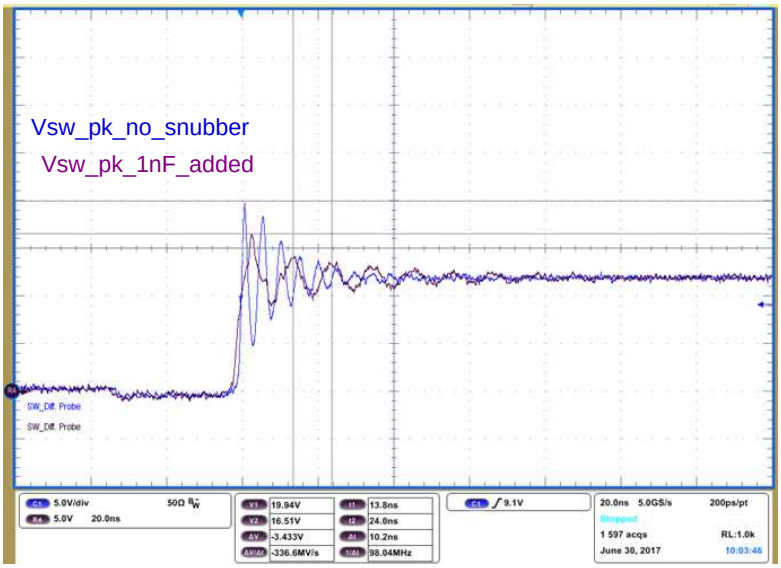


Figure 7. Switch Node Ringing Waveform Without Snubber

Figure 8 shows the unsnubbed switch node with a peak voltage of 19.9 V and a ringing frequency (*F_ring*_1) of 200 MHz.



(1) Purple: 1-nF capacitor added

(2) Blue: no snubber added

Figure 8. Switch Ringing Waveforms With Snubber

To reduce this original ringing frequency, a small capacitor was added. The goal is to reduce the original ringing frequency in half, by increasing the value of the capacitor. The 1-nF capacitor was chosen and placed from the switch to GND, which reduced the original frequency to 98 MHz (*F_ring_2*) and reduced peak voltage to 16.5 V. Now estimate Lp using the original ringing frequency, F_ring_1, and the ringing frequency after adding Cs, F_ring_2.

Using Equation 4, the parasitic inductance, Lp, is calculated as 2.43 nH (see Equation 7) and the parasitic capacitance, Cp, is approximately 261 pF (see Equation 8).

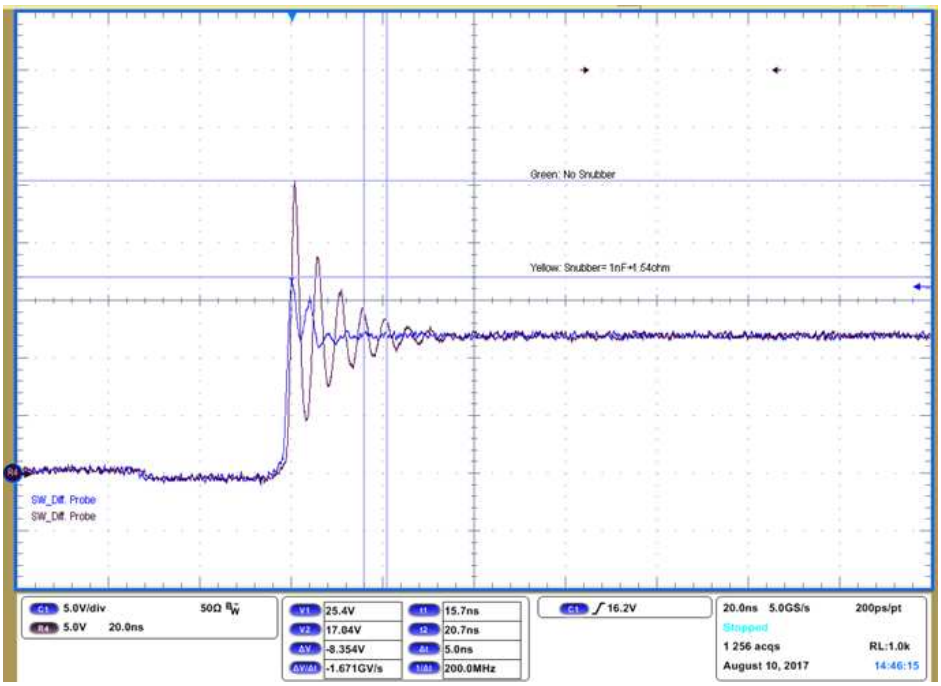
$$Lp = \frac{1}{4\pi^2 \left(98\ \text{MHz} - 200\ \text{MHz}\right)^2 1\,\text{nF}} = 2.43\ \text{nH} \tag{7}$$

$$Cp \approx \frac{1}{4\pi^2 (200\ \text{MHz})^2 2.43\ \text{nH}} = 261\,\text{pF} \tag{8}$$

When Lp and Cp are determined, the snubber resistor, Rs, which is required for optimal damping, is 1.53 Ω, and because 1.53 Ω is not available, an Rs = 1.54 Ω, 0805 chip resistor is used for this example.

$$Cp \approx \frac{1}{4\pi^2 (200\ \text{MHz})^2 2.43\ \text{nH}} = 261\,\text{pF} \tag{9}$$

With the previously calculated RC value, the RC snubber network (1.54 Ω + 1 nF) was placed at the switch to ground and optimum switch node ringing was measured at different load conditions. For instance, at the 14-A load condition, the snubber circuit reduced the switch ringing peak voltage to 17.04 V from 25.4 V. Figure 9 shows the ringing waveforms at a 14-A load with the snubber = 1 nF + 1.54 Ω, and without the snubber.



(1) Blue: With Snubber 1nF+1.54Ω;

(2) Purple: no snubber

Figure 9. Switch Node Ringing Waveforms at 14-A Load

Table 1 lists different RC snubber configurations test data.

Table 1. TPS53319 and TPS53318 Devices: Comparing Ringing Voltage of Three Snubbers

Test Condition	No Snubber Rbst = 0 Ω + 0.1 µF		Snubber = 1.54 Ω + 1000 pF Rbst = 0 Ω + 0.1 µF		Snubber = 1.54 Ω + 560 pF Rbst = 0 Ω + 0.1 µF	
V_{IN} = 12 V V_{OUT} = 1.5 V Temperature = 25°C F_{sw} = 500 kHz	Vsw_pk	dV/dt (V/nsec)	Vsw_pk	dV/dt (V/nsec)	Vsw_pk	dV/dt (V/nsec)
Load = 4 A	18	7.6	14.7	5.05	14.7	5.7
Load = 8 A	22	12.4	15.4	6.2	16	7.0
Load = 14 A	26	16.3	17.5	10.1	18.4	10.35

5 Adding Bootstrap Resistor

Another way to reduce switch ringing is to add a boot resistor, Rbst, in series with the boot capacitor, Cbst, as shown in Figure 4, to slow down the turn-on of the high-side MOSFET. To control the rising rate of the switch node and reduce the V_{sw} ring, add the Rbst = 0 Ω resistor and increase the Rbst resistance until the desired switch node ringing voltage is met. Figure 10 and Table 2 show the switch node ring comparison with the boot resistor = 0 Ω, 1.54 Ω, and 3.01 Ω at the same load conditions. For example, with Rbst = 0 Ω, the peak voltage of the switch node is 24.5 V and 14 V/nsec, and when Rbst = 3.01 Ω, the peak voltage of the switch node is reduced to 18 V and the rising edge is reduced to 10.4 V/nsec.

Table 2. TPS53319 and TPS53318: Comparing Ringing Voltage of three Bootstrap Resistors

Test Condition	Rbst = 0 Ω + 0.1 µF No snubber		Rbst = 0 Ω + 0.1 µF No Snubber		Rbst = 0 Ω + 0.1 µF No Snubber	
V_{IN} = 12 V V_{OUT} = 1.5 V Temperature = 25°C F_{sw} = 500 kHz	Vsw_pk	dV/dt (V/nsec)	Vsw_pk	dV/dt (V/nsec)	Vsw_pk	dV/dt (V/nsec)
Load = 14 A	24.5	14	20	11.7	18	10.4

So, increasing the boot resistor affects the turn-on of the high-side MOSFET and the related rising edge of the switch node voltage; however, as shown in Figure 10 adding a higher boot resistor does not affect the ringing frequency.

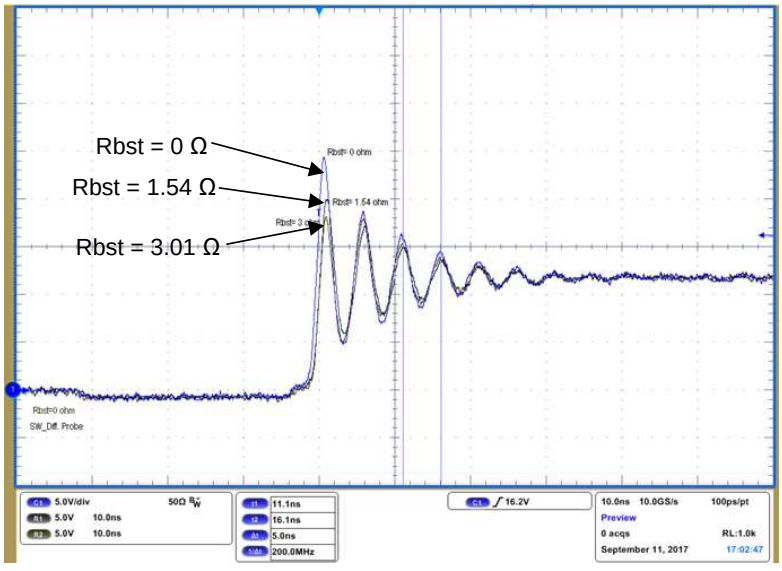
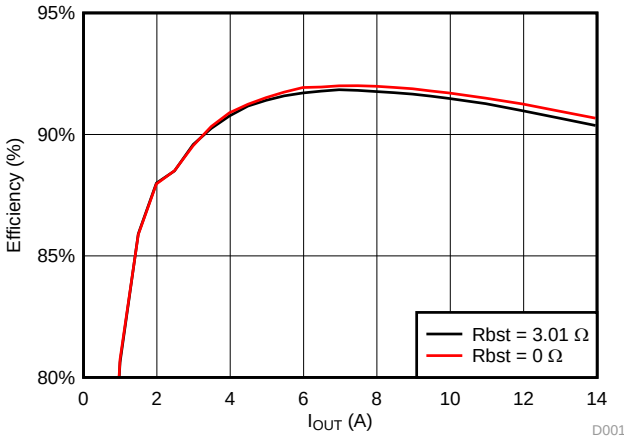


Figure 10. Affect of Boot Resistors on Ringing Voltage When Rbst = 0 Ω, 1.54 Ω, and 3 Ω

Adding a 3.01-Ω boost resistor has little efficiency impact on the converter. As shown in Figure 11, the 3.01-Ω boot resistor does not affect the efficiency at the light load current (< 5 A). Even at a load greater than 5 A, the boot resistor still has little effect on efficiency. With Rbst = 3.01 Ω, the efficiency at 14-A load current is 90.37%; however, with Rbst = 0 Ω, efficiency at the 14-A load current is 90.67%. Therefore, beacause increasing the boot resistor slows the MOSFET switch-on timing and increases switching power loss, the efficiency suffers as a result.



(1) Black: RBST = 3.01 Ω with 12 V_{IN}, 1.5 V_{OUT}, at 500 MHz and 25°C (no snubber)

(2) Red: RBST = 0 Ω with 12 V_{IN}, 1.5 V_{OUT}, at 500 MHz and 25°C (no snubber)

Figure 11. Boot Resistor Effects on Efficiency

6 Affects of Snubber on Efficiency Performance

Using Philip Todd's classic paper [2], the power dissipated in Rs can be estimated from the peak energy stored in Cs (see Equation 10).

$$PCs = \frac{1}{2} Cs\ V^2 sw \tag{10}$$

This is the amount of energy dissipated in Rs when Cs is charged and discharged in each switching cycle. By the principle of conservation of charge, an amount of energy equal to that stored is dissipated. This amount of power dissipation is independent of the snubber resistor; therefore, the average power dissipation at a given switching frequency (F_{sw}), Cs, and charging voltage, V_{sw}, can be estimated as follows (see Equation 11).

$$Pdiss \approx 2\left(\frac{1}{2} Cs\ V^2 sw\right) Fsw = FswCsV_{sw}^2 \tag{11}$$

Therefore, the main factor of power loss in the snubber circuit is Cs. It is essential to keep the snubber capacitor as small as possible for less power loss. Increasing Cs increases the power loss. For example, at an 8-A load current using Cs = 1000 pF, the efficiency is 91.62%, and at the same test condition with load current = 8 A with Cs = 330 pF, the efficiency is 91.81%. It is noticeable that using a small snubber capacitor improves the efficiency of the buck converter.

The following data in Figure 12 shows the efficiency performance of the TPS53319 converter using three different snubber capacitance configurations:

- Snubber = 1.54 Ω+1000 pF and Rbst = 0 Ω + 0.1 µF
- Snubber = 1.54 Ω+ 560 pF and Rbst = 0 Ω + 0.1 µF
- Snubber = 1.54 Ω+ 330 pF and Rbst = 0 Ω + 0.1 µF

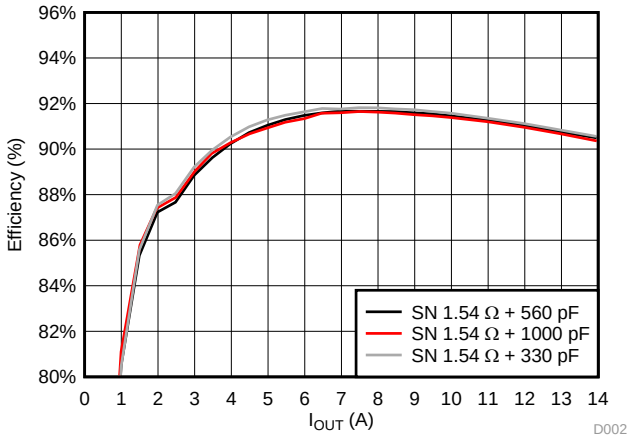


Figure 12. Efficiency Comparison When Snubber Capacitance-Cs Changes

7 Summary

In this application note, the proper measurement of switch node ringing is discussed, which showed that improper measurement can lead to a switch node ringing voltage that is higher than desired. The RC snubber design methods were introduced and examined, to reduce both the amplitude and the ringing frequency of the switch node voltage to acceptable levels. Moreover, this application note showed that the result of adding a boot resistor slows down the turn-on of the high-side MOSFET and reduces the associated rising edge of the SW node voltage. however, the boot resistor does not affect the ringing frequency. Finally, this document has shown the affects on efficiency performance of the synchronous buck converter by using different snubber component values.

8 References

1. Texas Instruments, *High Efficiency 14A Synchronous Buck Converter with Eco-Mode™*, User's Guide
2. Philip C. Todd, Snubber Circuits: Theory, Design and Practice, Unitrode Power Seminar 900 Topic 2, May 1993.
3. Rudy Severns, Design of Circuits for Power Circuits, Application Note from Cornell Dubilier Electronics, Inc.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2017) to A Revision	Page
• Rewrite the abstract to include end equipment applications.	1

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