

# Integrated Step-Down Converter with SVID Interface for Intel® CPU Power Supply

## 1 Features

- Single chip to support Intel VR13.HC SVID POL applications
- Two outputs to support VCCANA (5.5 A) and P1V8 (4 A)
- D-CAP+™ Control for Fast Transient Response
- Wide Input Voltage (4.5 V to 15 V)
- Differential Remote Sense
- Programmable Internal Loop Compensation
- Per-Phase Cycle-by-Cycle Current Limit
- Programmable Frequency from 800 kHz to 2 MHz
- I<sup>2</sup>C System Interface for Telemetry of Voltage, Current, Output Power, Temperature, and Fault Conditions
- Over-Current, Over-Voltage, Over-Temperature protections
- Low Quiescent Current
- 5 mm × 5 mm, 35-Pin QFN, PowerPAD Package

## 2 Applications

- Low Current SVID Rails for Intel Server Platforms

## 3 Description

The TPS53820 device is D-CAP+ mode integrated step-down converter for low current SVID rails of Intel CPU power supply. It provides up to two outputs to power the low current SVID rails such as VCCANA (5.5 A) and P1V8 (4 A). The device employs D-CAP+ mode control to provide fast load transient performance. Internal compensation allows ease of use and reduces external components.

The device also provides telemetry, including input voltage, output voltage, output current and temperature reporting. Over voltage, over current and over temperature protections are provided as well.

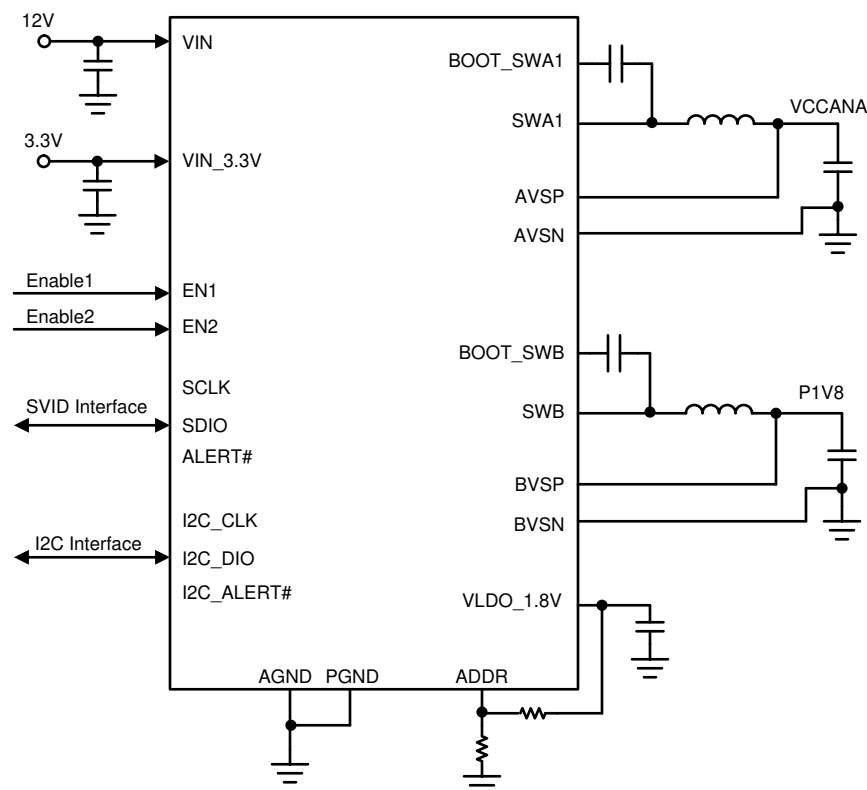
The TPS53820 device is packaged in a thermally enhanced 35-pin QFN and operates between –40°C and 125°C.

**Table 1. Device Information<sup>(1)</sup>**

| PART NUMBER | PACKAGE  | BODY SIZE (NOM) |
|-------------|----------|-----------------|
| TPS53820    | RWZ (35) | 5 mm × 5 mm     |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Figure 1. Simplified Application**



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE         | REVISION | NOTES            |
|--------------|----------|------------------|
| January 2020 | *        | Initial release. |

## 5 Device and Documentation Support

### 5.1 Trademarks

D-CAP+ is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 5.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 6.1 Package Option Addendum

### 6.1.1 Packaging Information

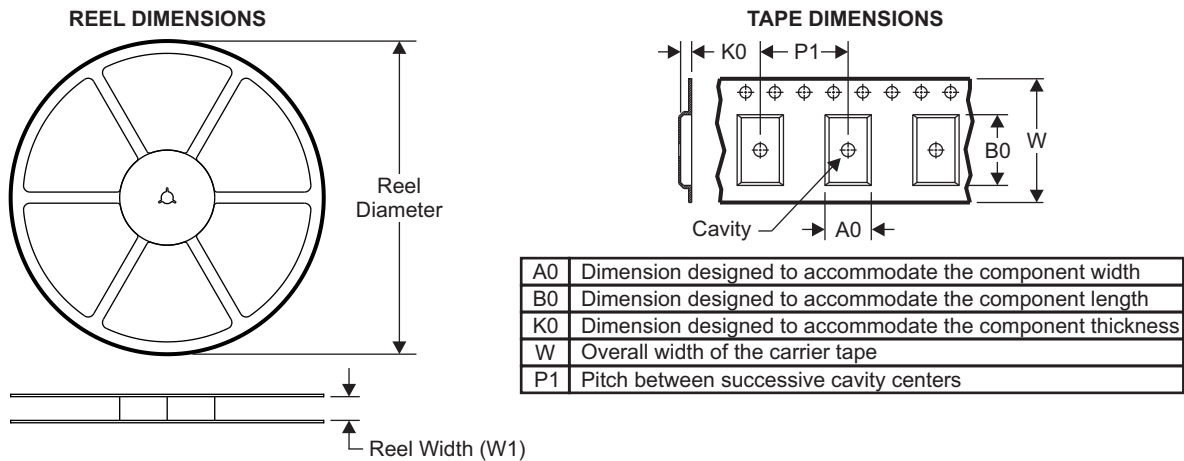
| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish <sup>(3)</sup> | MSL Peak Temp <sup>(4)</sup> | Op Temp (°C) | Device Marking <sup>(5)(6)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|---------------------------------|------------------------------|--------------|----------------------------------|
| TPS53820RWZR     | ACTIVE                | VQFN-HR      | RWZ             | 35   | 3000        | Green (RoHS & no Sb/Br) | NiPdAu                          | Level-2-260C-1 YEAR          | –40 to 125   | TPS53820                         |
| TPS53820RWZT     | ACTIVE                | VQFN-HR      | RWZ             | 35   | 250         | Green (RoHS & no Sb/Br) | NiPdAu                          | Level-2-260C-1 YEAR          | –40 to 125   | TPS53820                         |

- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.  
**TBD:** The Pb-Free/Green conversion plan has not been defined.  
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.  
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.  
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
- (4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

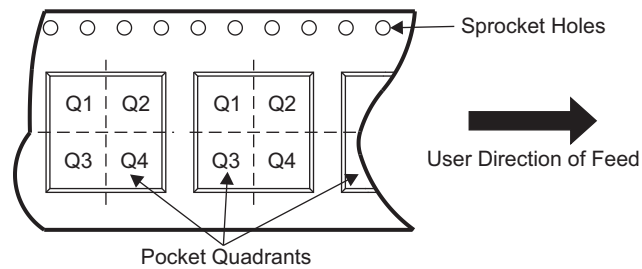
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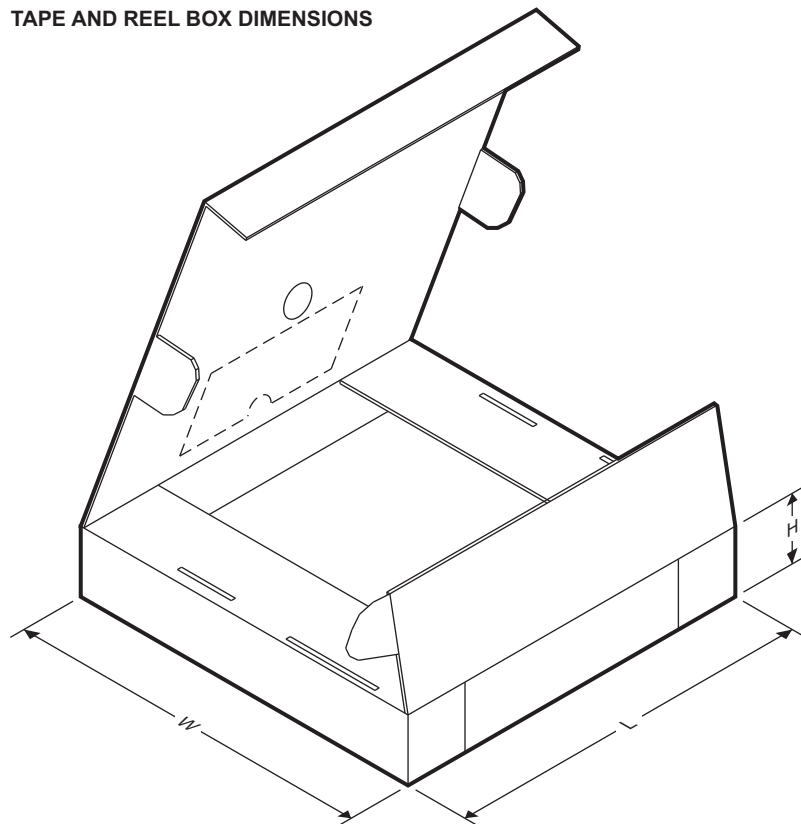
## 6.1.2 Tape and Reel Information



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS53820RWZR | VQFN-HR      | RWZ             | 35   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS53820RWZT | VQFN-HR      | RWZ             | 35   | 250  | 180.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |

**TAPE AND REEL BOX DIMENSIONS**


| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS53820RWZR | VQFN-HR      | RWZ             | 35   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS53820RWZT | VQFN-HR      | RWZ             | 35   | 250  | 210.0       | 185.0      | 35.0        |

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS53820RWZR     | ACTIVE        | VQFN-HR      | RWZ                | 35   | 3000           | RoHS & Green    | Call TI   NIPDAU                     | Level-2-260C-1 YEAR  | -40 to 125   | TPS<br>53820            | <a href="#">Samples</a> |
| TPS53820RWZT     | ACTIVE        | VQFN-HR      | RWZ                | 35   | 250            | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | TPS<br>53820            | <a href="#">Samples</a> |

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**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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