Application Report
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Designing a Simple and Low-Cost Flybuck Solution With the TPS54308

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ABSTRACT

In many applications, simple, low part-count, isolated power supplies working from an input voltage are needed. A popular solution to these requirements is an isolated buck power supply. This application report presents a simple and low-cost flybuck solution using the TPS54308 device. The basic operating principles of a flybuck converter are discussed, operating current and voltage waveforms are shown, and key design equations are derived. Lastly, a step-by-step design example is presented.

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1 Introduction

Isolated bias rails are common in many systems or subsystems, such as telecommunication equipment, medical equipment, and industrial factory automation. It is mandatory by safety standards to protect users from the hazardous voltage of a power supply, or the isolation is installed to break the ground loop interference for noise-sensitive applications.

In many cases, simple, low part count, isolated power supplies working from an input voltage are needed. This design solution is for when regulation may not be as important, but cost and board area are. A popular solution to these requirements is an isolated buck power supply, which is a synchronous buck converter, with the inductor replaced by a coupled inductor or flyback-type transformer. There is no need for an optocoupler or auxiliary winding because the secondary output closely tracks the primary voltage, resulting in smaller solution size and cost. The flybuck can support a simple, small, and cost effective power solution making it suitable as a flyback alternative.

This application report presents the basic operating principles of a flybuck converter, shows some typical operating current and voltage waveforms, and the key design equations are derived. The design example shows a step-by-step procedure for designing one nonisolated and two isolated outputs with the synchronous buck regulator TPS54308.

The TPS54308 device is a 4.5-V to 28-V input voltage range, 3-A switching regulator, that has two integrated switching FETs, internal loop compensation, and 5-ms internal soft start to reduce component count. By integrating the MOSFETs and employing the SOT-23 package, the TPS54308 achieves high-power density and offers a small footprint on the PCB.

2 Flybuck Converter Device Overview

2.1 Operation Description

An isolated buck converter is a synchronous buck converter with the inductor replaced by a coupled inductor or flyback-type transformer. The primary output is still regulated as in a sync buck. The secondary output is generated by a diode rectifying the secondary winding. Figure 1 shows an isolated buck converter with two outputs.

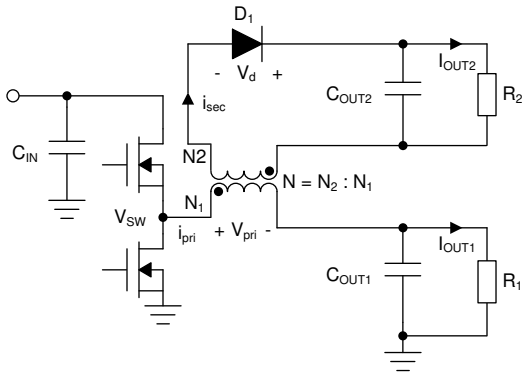

Figure 1. Isolated Buck Converter With Two Outputs

Figure 2 shows typical isolated buck operating waveforms. During T_{ON}, the high-side MOSFET is on, and the rectifier diode is turned off, because the reflected voltage across the secondary winding is negative. The isolated output capacitor C_{OUT2} is discharged, supplying the load current, and the primary side behaves identical to a buck regulator. During T_{OFF}, the low-side MOSFET is on, and the reflected voltage on the secondary winding turns positive, forcing the diode forward conducting. The current in the primary winding splits into two parts: one part continues to supply the primary output (the magnetizing current, i_m, similar to a buck converter inductor current), the other part starts to flow to the secondary output. The secondary current waveform is determined by the load, leakage inductance, and output capacitance.

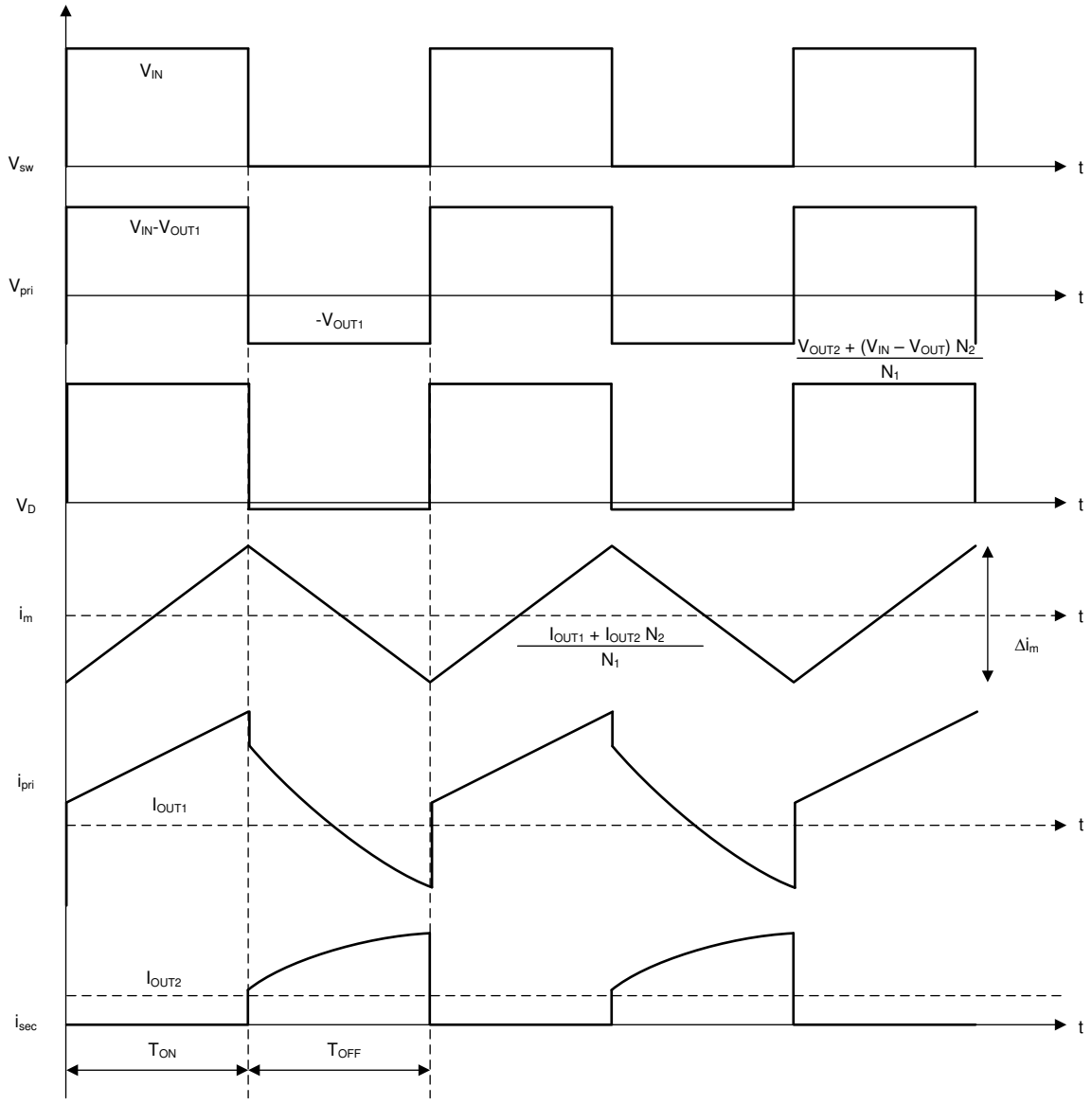

Figure 2. Simplified Isolated Buck Operating Waveforms

The primary output voltage is the same as a buck converter and is given by Equation 1:

$$V_{OUT1} = \frac{T_{on}}{T_{on} + T_{off}} V_{IN} = D \times V_{IN} \quad (1)$$

The secondary output voltage is given by Equation 2:

$$V_{OUT2} = V_{OUT1} \times \frac{N_2}{N_1} - V_F \quad (2)$$

where

- N_1 and N_2 are the turns of the primary winding and secondary winding
- V_F is the forward voltage drop of the secondary rectifier diode

The blocking voltage of the rectifier during T_{ON} is given by Equation 3:

$$V_D = V_{OUT2} + \frac{N_2}{N_1}\left(V_{IN} - V_{OUT1}\right) \quad (3)$$

2.2 Equations for Maximum Output Current

In practice, the transformer has more or less leakage inductance, which determines the ramp rate of the current in the secondary winding to charge the output capacitor. The simplified current waveforms in Figure 3 shows its relationship with leakage inductance. With lower leakage inductance, the current ramps up quickly to a high value, charging the output capacitor quickly. With the leakage inductance increasing, the current rises slowly, which can result in less energy being supplied to the output capacitance and less output voltage. The higher leakage inductance is the higher peak charging current obtained in secondary winding under the same output power rate. A high negative current is reflected in the primary winding at the same time. Leakage inductance along with duty cycle impacts not only the output voltage regulation, but also limits the output power resulting from the minimum low-side sink current limit. Therefore, the leakage inductance must be minimized and the maximum duty cycle must be chosen carefully to mitigate their impacts.

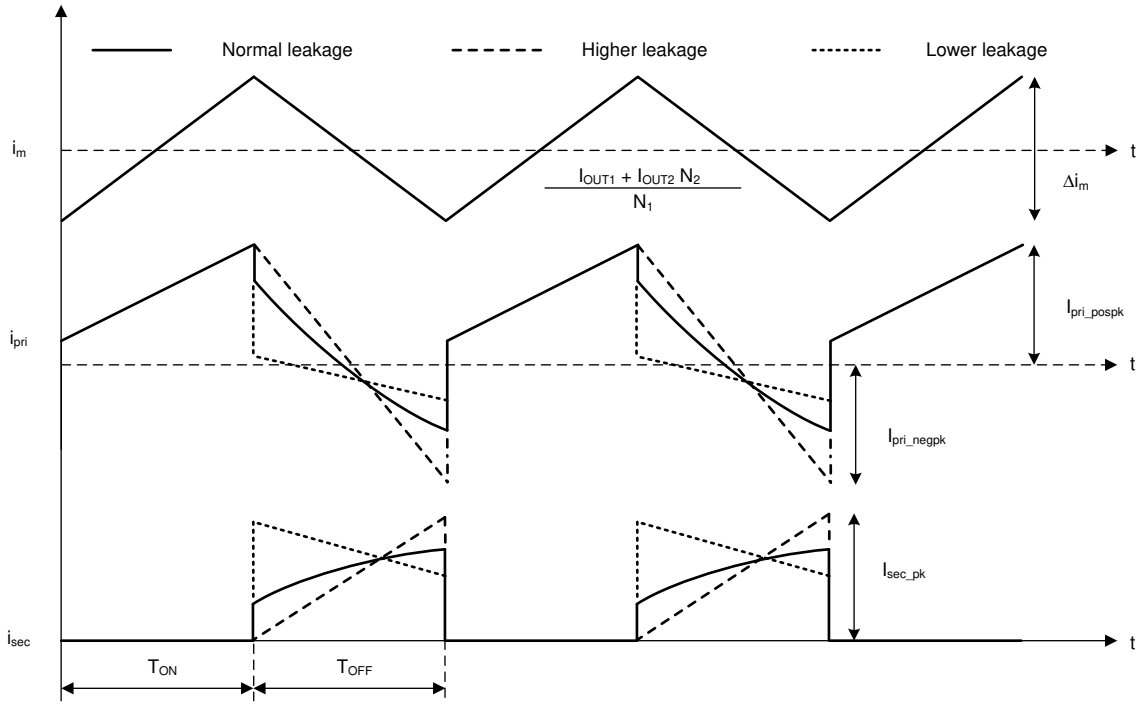

Figure 3. Current Waveforms Affected by Leakage Inductance

The winding and output currents have a relationship as shown in Equation 4 and Equation 5 on one cycle average basis.

$$I_{pri} = I_{OUT1} \quad (4)$$

$$I_{sec} = I_{OUT2} \quad (5)$$

The magnetizing current in the transformer that combines the two windings current is identical to a buck converter. Therefore, the magnetizing current ripple can be derived as in Equation 6.

$$\Delta i_m = \frac{(V_{IN} - V_{OUT1})}{L_{pri} \times f_{SW}} \frac{V_{OUT1}}{V_{IN}} = \frac{(V_{IN} - V_{OUT1})}{L_{pri}} \frac{D}{f_{SW}} \quad (6)$$

The positive primary winding and switching peak current during T_{ON} is given by Equation 7.

$$i_{SW\_pospk} = i_{pri\_pospk} = I_{OUT1} + \frac{N_2}{N_1} I_{OUT2} + \frac{\Delta i_m}{2} \quad (7)$$

Implementing the principle of charge balance to the secondary output capacitor, the secondary winding peak current can be approximately derived as Equation 8 for a higher leakage case, and Equation 9 for a normal leakage case.

Considering the worst case, the following equations are derived based on having higher leakage.

$$i_{sec\_pk} = \frac{2}{1-D} I_{OUT2} \quad (8)$$

$$i_{sec\_pk} = \frac{1+D}{1-D} I_{OUT2} \quad (9)$$

Then the negative primary winding peak current can be derived as Equation 10 for a higher leakage case, and Equation 11 for a normal leakage case.

$$i_{pri\_negpk} = -\frac{N_2}{N_1} i_{sec\_pk} + i_{pri\_pospk} - \Delta i_m = -\frac{N_2}{N_1} I_{OUT2} \left(\frac{1+D}{1-D}\right) - \frac{\Delta i_m}{2} + I_{OUT1} \quad (10)$$

$$i_{pri\_negpk} = -\frac{N_2}{N_1} I_{OUT2} \left(\frac{2D}{1-D}\right) - \frac{\Delta i_m}{2} + I_{OUT1} \quad (11)$$

In fact, we must ensure that during T_{ON} the positive primary winding peak current does not exceed the minimum high-side source current limit, $ILIM_{HS(min)}$, and that during T_{OFF}, the negative primary winding peak current does not exceed the minimum low-side sink current limit, $ILIM_{LSSOC(min)}$. Therefore the positive and negative primary winding peak current should meet that of Equation 12.

$$\begin{cases} i_{pri\_pospk} \le I_{LIM_{HS(min)}} \\ \left|i_{pri\_negpk}\right| \le I_{LIM_{LSSOC(min)}} \end{cases} \quad (12)$$

3 Design Flybuck With TPS54308

Figure 4 shows the design example with the typical flybuck circuit, using the synchronous buck regulator TPS54308 from TI.

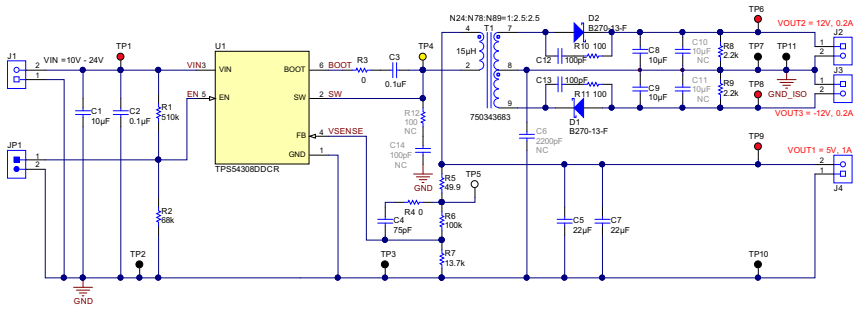

Figure 4. TPS54308 Two Output Isolated Buck Solution

Table 1 lists the design specification.

Table 1. Design Parameters

Design Parameter	Example Value
Input voltage range (V_{IN})	10 V to 24 V
Primary output voltage (V_{OUT1})	5 V
Positive isolated output voltage (V_{OUT2})	12 V
Negative isolated output voltage (V_{OUT3})	–12 V
Primary load current (I_{OUT1})	1 A
Positive isolated load current (I_{OUT2})	0.2 A
Negative isolated load current (I_{OUT3})	0.2 A
Switching frequency (f_{sw})	350 kHz

In this example, one primary output and two isolated outputs are obtained. We will begin with the buck converter component calculations and qualify the steps for the isolated configuration.

3.1 Primary Voltage and Turns Ratio

The primary-side, nonisolated output is set to 5 V for several considerations. First, the setting is below the minimum input voltage, 10 V, and the theoretical duty cycle varies from 20 to 50 percent at the full V_{IN} range, which is a balanced duty cycle during normal operation. Because the isolated outputs only have the off-time window to transfer energy, for a duty cycle that is too high, the secondary winding current will have a huge spike, which leads to poor regulation. Next, the turns ratio of the transformer is not too high to handle for the 5 V voltage level steps up to 12 V. Last, 5 V is one of the most common voltage levels in many applications. In this design, a transformer turns ratio (N_1:N_2:N_3) of 1:2.5:2.5 is selected (see Equation 13 and Equation 14).

$$V_{OUT2} = V_{OUT1} \times \frac{N_2}{N_1} - V_F = 12\ V \tag{13}$$

$$\left|V_{OUT3}\right| = V_{OUT1} \times \frac{N_3}{N_1} - V_F = 12\ V \tag{14}$$

In this design, the V_F is targeted at 0.5 V.

3.2 Feedback Resistor

With the expected primary voltage set point at 5 V, and V_{FB} = 0.596 V (typical), V_{OUT1} is calculated to be as in Equation 15:

$$V_{OUT1} = V_{FB} \times \left(1 + \frac{R_6}{R_7}\right) \tag{15}$$

Start with 100 kΩ for the upper resistor divider, R6 = 100 kΩ (see Equation 16).

$$R_7 = \frac{R_6 \times V_{FB}}{V_{OUT1} - V_{FB}} = 13.53\ k\Omega \tag{16}$$

Next choose R7 = 13.7 kΩ. The 49.9-Ω resistor, R5, is provided as a convenient location to break the control loop for stability testing.

3.3 Rectifier Diode

The rectifier diode D_1 and D_2, must meet the blocking voltage and maximum current requirements (see Equation 17, Equation 18, Equation 19, and Equation 20).

$$V_{D1} = \frac{N_2}{N_1} \times \left(V_{IN(max)} - V_{OUT1}\right) + V_{OUT2} = 59.5\ V \tag{17}$$

$$V_{D2} = \frac{N_2}{N_1} \times \left(V_{IN(max)} - V_{OUT1}\right) + V_{OUT3} = 59.5\ V \tag{18}$$

$$i_{D1\_pk} = \frac{2 \times I_{OUT2}}{1 - D_{max}} = 0.8\ A \tag{19}$$

$$i_{D2\_pk} = \frac{2 \times I_{OUT3}}{1 - D_{max}} = 0.8\ A \tag{20}$$

Considering the voltage spike and keeping some margin, as well as the less forward voltage drop, a schottky diode of 70 V or higher reverse voltage rating is required. A 70-V, 2-A diode is selected for each rectifier diode in this design.

3.4 Primary Inductance

For the TPS54308, the minimum high-side current is 4 A, and therefore the maximum magnetizing current ripple that can be tolerated is given by Equation 21:

$$\Delta i_m = 2 \times \left(I_{LIM_{HS(min)}} - \left(I_{OUT1} + \frac{N_2}{N_1} I_{OUT2} + \frac{N_3}{N_1} I_{OUT3}\right)\right) = 4\ A \tag{21}$$

Using Equation 21 for the maximum magnetizing current ripple calculation, the minimum primary inductance is given by Equation 22.

$$L_{pri(min)} = \frac{\left(V_{IN(max)} - V_{OUT1}\right)}{\Delta i_m \times f_{sw}} \frac{V_{OUT1}}{V_{IN(max)}} = 1.79\ \mu H \tag{22}$$

Too much high Δi_m may not be good for the efficiency and output voltage ripple. Assuming the 30% ripple of the rate output current of the device, then the optimized minimum primary inductance is given by Equation 23:

$$L_{pri} = \frac{\left(V_{IN(max)} - V_{OUT1}\right)}{0.3 \times 3 \times f_{sw}} \frac{V_{OUT1}}{V_{IN(max)}} = 12.6\ \mu H \tag{23}$$

We chose 15 µH for the primary inductor, therefore $\Delta i_{m(max)}$ = 0.75 A and $\Delta i_{m(min)}$= 0.48 A. Use Equation 7, Equation 10, and Equation 11 to check the positive and negative primary winding peak current (see Equation 24, Equation 25, and Equation 26.

$$i_{sw\_pospk(max)1} = I_{OUT1} + \frac{N_2}{N_1} I_{OUT2} + \frac{N_3}{N_1} I_{OUT3} + \frac{\Delta i_{m(max)}}{2} = 2.38\ A \tag{24}$$

$$i_{SW\_negpk(max)1} = -\left(\frac{N_2}{N_1} I_{OUT2} + \frac{N_3}{N_1} I_{OUT3}\right)\left(\frac{1+D_{max}}{1-D_{max}}\right) - \frac{\Delta i_{m(min)}}{2} + I_{OUT1} = -2.24\ A \tag{25}$$

$$i_{SW\_negpk(max)1} = -\left(\frac{N_2}{N_1} I_{OUT2} + \frac{N_3}{N_1} I_{OUT3}\right)\left(\frac{2D_{max}}{1-D_{max}}\right) - \frac{\Delta i_{m(min)}}{2} + I_{OUT1} = -1.24\ A \tag{26}$$

The primary output side is not always loaded, and without the primary load, the negative current is more obvious. So consider the worst case, I_{OUT1} = 0 A, check the positive and negative primary winding peak current again, as given by Equation 27, Equation 28, and Equation 29.

$$i_{sw\_pospk(max)2} = \frac{N_2}{N_1} I_{OUT2} + \frac{N_3}{N_1} I_{OUT3} + \frac{\Delta i_{m(max)}}{2} = 1.38\ A \tag{27}$$

$$i_{SW\_negpk(max)2} = -\left(\frac{N_2}{N_1} I_{OUT2} + \frac{N_3}{N_1} I_{OUT3}\right)\left(\frac{1+D_{max}}{1-D_{max}}\right) - \frac{\Delta i_{m(min)}}{2} = -3.24\ A \tag{28}$$

$$i_{SW\_negpk(max)2} = -\left(\frac{N_2}{N_1} I_{OUT2} + \frac{N_3}{N_1} I_{OUT3}\right)\left(\frac{2D_{max}}{1-D_{max}}\right) - \frac{\Delta i_{m(min)}}{2} = -2.24\ A \tag{29}$$

For the TPS54308, the minimum high-side source current limit, $ILIM_{HS(min)}$, is 4 A and the minimum low-side sink current limit, $ILIM_{LSSOC(min)}$, is 2.6 A. Therefore the positive and negative primary winding peak current can meet the current requirements with the normal leakage of a transformer.

3.5 Primary Turns

A coupled inductor or a flyback-type transformer is required for flybuck topology. Calculate the minimum primary turns for a flyback-type transformer using Equation 30.

$$N_1 = \frac{L_{pri} \times i_{SW\_pospk(max)1}}{B_{max} \times A_e} \tag{30}$$

where

- B_{max} is the maximum flux density.
- A_e is the effective core area of the chosen transformer.

In this design, the 750343683 inductor from Würth is selected for the transformer. Würth offers many other flyback-type transformers and ready-made coupled inductors, in a variety of standard values, saturation currents, and sizes.

3.6 Input and Output Capacitor

The input capacitor must be large enough to limit the input voltage ripple, see Equation 31.

$$C_{IN} \geq \frac{I_{OUT1} + \frac{N_2}{N_1} I_{OUT2} + \frac{N_3}{N_1} I_{OUT3}}{8 \times f_{SW} \times \Delta V_{IN}} = \frac{(1 + 2.5 \times 0.2 + 2.5 \times 0.2)A}{8 \times 350\ kHz \times 0.2\ V} = 3.6\ \mu F \tag{31}$$

Choosing ΔV_{IN}= 0.2 V gives a minimum of C_{IN}= 3.6 µF. Considering derating, one standard value 10-µF, 35-V capacitor is selected for better input ripple performance. Another 0.1µF capacitor has been added as a bypass capacitor to clear high-frequency noise.

Choosing ΔV_{OUT1}= 0.05 V gives a minimum of C_{OUT1}= 28.5 µF. Considering derating, two standard value 22-µF, 16-V capacitors are selected to maintain a small voltage ripple.

Energy is transferred from primary to secondary when the synchronous switch of the buck converter is on. The primary output capacitance is given by Equation 32:

$$C_{OUT1} \geq \frac{\left(\frac{N_2}{N_1} I_{OUT2} + \frac{N_3}{N_1} I_{OUT3}\right) \times D_{max}}{f_{SW} \times \Delta V_{OUT1}} = \frac{(2.5 \times 0.2 + 2.5 \times 0.2) \times 0.5}{350\ kHz \times 0.05\ V} = 28.5\ \mu F \quad (32)$$

The secondary output current is sourced by C_{OUT2} during T_{ON}. Ignoring the current transitions time in the secondary winding, the value of the secondary output capacitor can be calculated using Equation 33:

$$C_{OUT2} = \frac{I_{OUT2} \times D_{max}}{f_{SW} \times \Delta V_{OUT2}} = \frac{0.2 \times 0.5}{350\ kHz \times 0.1\ V} = 2.9\ \mu F \quad (33)$$

Choosing ΔV_{OUT2}= 0.1 V gives a minimum of C_{OUT2}= 2.9 µF. Considering derating, a standard value 10-µF, 25-V capacitor is selected, the same as the C_{OUT3}.

3.7 Pre-Load

Pre-load is necessary to prevent V_{OUT2} and V_{OUT3} from going too high at light load. The required pre-load current is usually set around 5 mA as a starting point, but it should be adjusted based on the circuit test and application requirements. In this design, the pre-load resistor is selected as 2.2 kΩ for ±12-V outputs. Users can use a Zener diode instead of the pre-load resistor to increase the transfer efficiency.

3.8 Factors Affecting Voltage Regulation

A flybuck converter regulates the primary output voltage with a closed-loop controller. The isolated output is achieved by rectifying the secondary winding of the coupled inductor when the low side MOSFET is on. Therefore the isolated output regulation is passive, affected by the winding leakage inductance, winding resistances, diode drop, and low-side MOSFET, RDSON.

3.9 Avoiding Low-Side Sink Current Limit

In a flybuck application, the isolated output power rate may be limited by the low-side sink current limit. Therefore, users must select design parameters elaborately to promote the isolated power rate. From Equation 25 and Equation 26, we know that the key factors affecting the negative primary winding peak current are D_{max}, $N2/N_1$, N_3/N_1, and the output current. The following tips are for trying to keep the margin:

1. Select a reasonable range of duty cycle. TI recommends a duty cycle ranging from 20% to 50% in most cases. Users can reduce D_{max} by setting a lower primary voltage or increasing the minimum input voltage to increase the negative current margin.
2. Minimize the leakage inductance. Leakage inductance is a crucial factor determining the ramp rate of the current in the secondary winding which charges the output capacitor. A nominal amount of leakage is within 1% of primary inductance.
3. Pick the correct turns ratio. A lower turns ratio (isolated side to non-isolated side) results in a lower reflected current in the primary winding.
4. Raise the non-isolated output power, which will reduce the negative winding peak current.
5. Reduce the isolated output power. This is the most direct way to lower the level of the negative current.

4 Experimental Results

Figure 5 through Figure 17 show the experimental test results of Figure 4.

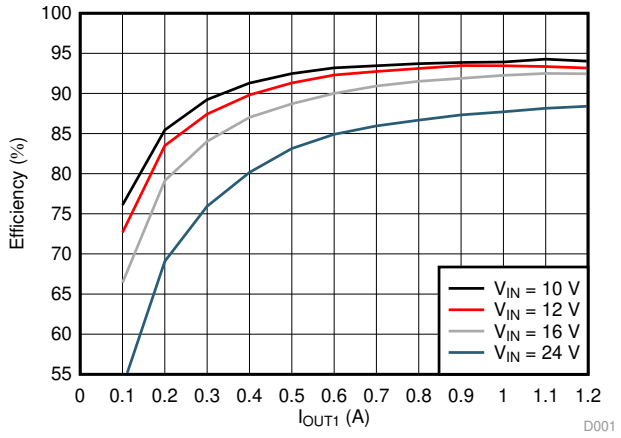

Figure 5. Efficiency vs I_{OUT1} (I_{OUT1} = 0 A, I_{OUT2} = 0 A)

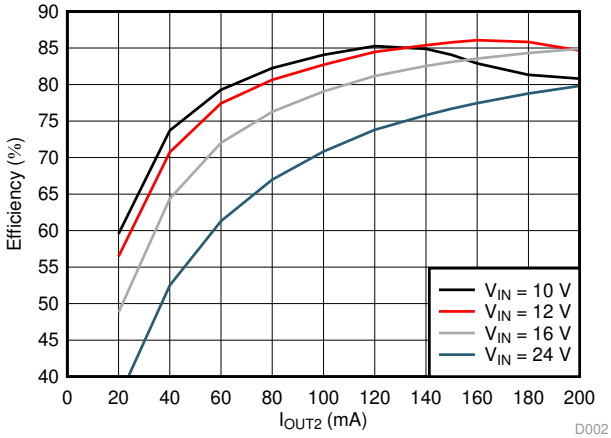

Figure 6. Efficiency vs I_{OUT2} (I_{OUT1} = 0 A, I_{OUT3} = 0 A)

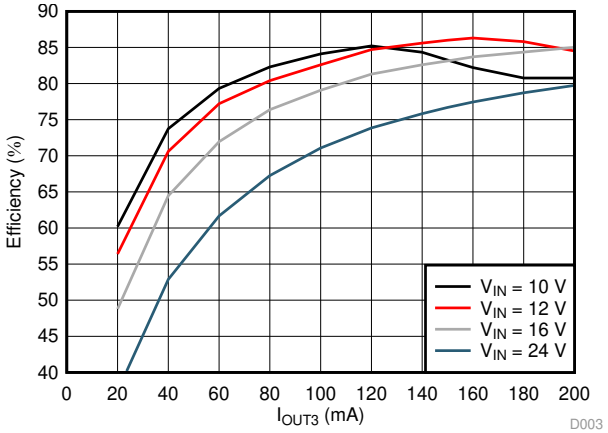

Figure 7. Efficiency vs I_{OUT3} (I_{OUT1} = 0 A, I_{OUT2} = 0 A)

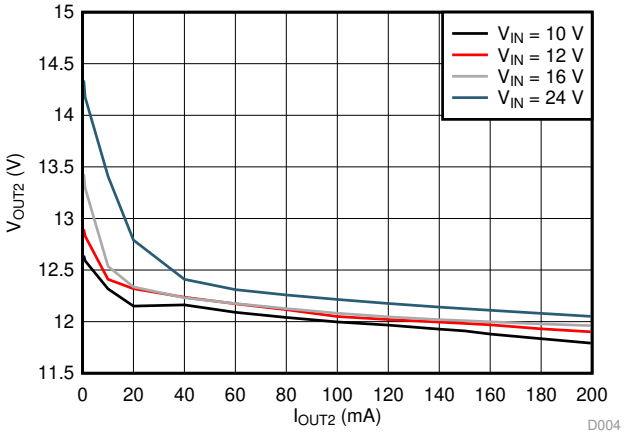

Figure 8. V_{OUT2} Regulation vs I_{OUT2} (I_{OUT1} = 0 A, I_{OUT3} = 0 A)

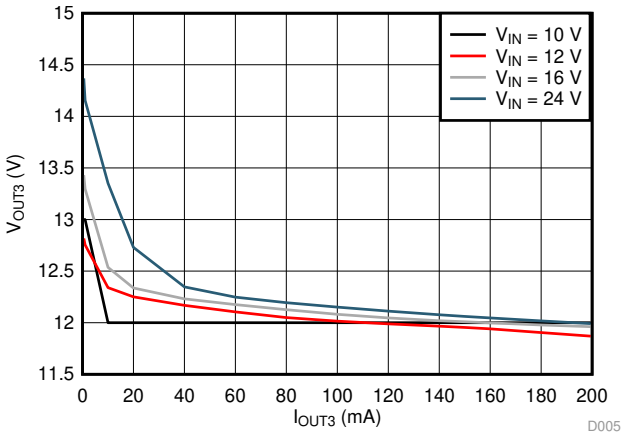

Figure 9. V_{OUT3} Regulation vs I_{OUT3} (I_{OUT1} = 0 A, I_{OUT2} = 0 A)

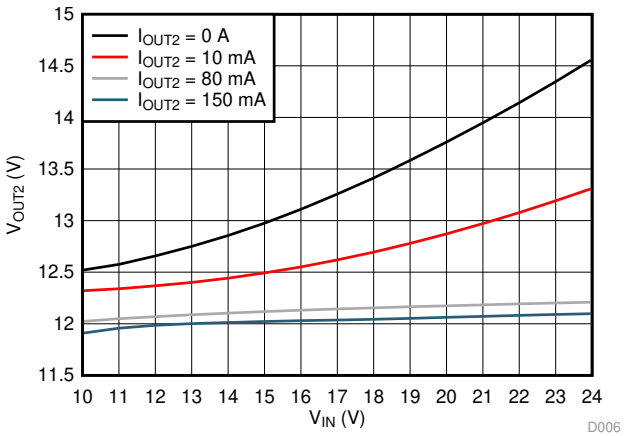

Figure 10. V_{OUT2} Regulation vs V_{IN} (I_{OUT1} = 0 A, I_{OUT3} = 0 A)

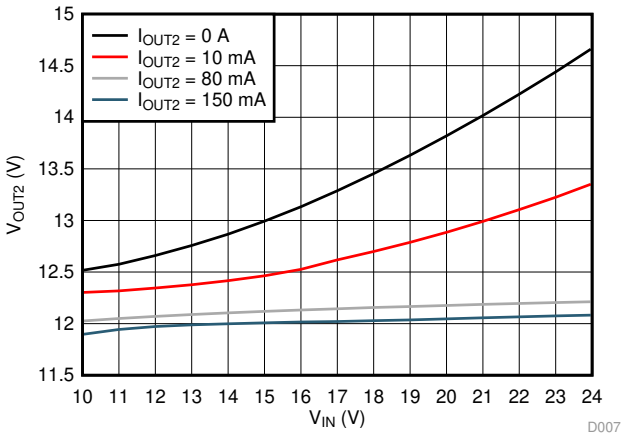

Figure 11. V_{OUT3} Regulation vs V_{IN} (I_{OUT1} = 0 A, I_{OUT2} = 0 A)

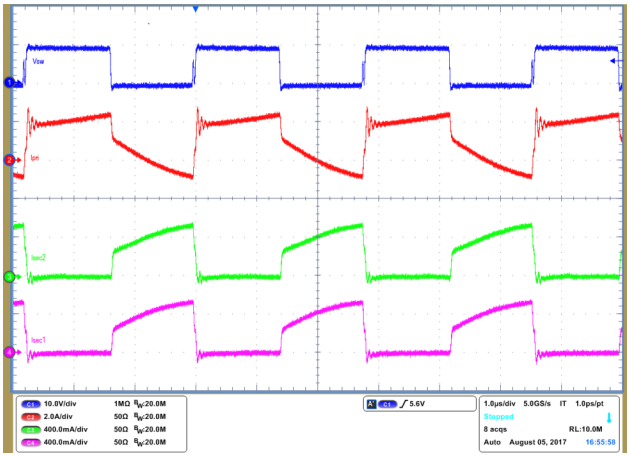

Figure 12. Steady State Waveforms (V_{IN} = 10 V, I_{OUT1} = 1 A, I_{OUT2} = 0.2 A, and I_{OUT3} = 0.2 A)

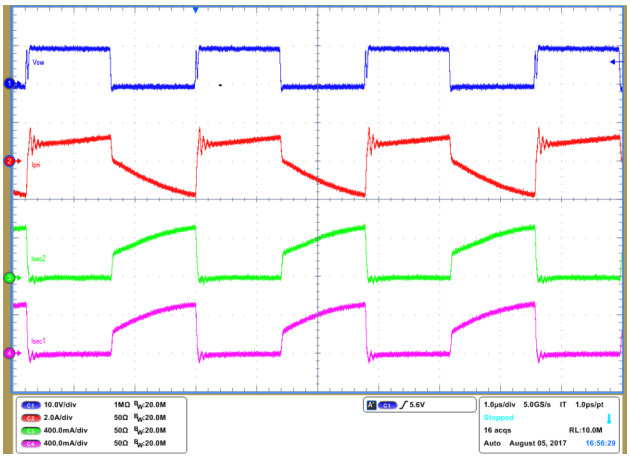

Figure 13. Steady State Waveforms (V_{IN} = 10 V, I_{OUT1} = 0 A, I_{OUT2} = 0.2 A, and I_{OUT3} = 0.2 A)

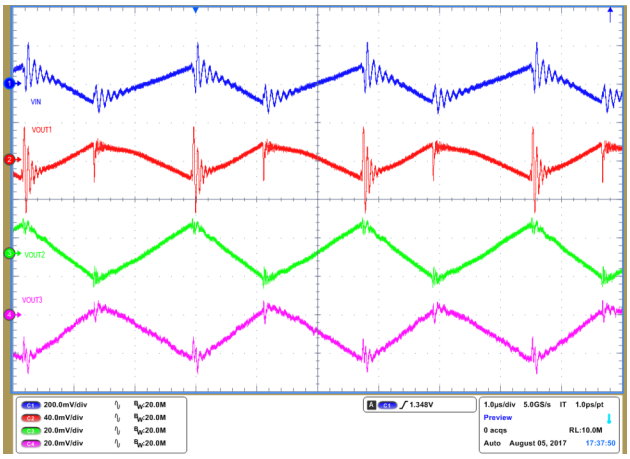

Figure 14. Ripple Voltage Waveforms (V_{IN} = 10 V, I_{OUT1} = 1 A, I_{OUT2} = 0.2 A, and I_{OUT3} = 0.2 A)

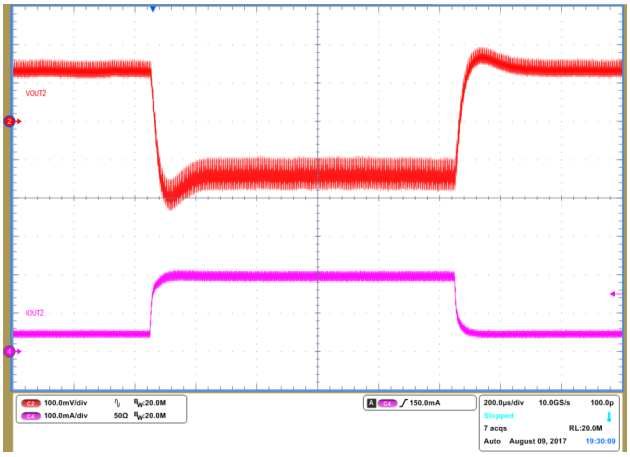

Figure 15. Load Step Response 50 mA to 200 mA (V_{IN} = 10 V, I_{OUT1} = 0 A, and I_{OUT3} = 0 A)

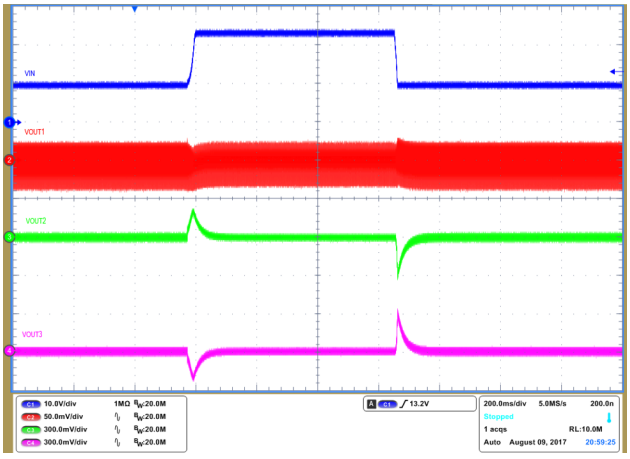

Figure 16. Line Step Response 10 V to 24 V (I_{OUT1} = 1 A, I_{OUT2} = 0.2 A, and I_{OUT3} = 0.2 A)

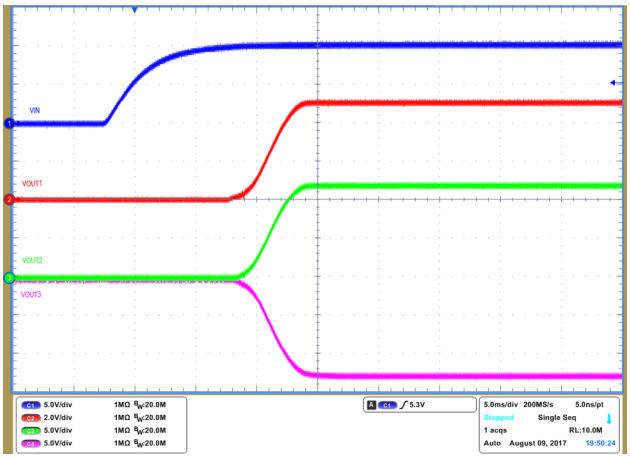

Figure 17. Power Up (V_{IN} = 10 V, I_{OUT1} = 1 A, I_{OUT2} = 0.2 A, and I_{OUT3} = 0.2 A)

5 Conclusion

This application report presented the operating principles of a flybuck converter, showed typical operating current and voltage waveforms, and provided a detailed, step-by-step design example which explained how to select the external components. Data and waveforms tested based on the example design show that the flybuck can support a simple, small, and cost effective power solution, making it suitable as a flyback alternative, and the TPS54308 makes the advantage more obvious.

6 References

- Texas Instruments, TPS54308: 4.5-V to 28-V Input, 3-A Output, Synchronous 350-kHz FCCM Step-Down Converter in SOT23 Package , data sheet
- Texas Instruments, Designing an Isolated Buck (Flybuck) Converter, application report
- Texas Instruments, Design a Flybuck Solution With Optocoupler to Improve Regulation Performance Create an Inverting Power Supply, application report
- Texas Instruments, Creating a Split-Rail Power Supply With a Wide Input Voltage Buck Regulator, application report

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2017) to A Revision **Page**

- Changed Equation 6 to Equation 21 for the maximum magnetizing current ripple calculation in Section 3.4section 7
- Changed $I_{pri(min)}$, $I_{pri}$to $L_{pri(min)}$, L_{pri}in Equation 22, 23. 7
- Changed the values of Equation 24, 27 8
- Changed Change ΔV_{OUT1} to ΔV_{OUT2}in Section 3.6section 9

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