Application Report
SLVA109 – December 2001

Designing With the TPS54310 Synchronous Buck Regulator

Brian King *Power Management Products*

ABSTRACT

The SWIFT™ TPS54310 externally compensated synchronous buck regulator makes designing a power solution quick and easy. The *SWIFT Designer* software tool is a resource that can greatly reduce design time by providing a complete power supply solution with only a few clicks of a mouse. The design methods presented in this application note are similar to the design methods used by the *SWIFT Designer* software. The *SWIFT Designer* software is available for download at the TI web site. This application report provides step-by-step instructions for generating a design using the SWIFT TPS54310 externally compensated, 3-A, synchronous buck regulator.

Contents

Figures

Tables

SWIFT is a trademark of Texas Instruments

Introduction

This application note provides systematic instructions for generating a power supply design using the TPS54310 externally compensated SWIFT synchronous buck regulator. The TSP54310 is part of the 3-A, low input voltage SWIFT product family. Other devices in this product family include the TPS54311/2/3/4/5/6 fixed output voltage, internally compensated regulators. The TPS54310 offers an advantage over the internally compensated SWIFT devices in that the choice of output filter components is not nearly as limited. However, this advantage comes with the trade-off that more components are required to stabilize the feedback loop. If board space or component count is a significant concern, an internally compensated TPS5431x may provide a more attractive solution.

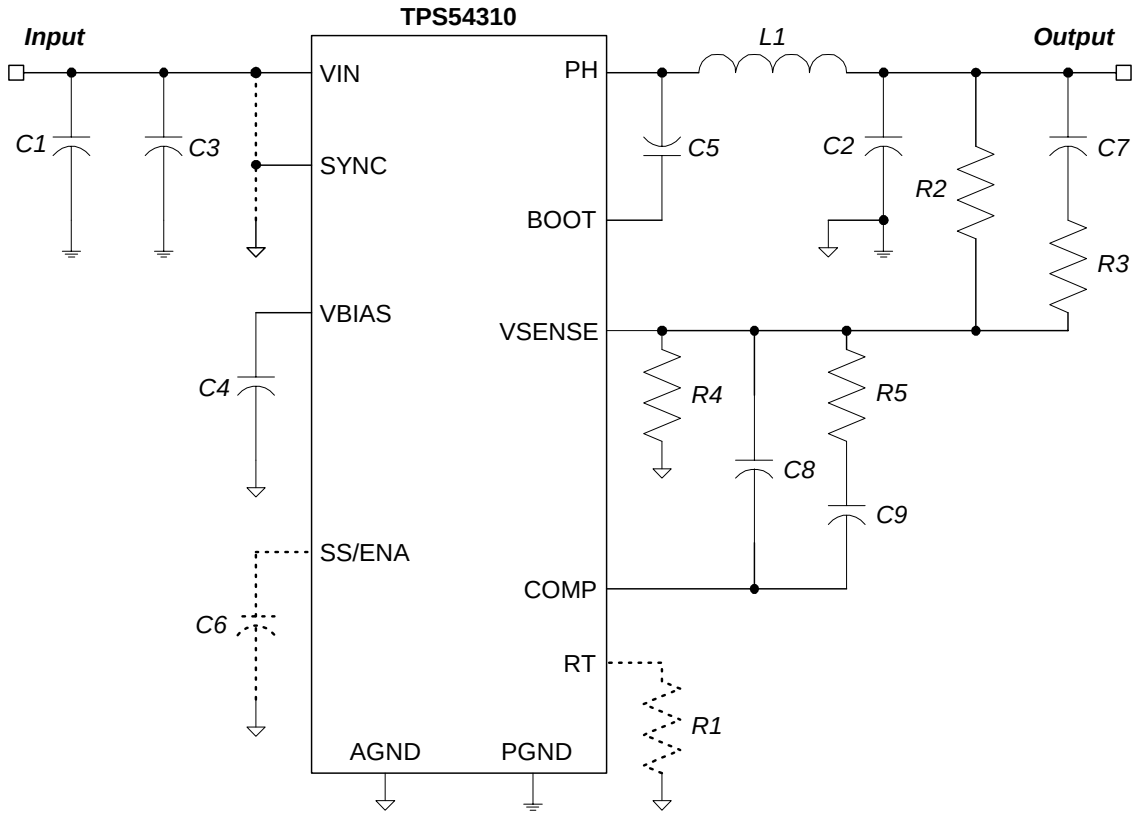

Figure 1. Typical Schematic

Internal Compensation vs External Compensation

Before designing with the TPS54310, investigate the possibility of using an internally compensated SWIFT regulator (TPS5431x). An internally compensated regulator requires fewer external components and consumes less board space. Designing a power supply with an internally compensated regulator is simple, and can be accomplished with either the *SWIFT Designer* software, or by using the step-by-step instructions given by Texas Instruments application report SLVA111. In design situations where an internally compensated SWIFT regulator cannot be used, the TPS54310 provides a solution to fill the gap.

There are two main reasons why it may not be possible to generate an internally compensated design for a particular application. The first reason is that the internally compensated regulators are only available with fixed output voltages. Table 1 provides a list of internally compensated, 3-A, SWIFT devices. The TPS54310, however, provides an adjustable output voltage. In applications where nonstandard output voltages are required, it may be necessary to use the TPS54310.

The second reason that an internally compensated regulator may not provide the best solution is that internally compensated regulators limit the choice of output inductors and output capacitors. In some situations, the availability or cost of the output inductor and/or output capacitor(s) may prohibit the use of an internally-compensated regulator. In applications such as these, the versatility of the TPS54310 may provide a better solution.

Table 1. Internally Compensated 3-A SWIFT™ Devices

Device	Output Voltage
TPS54311	0.9 V
TPS54312	1.2 V
TPS54313	1.5 V
TPS54314	1.8 V
TPS54315	2.5 V
TPS54316	3.3 V

Design Procedure

The procedure for designing with the TPS54310 is very similar to the TPS5431x internally compensated SWIFT design procedure. Only one additional step (selecting the compensation components) is required. A complete power supply design can be accomplished by performing the following six steps:

1. Select a switching frequency.
2. Select the input filter components.
3. Select the output filter components.
4. Select the compensation components.
5. Select the bias and bootstrap capacitors.
6. Select a slow start time.

Step One: Select a Switching Frequency

The switching frequency can be fixed at 350 kHz or 550 kHz without using any external components. To set the switching frequency to 350 kHz, simply pull the SYNC pin to ground. For a 550 kHz switching frequency, the SYNC pin should be connected to the input voltage. Using the SYNC pin to set the switching frequency results in a frequency accuracy of +/- 20%.

If a more precise switching frequency or a switching frequency other than 350 kHz or 550 kHz is desired, the switching frequency can be programmed by connecting an external resistor (R1 in Figure 1) between the RT pin and ground. The switching frequency can be programmed to any value between 280 kHz and 700 kHz by selecting R1 from the graph in Figure 2. When setting the frequency through this method, the SYNC pin should be left open. Using a 100-kΩ resistor for R1 results in a 500 kHz switching frequency with an accuracy of +/- 8%.

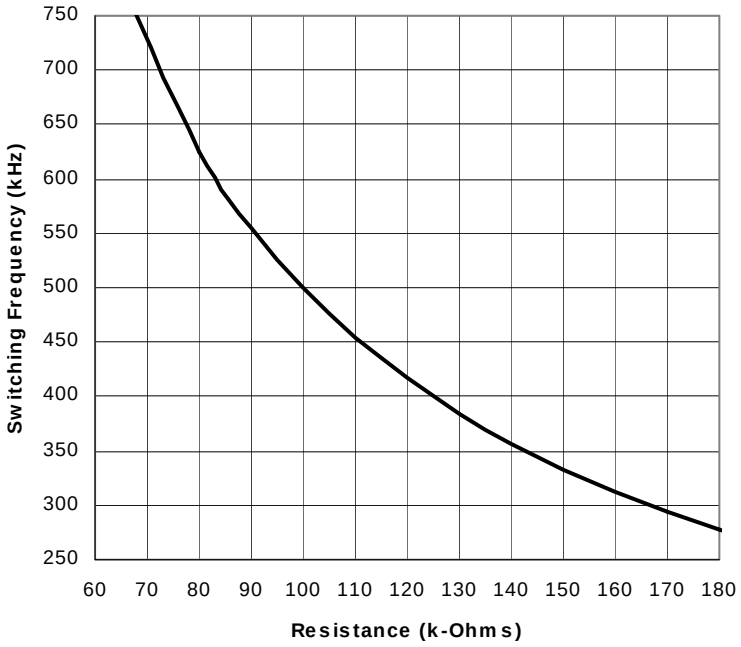

Figure 2. Switching Frequency Trimming Resistor Selection

Step Two: Select an Input Capacitor

The TPS54310 input requires a decoupling capacitor and a bulk input capacitor.

Input Decoupling Capacitor

The input decoupling capacitor (C3 in Figure 1) is needed to attenuate high frequency noise on the input of the device. The decoupling capacitor should be a ceramic capacitor in the range of 1 μF to 10 μF. A 10-μF, 10-V, 1210, X5R (or X7R) capacitor is recommended. This capacitor needs to be located as close as possible to the IC to be fully effective.

Bulk Input Capacitor

The purpose of the bulk input capacitor (C1 in Figure 1) is to reduce the ripple voltage on the input bus. Depending on the application, a 10-μF ceramic decoupling capacitor may provide enough filtering, and a bulk input capacitor may not be required.

To determine if a bulk capacitor is needed, first determine what the maximum allowable input ripple voltage is for the application. To ensure proper operation of the TPS54310, the maximum input ripple voltage should not exceed 300 mV_{pp}. Next, calculate the expected worst case input ripple voltage with only a 10-µF ceramic capacitor using Equation 1. If the value calculated by Equation 1 is greater than the maximum allowable input ripple voltage, then a bulk input capacitor is required.

Equation 1

$$\Delta V_{IN} = \frac{0.25 \cdot I_{OUT(MAX)}}{10\mu F \cdot F_{SW}}$$

Where:

ΔV_{IN} is the maximum peak-to-peak input ripple voltage without a bulk capacitor.

$I_{OUT(MAX)}$ is the maximum dc load current.

F_{SW} is the selected switching frequency.

The bulk input capacitor stores additional energy that keeps the input voltage from drooping too much when the TPS54310 draws a pulse of current during the on time of the topside MOSFET. Larger bulk input capacitors result in less of a voltage droop. The voltage drop across the equivalent series resistance (ESR) of the bulk capacitor also adds to the input ripple voltage. As a result, the bulk capacitor should be a relatively high valued capacitor with a low ESR. Aluminum electrolytic, tantalum, POSCap, and Oscon capacitors all work well as bulk input capacitors.

Equation 2 can be used to estimate the maximum input ripple voltage for a specific bulk input capacitor. If a particular bulk capacitor results in too high of an input ripple voltage, multiple capacitors can be used in parallel.

Equation 2

$$\Delta V_{IN} = \frac{0.25 \cdot I_{OUT(MAX)}}{C_{BULK} \cdot F_{SW}} + I_{OUT(MAX)} \cdot ESR_{MAX}$$

Where:

ΔV_{IN} is the maximum peak-to-peak input ripple voltage without a bulk capacitor.

$I_{OUT(MAX)}$ is the maximum dc load current.

F_{SW} is the selected switching frequency.

C_{BULK} is the selected bulk capacitance.

ESR_{MAX} is the maximum ESR of the selected bulk capacitor.

The voltage and current ratings of the bulk capacitor must also be checked. The maximum voltage across the bulk capacitor can be estimated using Equation 3. The maximum RMS current in the bulk input capacitor can be estimated using Equation 4. Ensure that the voltage and RMS current rating of the selected bulk input capacitor are not exceeded.

Equation 3

$$V_{CIN(MAX)} = V_{IN(MAX)} + \frac{\Delta V_{IN}}{2}$$

Where:

$V_{CIN(MAX)}$ is the maximum voltage across the bulk capacitor.

$V_{IN(MAX)}$ is the maximum input voltage.

ΔV_{IN} is the peak-to-peak input ripple voltage calculated by Equation 2.

Equation 4

$$I_{CIN,RMS(MAX)} = \frac{I_{OUT(MAX)}}{2}$$

Where:

$I_{CIN,RMS(MAX)}$ is the maximum RMS current in the bulk capacitor.

$I_{OUT(MAX)}$ is the maximum dc load current.

Step Three: Select the Output Filter Components

Two components must be selected for the output filter: an output inductor (L1 in Figure 1) and an output capacitor(s) (C2 in Figure 1). Compared to internally compensated devices, the TPS54310 imposes much fewer restrictions on the selection of these two components.

Inductor Selection

When selecting an inductor, the inductor's RMS current and saturation current ratings must not be exceeded. The maximum RMS current in the inductor can be calculated using Equation 5. The maximum instantaneous current in the inductor can be calculated using Equation 6.

Select an inductor with an RMS current rating greater than the value calculated by Equation 5, and a saturation current rating greater than the value calculated by Equation 6.

Equation 5

$$I_{L(RMS,MAX)} = \sqrt{I_{OUT(MAX)}^{2} + \frac{1}{12} \cdot \left(\frac{\left(V_{IN(MAX)} - V_{OUT}\right) \cdot V_{OUT}}{V_{IN(MAX)} \cdot L_{OUT} \cdot F_{SW} \cdot 0.8} \right)^{2}}$$

Where:

$I_{L(RMS,MAX)}$ is the maximum RMS output inductor current.

$I_{OUT(MAX)}$ is the maximum dc load current.

$V_{IN(MAX)}$ is the maximum input voltage.

V_{OUT} is the output voltage.

L_{OUT} is the selected output inductance.

F_{SW} is the selected switching frequency.

Equation 6

$$I_{L(PEAK,MAX)} = I_{OUT(MAX)} + \frac{1}{2} \cdot \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \cdot V_{OUT}}{V_{IN(MAX)} \cdot L_{OUT} \cdot F_{SW} \cdot 0.8}$$

Where:

$I_{L(PEAK,MAX)}$ is the maximum instantaneous output inductor current.

$I_{OUT(MAX)}$ is the maximum dc load current.

$V_{IN(MAX)}$ is the maximum input voltage.

V_{OUT} is the output voltage.

L_{OUT} is the selected output inductance.

F_{SW} is the selected switching frequency.

Capacitor Selection

When selecting an output capacitor(s), three factors must be considered: the capacitor's dc voltage rating, the capacitor's ripple current rating, and the maximum output ripple voltage.

Verifying the output capacitor(s) dc voltage rating is simple. Simply ensure that the dc voltage rating is greater than the output voltage. It is a good idea to leave some margin (at least 10%) between the output voltage and the capacitor's voltage rating to account for ripple and transients.

The maximum output capacitor ripple current is calculated by Equation 7. Verify that the capacitor's ripple current rating is greater than the value calculated in Equation 7.

Regarding the output ripple voltage, first determine the maximum ripple voltage requirements of the application that will be using the TPS54310 output voltage. Then calculate the maximum allowable ESR using Equation 8. The selected capacitor should have a maximum ESR rating less than the value calculated by Equation 8 in order to ensure that the output ripple voltage does not exceed the application requirements. Variation of the ESR with temperature should also be considered.

To summarize, when selecting an output capacitor the following items must be checked:

1. Verify that the dc voltage rating is at least ten percent greater than the output voltage.
2. Verify that the ripple current rating is greater than the value calculated by Equation 7.
3. Verify that the maximum ESR is less than the value calculated by Equation 8.

Equation 7

$$I_{C(RMS,MAX)} = \frac{1}{\sqrt{12}} \cdot \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \cdot V_{OUT}}{V_{IN(MAX)} \cdot L \cdot F_{SW}} \cdot \frac{1}{N_C}$$

Where:

$I_{C(RMS,MAX)}$ is the maximum RMS output capacitor current.

$V_{IN(MAX)}$ is the maximum input voltage.

V_{OUT} is the output voltage.

L_{OUT} is the selected output inductance.

F_{SW} is the selected switching frequency.

N_C is the number of capacitors in parallel.

Equation 8

$$ESR_{MAX} = N_C \cdot \frac{\Delta V_{PK-PK(MAX)} \cdot V_{IN(MAX)} \cdot L_{OUT} \cdot F_{SW} \cdot 0.8}{\left(V_{IN(MAX)} - V_{OUT}\right) \cdot V_{OUT}}$$

Where:

ESR_{MAX} is the maximum allowable output capacitor ESR.

N_C is the number of capacitors in parallel.

$\Delta V_{PK\_PK(MAX)}$ is the maximum peak-to-peak output ripple voltage.

$V_{IN(MAX)}$ is the maximum input voltage.

V_{OUT} is the output voltage.

L_{OUT} is the selected output inductance.

F_{SW} is the selected switching frequency.

Step Four: Select the Compensation Components

Seven components (resistors and capacitors) are required for the feedback compensation. These components, as shown in the schematic of Figure 1, are R2, R3, R4, R5, C7, C8, and C9. While there are an infinite number of ways to design the compensation, the design procedure presented here assures a stable design with a relatively high bandwidth.

When designing the compensation, several factors need to be considered. The gain of the compensated error amplifier should never be limited by the amplifier itself. In addition, the compensated error amplifier should limit the ripple on the COMP pin of the TPS54310 to around 100 mV. Also, the total loop crossover frequency should be limited to less than one-eighth of the switching frequency, and the phase margin should be at least 45°.

The first step is to determine the maximum allowable bandwidth of the compensated error amplifier by using Equation 9. By keeping the bandwidth of the error amplifier below the value calculated by Equation 9, the ripple on the COMP pin is limited to 100 mV.

Equation 9

$$F_{BW} = F_{SW}^{2} \cdot \frac{0.1V \cdot N_C \cdot V_{IN(MAX)} \cdot L_{OUT}}{ESR_{MAX} \cdot \left(V_{IN(MAX)} - V_{OUT}\right) \cdot V_{OUT}}$$

Where:

F_{BW} is the maximum compensated error amplifier bandwidth.

F_{SW} is the selected switching frequency.

N_C is the number of output capacitors in parallel.

$V_{IN(MAX)}$ is the maximum input voltage.

L_{OUT} is the selected output inductance.

ESR_{MAX} is the maximum rated output capacitor ESR.

V_{OUT} is the output voltage.

Next, calculate the desired total loop crossover frequency using Equation 10. The value used for F_{BW} should be the value calculated by Equation 9 or 3 MHz, whichever is lower. (The 3-MHz bandwidth limit assures that the amplifier does not limit the gain of the compensated error amplifier.)

Equation 10

$$F_{CO} = \sqrt{\frac{F_{BW} \cdot ESR_{MAX}}{12.6 \cdot N_C \cdot L_{OUT}}}$$

Where:

F_{CO} is the desired total loop crossover frequency.

F_{BW} is 3 MHz or the value calculated by Equation 9, whichever is lower.

ESR_{MAX} is the maximum rated output capacitor ESR.

N_C is the number of output capacitors in parallel.

L_{OUT} is the selected output inductance.

Finally, calculate the values of the compensation components using Equation 11 through Equation 16.

The values of R2 and R4 should be selected first. These resistors determine the output voltage of the converter and should be 0.1% precision resistors. The value of R2 should be in the range of 10 kΩ to 50 kΩ. The value of R4 should then be selected that gives the desired output voltage. The output voltage can be calculated for any values of R2 and R4 by using Equation 11.

Next, select R3, R5, C7, C8 and C9 using Equation 12 through Equation 16. This set of equations shapes the total loop response to result in a typical crossover frequency in the range of 10 kHz to 70 kHz, and a typical phase margin in the range of 60° to 90°. These resistors should have a tolerance no greater than 1%. The capacitors in the compensation should be ceramic X7R with a tolerance no greater than 10%.

Equation 11

$$V_{OUT} = 0.891V \cdot \frac{R2 + R4}{R4}$$

Equation 12

$$C9 = \frac{1.6}{F_{CO} \cdot R2}$$

Where:

F_{CO} is one-eighth of the switching frequency, or the value calculated in Equation 10, whichever is lower.

Equation 13

$$R5 = \frac{\sqrt{L_{OUT} \cdot N_C \cdot C_{OUT}}}{C9}$$

Where:

L_{OUT} is the output inductance.

N_C is the number of output capacitors in parallel.

C_{OUT} is the capacitance of a single output capacitor.

Equation 14

$$C8 = \frac{1}{2 \cdot \pi \cdot R5 \cdot 10 \cdot F_{CO}}$$

Where:

F_{CO} is one-eighth of the switching frequency, or the value calculated in Equation 10, whichever is lower.

Equation 15

$$C7 = \frac{2 \cdot \sqrt{L_{OUT} \cdot N_C \cdot C_{OUT}}}{R2}$$

Where:

L_{OUT} is the output inductance.

N_C is the number of output capacitors in parallel.

C_{OUT} is the capacitance of a single output capacitor.

Equation 16

$$R3 = ESR \cdot \frac{C_{OUT}}{C7}$$

Where:

ESR is the ESR rating of a single output capacitor.

C_{OUT} is the capacitance of a single output capacitor.

Step Five: Select the Bias and Bootstrap Capacitors

Every TPS54310 application requires a bias capacitor (C4 in Figure 1) and a bootstrap capacitor (C5 in Figure 1). The bias capacitor should be a ceramic 0.1 μF, and should be placed between the VBIAS pin and analog ground. The bias capacitor should be physically located as close to the IC as possible. The bootstrap capacitor should be ceramic and in the range of 0.022 μF to 0.1 μF. The bootstrap capacitor should be connected between the BOOT pin and the PH pin.

Step Six: Select a Slow Start Time

The TPS54310 contains an internal slow start circuit that controls the rise time of the output voltage during start-up. The internal slow start time is set to 3.6 ms. Alternatively, the output voltage rise time can be extended beyond the internal slow start time by connecting a capacitor (C6 in Figure 1) between the SS/ENA pin and analog ground. The equation for selecting a slow start capacitor is given by Equation 17. Using either method, the slow start time is independent of input voltage, output voltage, and load current.

The slow start cycle begins once the input to the TPS54310 rises above the 3-V start-up threshold, or the enable pin is released from ground. With an internally controlled slow start, the output voltage then begins to rise in a linear fashion until it reaches the programmed output voltage level. If a slow start capacitor is used, there is an inherent time delay from the start of the slow start cycle to the time where the output voltage begins to rise. This time delay is dependent on the size of the slow start capacitor, and can be calculated by Equation 18.

Equation 17

$$C_{SS} = \frac{t_{SS} \cdot 5\mu A}{0.891V}$$

Where:

C_{SS} is the slow start capacitance in farads.

t_{SS} is the slow start time in seconds.

Equation 18

$$t_d = \frac{C_{SS} \cdot 1.2V}{5\mu A}$$

Where:

t_d is the slow start delay time in seconds.

C_{SS} is the slow start capacitance in farads.

Layout Considerations

All the components of a TPS54310 design should be kept as close together as possible. In particular, the decoupling and bootstrap capacitors should be located next to the pins of the IC. It is also a good idea to keep the etch associated with the power stage away from the compensation circuitry. The compensation circuitry should also be kept as close together as possible and located close to the IC. Try to minimize the area of any loops in the compensation layout.

The TPS54310 has two internal grounds (analog and power). Inside the TPS54310, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. The PowerPAD™ is tied internally to the analog ground. Noise injected between the two grounds can degrade the performance of the TPS54310, particularly at higher output currents. However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground planes are recommended. These two planes should tie together directly at the IC to reduce noise between the two grounds. The only components that should tie directly to the power ground plane are the input capacitor, the output capacitor, the input voltage decoupling capacitor, and the PGND pins of the TPS54310. The layout of the TPS54310 evaluation module is representative of a recommended layout for a 2-layer board. Documentation for the TPS54310 evaluation module can be found on the Texas Instruments web site under the TPS54310 product folder.

PowerPAD is a trademark of Texas Instruments

Alternative ground structures are also possible, as long as care is taken to minimize the ground noise. One alternative is to tie the analog and power ground together at the point of regulation (usually the output capacitor). The advantage of this ground structure is a slight improvement in the converter's load regulation. Using this method, a wide power ground should be used to limit the noise injected between the analog and power grounds. A primary source of this noise is the circulating current from the input capacitor. When laying out a board in this manner, try to place the input capacitor such that its ground current does not flow between the two ground connections.

Yet another grounding technique is to use one common ground plane for both analog and power grounds. This ground structure simplifies the layout process, but still requires caution. The power and analog ground connections to the IC must still be made as close as possible to the IC. In addition, any ground plane obstructions should not force the noisy power ground currents to flow by any of the sensitive control signal ground connections.

The PowerPAD device package helps the TPS54310 keep junction temperatures from becoming excessive, particularly at high load currents. To ensure that the regulator has good heat sinking capabilities, the PowerPAD layout guidelines provided by the data sheet should be followed.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265