

Optimize Output Filter on D-CAP2™ for Stability Improvement

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ABSTRACT

Buck converters using D-CAP2™ mode control scheme are used in applications such as personal electronics and industrial and automotive systems. D-CAP2 mode supports superior load transient response with high system bandwidth (F_{co}). Its internal ripple injector block allows for low equivalent series resistance (ESR)-type output capacitor usage and reinforces loop stability. Although D-CAP2 mode ensures stability without external compensation components, optimizing the output filter in the design stage maximizes stability results to meet local specifications. This application report shows how to visually interpret D-CAP2 mode control to improve stability.

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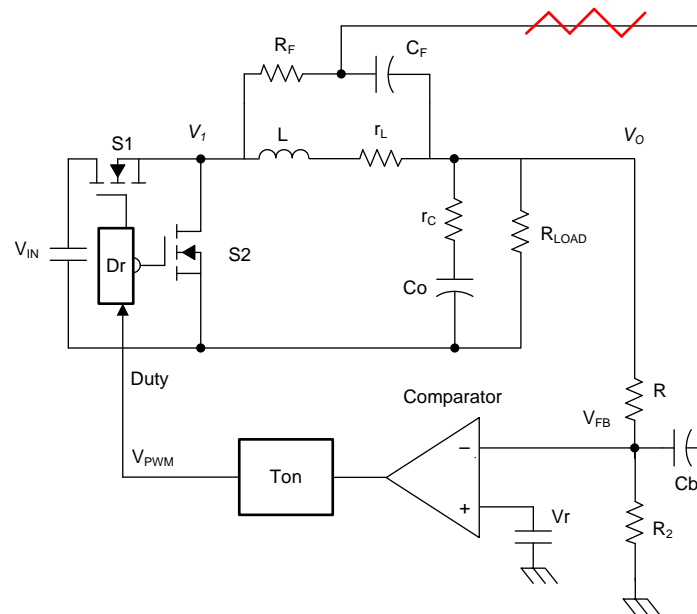
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1 D-CAP2™ Characteristics in the Frequency Domain

1.1 Internal Ripple Injector of D-CAP2™

Figure 1 shows how D-CAP2 mode control has an internal ripple injection block and how the block catches inductor current information. The R_F and C_F network across the inductor generate voltage ripple that is sent to the IC's feedback node (V_{FB}). This feedback results in high field effect transistor (FET) turnon of the internal comparator and allows for low ESR-type capacitor usage such as with the multi-layer ceramic capacitor (MLCC).



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Figure 1. Ripple Injection of D-CAP2™

1.2 Frequency Domain Analysis With Ripple Injector of D-CAP2™ Converter

The TPS54327, a D-CAP2 converter, has an internal, radio-controlled (RC) network for receiving ripple information from the switching node. When the sensed ripple voltage hits the internal reference, high-side FET is turned on and sustained on-time by an internal timing generator. In the frequency domain, the ripple injector generates additional zero which increases gain and boosts phase movement at its zero frequency around. Usually in voltage and current mode control, the phase movement rolls off around bandwidth (BW). The system may operate unstably if there isn't enough phase margin. Loop stability issues should be cleared in the design stage. Alternatively, Figure 2 shows how D-CAP2 mode control has different phase movement around bandwidth (crossover frequency). The output inductor and capacitor set corner frequency and produce 2 poles in the frequency domain. Around corner frequency, the phase margin drops rapidly if the ceramic capacitor is used as the output filter. The phase will then be boosted around bandwidth by internal zero which is made from the IC's ripple injector block.

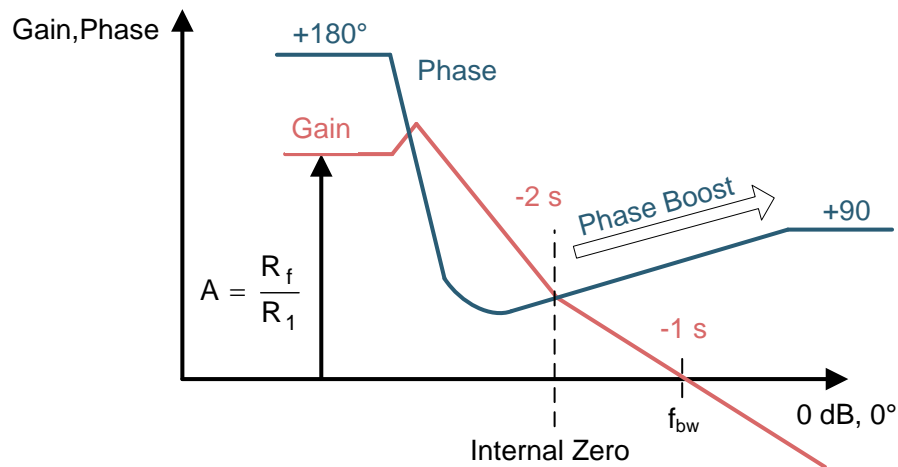


Figure 2. Gain and Phase Movement of D-CAP2™

Because of additional zero caused by the ripple injector, D-CAP2 easily compares the phase margin in the voltage and current mode control scheme. In some designs, the phase margin should be over a certain degree regardless of phase behavior in the frequency domain.

2 Improve Phase Margin by Visual Interpretation

2.1 Low V_{OUTPUT} and High Duty Cycle Condition

Table 1 shows the phase margin and system bandwidth (f_{bw}) results on the TPS54327 according to input voltage with the fixed $1.05 \cdot V_{OUT}$. The phase margin decreases when V_{IN} is reduced from $12 V_{IN}$ to $5 V_{IN}$. The output capacitor value is $44 \mu F$ and the inductor value is $1.5 \mu H$. The feedforward capacitor is not populated, and the load current is $3 A$.

Table 1. TPS54327 PM and BW Results According to V_{IN} With Fixed $1.05 V_{OUT}$

V_{INPUT} (V_{dc})	Bandwidth (KHz)	Phase Margin (degree)
12	219	31
10	216	28.3
8	216	28.2
6	216.7	26.9
5	216.7	18.9

Figure 3 shows how low V_{OUTPUT} has high system bandwidth over approximately 200 KHz and how the high duty cycle system causes phase drop around bandwidth. Phase drop at high frequency is caused by the IC's on-time delay.

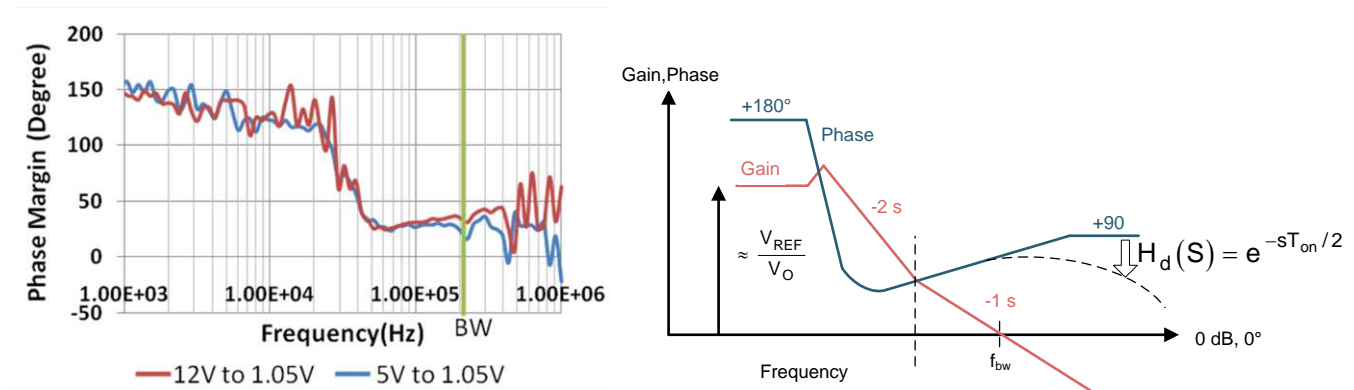


Figure 3. Phase Margin of the TPS54327 and Phase Drop Caused by On-Time Delay

When Input voltage is decreased from 12 V_{dc} to 5 V_{dc} with the fixed 1.05- V_{OUT} , the buck converter's duty cycle will increase, resulting in the IC's on-time causing phase delay around bandwidth following transfer function.

$$H_d(s) = e^{-sT_{\text{ON}}/2}$$

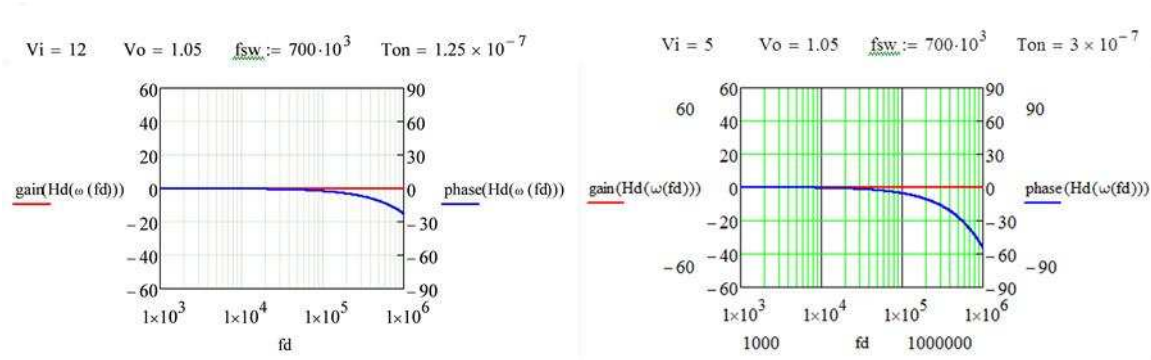


Figure 4. On-Time Versus Phase Delay of the TPS54327

Figure 4 shows how the Mathcad™ tool can help estimate how much phase delay exists in the system. Figure 4 also shows that the phase drop starts at approximately 50–60 KHz, at 5 V_{in} and 1.05 V_{out} , and gets 15°–20° phase delay at 200 KHz band. Improve delay in the design stage to get substantial phase margin.

2.1.1 Optimize Output Filter in Low V_{OUTPUT} and High Duty Cycle Condition

Previous tests show that a high duty cycle and low output condition, such as 5 V_{in} to 1.05 V_{out} , results in high bandwidth and low phase margin. Reduce bandwidth to avoid a phase drop that is caused by fixed on-time delay in a high frequency range. In D-CAP2 mode control, corner frequency (Fn) is mainly set by the output inductor and capacitor. Bandwidth can be decreased by increasing the L and C output value. However, this decrease may cause poor load transient response by increasing inductor value.

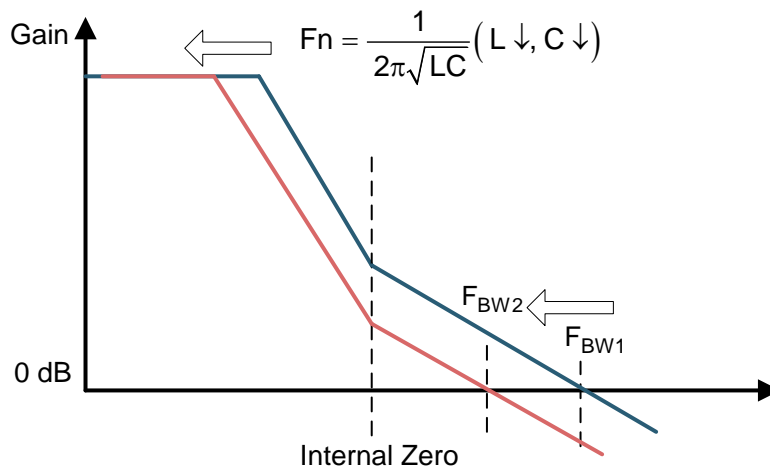


Figure 5. Reducing Corner Frequency (Fn) and Bandwidth

Figure 5 shows how the system bandwidth can be reduced by increasing the value of the output inductor and the capacitor value which sets corner frequency.

Table 2. TPS54327 PM and BW Results According to L, C in 5 V_{IN} to 1.05 V_{OUT} Condition

Output L,C	Bandwidth (KHz)	Phase Margin (degree)
1.5 uH, 44 uF (Default)	220 (F _{BW1})	19
2.2 uH, 44 uF	167	29
3.3 uH, 44 uF	153	30
2.2 uH, 66 uF	130	33
4.7 uH, 44 uF	118 (F _{BW2})	35

Table 2 shows that when bandwidth reduces from 220 KHz to 118 KHz by adjusting output L and C, phase margin is increased from 19° to 35°. Load transient response time will increase as the system bandwidth is reduced, and the inductor current will follow load current slowly if inductance is increased. Consider the effects of the time domain even though the system has a substantial phase margin.

2.2 High V_{OUTPUT} Condition

High V_{OUTPUT} conditions is another factor considered that affects the stability characteristic. Unlike in the case of low V_{OUTPUT} , the system will have low bandwidth if the absolute output voltage is increased. Figure 6 compares the system bandwidth between high and low output voltage case and shows the approximate DC gain of D-CAP2.

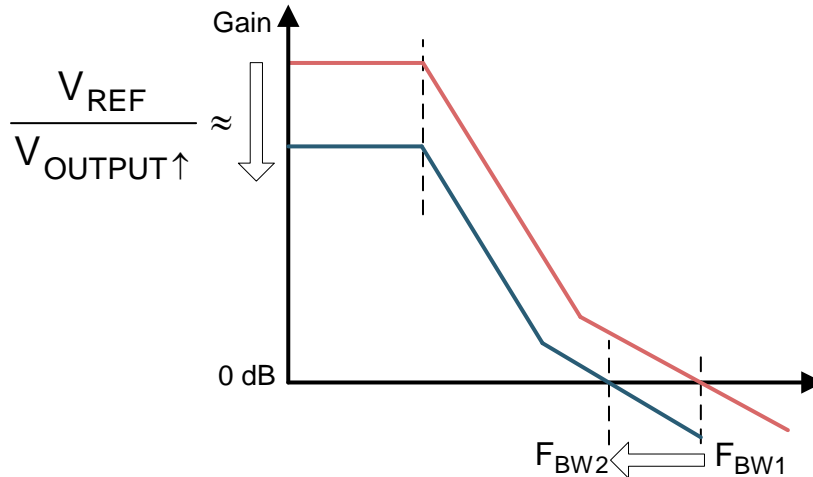


Figure 6. Output Voltage Level Versus Bandwidth

The converter, which has a high output voltage, will have low DC gain and low bandwidth.

Table 3 shows the results of the TPS54327 EVM using a 4.7- μ H output inductor and 44- μ F output capacitor. Input voltage is fixed at 12 V_{dc} .

Table 3. TPS54327 PM and BW Results According to V_{OUT} With Fixed 12 V_{IN}

Output Voltage (Vdc)	Bandwidth (KHz)	Phase Margin (degree)
1.05	133 (F_{BW1})	32
1.8	108	32
2.7	89	31
3.3	81	29.5
5	70 (F_{BW2})	27

Table 3 shows that phase margin also drops when system bandwidth is lower than 80 KHz. This drop means that the TPS54327's internal zero frequency from the ripple injector is higher than the bandwidth, and the phase-boosting effect cannot affect the result. The output filter needs to be redesigned to achieve the phase-boosting effect by internal zero of D-CAP2.

2.2.1 Optimize Output Filter in High V_{OUT} Condition

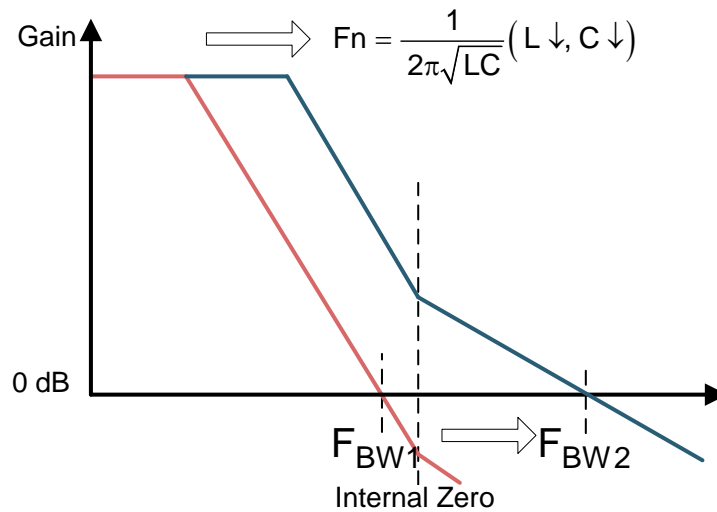


Figure 7. Increasing Corner Frequency (F_n) and Bandwidth

Figure 7 shows how the system bandwidth can be increased by reducing the value of the output inductor and capacitor. Achieve more of a phase-boosting effect by placing system bandwidth greater than internal zero frequency.

Table 4. TPS54327 PM and BW Results According to L, C in 12 V_{IN} to 5 V_{OUT} Condition

Output L,C	Bandwidth (KHz)	Phase Margin (degree)
4.7uH, 66uF	49	23
4.7uH, 44uF	70 (F_{BW2})	27
3.3uH, 44uF	92	33
2.2uH, 44uF	110	33
1.5uH, 44uF	135 (F_{BW1})	33

Table 4 shows the phase margin recovering when bandwidth is increased from a lower range. It can be assumed that the IC's internal zero is located around 90 KHz because that is the point that the phase margin jumps. Optimize system stability by redesigning output filter in high V_{OUT} condition as well.

3 Conclusion

D-CAP2 shows stable behavior in the loop stability but is sometimes faced with meeting specifications required by local systems. The design system must be more robust so that D-CAP2 control schemes can be optimized by the output filter design. By analyzing the IC's on-time and V_{OUT} level and bandwidth, a maximum phase margin can be achieved.

4 References

- Texas Instruments, [D-CAP2™ Frequency Response Model based on frequency domain analysis of Fixed On-Time with Bottom Detection having Ripple Injection Application Report](#)

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