Application Report
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Designing for Small-Size, High-Frequency Applications Using TPS546xx DC/DC Converters

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ABSTRACT

This application report describes the design procedure for a small-size, high-frequency application using SWIFT synchronous buck regulators. It shows that the compensation circuitry of the regulators, with the minimum size output filter and fast transient response, provides the 150-kHz unity gain bandwidth of the open feedback loop. The design is illustrated by the 6-A DDR memory, V_{TT} tracking regulator TPS54672. The regulator occupies only 1.33” x 0.445” x 0.3” board space including input and output filters. The schematic, bill of materials, and main performance curves complete the evaluation of the design example.

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Introduction

Integrated FET, SWIFT family regulators from Texas Instruments provide a simple and low cost solution in many industrial, computer, telecommunication and consumer applications. TI recommends using the SWIFT software designer tool to save time and to simplify the design for most generic applications. Meanwhile, there are some applications where the design is driven by minimum size and fast transient response. In this particular case, the regulator operates at maximum frequency with the low-value output inductor and low equivalent series resistance (ESR) output capacitor. SWIFT family synchronous buck regulators perfectly fit these applications. However, designing the feedback loop requires special attention because of high 150-kHz overall loop bandwidth, and maximum gain below crossover frequency needs to be provided. Special precautions need to be taken to assure both stability and good dynamic characteristics. This application report addresses the issue by using the TPS54672 tracking regulator for the termination voltage of the double data rate (DDR) memory as an example. Nevertheless, this design procedure and performance are valid for any 6-A SWIFT regulator.

The termination-voltage regulator tracks an external reference voltage with high accuracy and provides both source and sink capability for a load current. Figure 1 illustrates the basic principle of operation with this type of logic as the load.

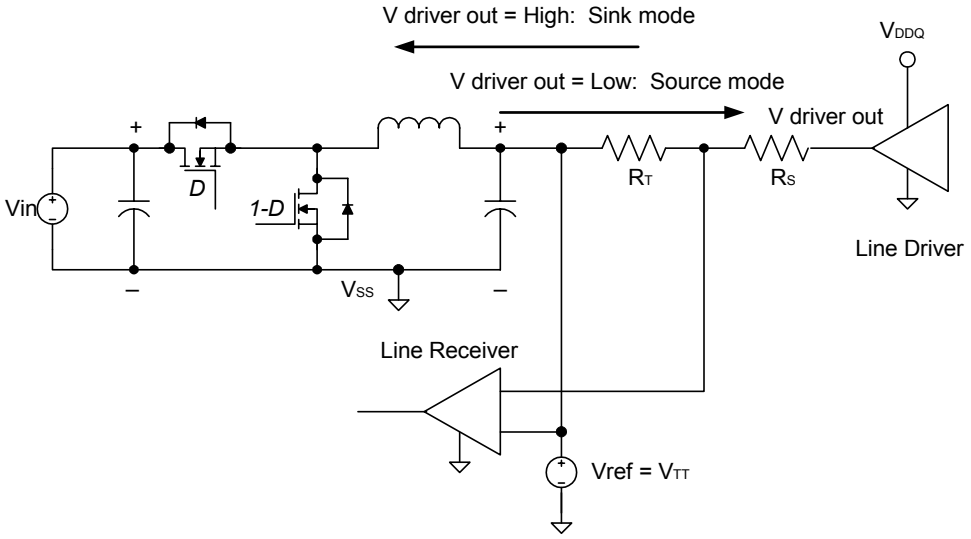


Figure 1. Two Operating Modes of the Termination Voltage Regulator

Depending on the output state of the line driver, the bus termination resistors R_T and series resistors R_S are connected either between the termination voltage V_{TT} and ground (source mode), or between the supply voltage V_{DDQ} and termination voltage V_{TT} (sink mode).

In the sink mode, the inductor current of a buck regulator is reversed. However, the switching processes are similar to a boost converter, and nothing changes in terms of the control circuitry operation and the feedback-loop frequency response. The same synchronous buck regulator analysis of stability is applied for both source and sink modes. The polarity change of the inductor current does not influence the conduction losses in a regulator if the absolute current value is the same. Meanwhile, the load-current transient analysis needs to take into account the current direction change. This must be accomplished by estimating the load current step as the sum of the absolute source and sink currents.

SWIFT Family of Synchronous Buck Regulators

The 6-A output current SWIFT family includes fixed-output TPS546XX regulators with internal compensation[1], the adjustable-output TPS54610 regulator with an external compensation[2], and the tracking regulator TPS54672[3]. Although the TPS54672 is specifically designed as the termination voltage power supply, it can be used in any application where the output voltage needs to be controlled by an external reference. The block diagram of the regulator is shown in Figure 2. Other SWIFT family regulators do not have access to the reference input of an error amplifier REFIN, but they have a combined slow/start and enable pin. They also have power good pin PWRGD instead of STATUS pin as in the case of TPS54672. TPS546XX regulators with the internal compensation do not have access to the COMP pin.

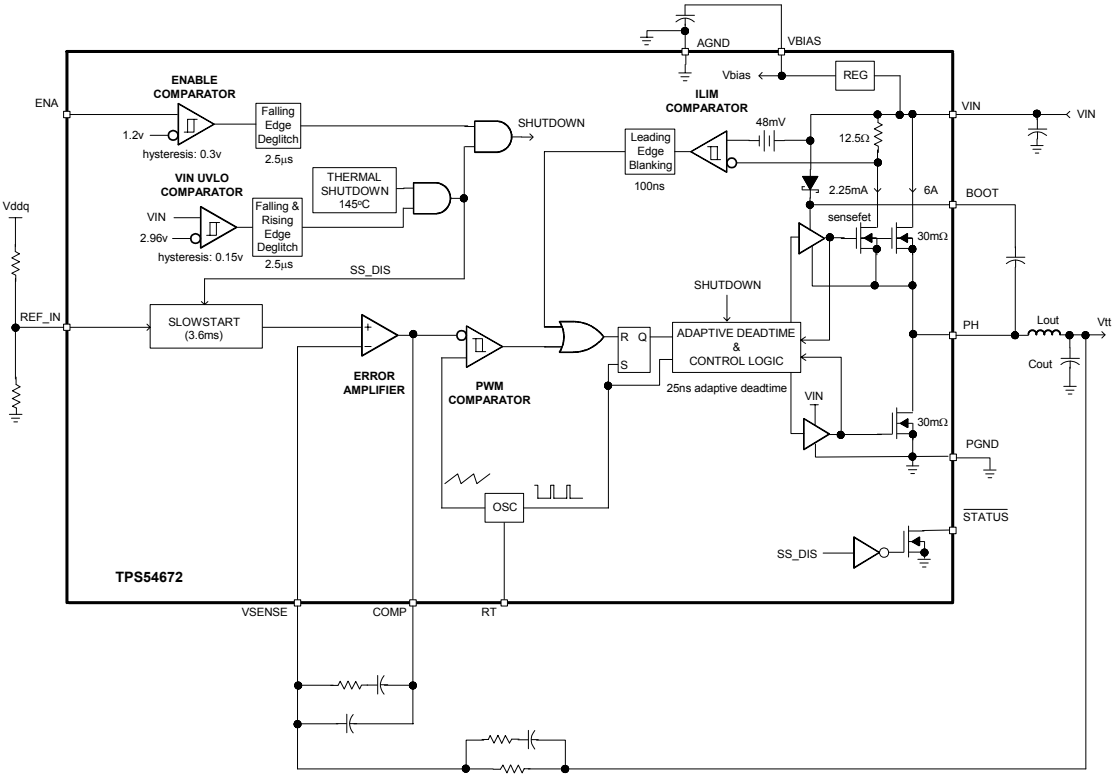


Figure 2. TPS54672 Block Diagram

The TPS54672 includes all the main features of the SWIFT TPS546XX family:

- 30-mΩ, 12-A peak current integrated FETs
- Input voltage range from 3 V to 6 V
- 280 kHz to 700 kHz fixed switching frequency set internally or by an external resistor
- PWM voltage-mode control with 5-MHz gain-bandwidth product and 1.4 V/μs output slew rate of an error amplifier
- Fast cycle-by-cycle peak current limit along with a thermal protection
- Input under voltage protection, enable pin, status indication pin
- Thermally enhanced 28-pin PWP package with the exposed PowerPad™

The detailed characteristics of the part can be found in the related SLVS397 data sheet[3].

Design Procedure

The design procedure shows how to use the TPS54672 regulator in an application where minimum size and fast transient response is critical. Although the highest allowable 700-kHz switching frequency has been selected, switching losses of TPS546XX regulators are below 0.1 W, so the high switching frequency does not increase the total power losses significantly. At the same time the high-frequency operation minimizes the size of the input and output filters. The input filter includes only two 10-μF ceramic capacitors for this application.

There are two main things to consider when designing for the fast transient response. First, an output filter needs to be optimized. Optimization includes proper inductor value and selection of output capacitors. If the inductor value is high, it takes longer time for the inductor to reach the new current level at transient. If the inductor value is too small, the overall peak to peak output voltage at transient could be even higher because of the increased ripple at the output capacitors. Optimized output filter selection is presented in detail in reference[4]. Table 1 shows the results for the required number of capacitors as the function of load-current step 2 x Io from the source current +Io to the sink current -Io. The optimal 0.56-μH inductor has been selected for this application based on the smallest size and fast transient response.

Table 1. Number of Output Capacitors

Load Current Transient, A	± 2	± 3	± 6
Number of Capacitors ESRE151M06R	2	3	4

The design is fulfilled for the following conditions:

- Input voltage: 3.3 V
- Output termination voltage: 1.25 V ±0.04V
- Load current slew rate: 10 A/μs
- Output capacitor: ESRE151M06R from Cornell-Dubilier with C = 150 μF, ESR = 15 mΩ, ESL = 3.2 nH

PowerPAD is a trademark of Texas Instruments

If the load current slew-rate is higher than 10 A/μs, additional high-frequency ceramic capacitors need to be added to the output to avoid excessive spikes caused by parasitic board-layout inductance and equivalent series inductance (ESL) of output capacitors.

The second thing that needs to be considered for the fast transient response is the bandwidth and gain of the feedback control loop. The advantage of an output filter optimized for the best transient is useless if it takes a long time for a control circuitry to change the duty cycle of regulator. The transient analysis[4] assumes that the controller reacts within the same switching cycle the transient occurs, which is true for hysteretic control. This is not the case for the voltage mode control having a relatively slow feedback loop.

Transient test waveforms have shown that 150-kHz unity gain bandwidth of the feedback loop and 1.4-V/μs slew rate of an error amplifier ensure that the regulator reacts in the next switching cycle following the transient. The difference between the theory and practice could require adding 1 or 2 more capacitors to the output filter especially at higher load current steps. The supply-path stray inductance and resistance of the PCB is not included in the analysis because it depends on the layout. Nevertheless, the design procedure referenced[4] enables the user to estimate the impact of supply path parasitics on the transient if some preliminary numbers are available.

Input/output ripple and power loss calculations are similar to any other synchronous buck converter. This information can be found in TI document SLVA104[5]. The following analysis is focused on optimal compensation circuitry selection for minimum-size, fast transient response applications.

The small signal transfer function of the output of the synchronous buck converter to the output of an error amplifier Vo(s)/Vea(s) = Wpt(s) is defined by the following equation[6]:

$$Wpt(s) = Vs \cdot \frac{R}{R + RL} \cdot KPWM \cdot \frac{(1 + s \cdot RC)}{1 + s \cdot \left(RC \cdot C + \frac{R \cdot RL}{R + RL} \cdot C + \frac{Lo}{R + RL} \right) + s^2 \cdot Lo \cdot C \cdot \frac{R + RC}{R + RL}}$$

Where:

Vs = 3.3 V – input voltage

R = 0.208 Ω – load resistance

Lo = 0.56 μH – output inductance

C = 300 μF – output capacitance

RL = 65 mΩ – dc resistance of output inductor and Rdson of FETs

RC = 7.5 mΩ – equivalent series resistance (ESR) of the output capacitor

KPWM = 1/Vpwm – PWM gain where Vpwm = 1 V is an amplitude of the ramp signal (see Fig.2)

$Fo = \frac{1}{2 \cdot \pi \cdot \sqrt{Lo \cdot C \cdot \frac{R + RC}{R + RL}}}$ is a corner frequency, Fo = 13.9 kHz

$$Fesr = \frac{1}{2 \cdot \pi \cdot RC \cdot C}$$ is zero frequency because of ESR of output capacitor; Fesr = 88 kHz.

$$\xi = \pi \cdot Fo \cdot \left(RC \cdot C + \frac{R \cdot RL}{R + RL} \cdot C + \frac{Lo}{R + RL} \right)$$ is damping factor; ξ = 0.815

The gain and phase Bode plots for this transfer function are shown in Figure 3. The output filter of SWIFT regulators is overdamped because the damping factor ξ = 0.815 is close to one. At ξ = 1 the denominator of transfer function Wpt(s) becomes the product of two equal single poles with corner frequency Fo. The overdamped filter does not have an abrupt 180-degree phase drop as in the case of low ξ underdamped filter. This feature is used to increase the overall unity bandwidth of the feedback loop as shown next.

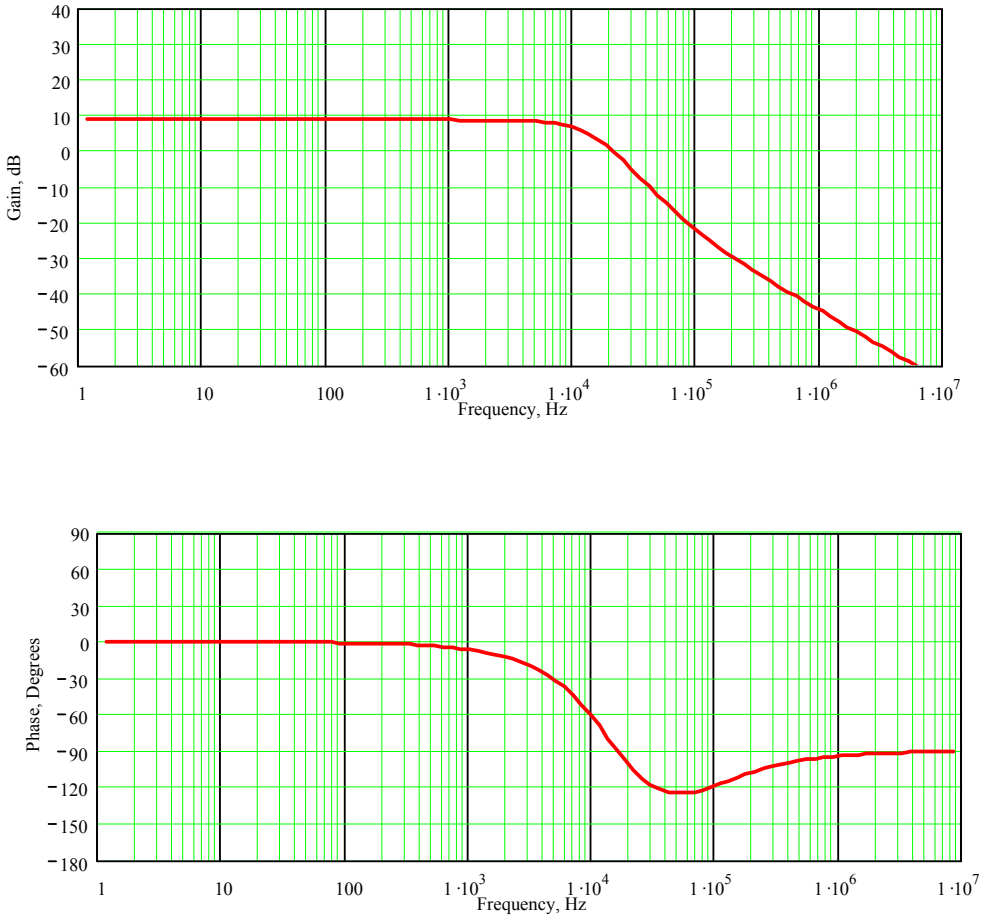


Figure 3. Bode Plot of Output Stage of SWIFT Regulator Including PWM

The error amplifier has a unity gain bandwidth of at least 3 MHz (5 MHz typ.). Gain as function of frequency $A_{EA}(f)$ is shown in Figure 4. The minimum dc gain of the error amplifier is 90 dB. The open loop frequency response of the error amplifier depends on its internal compensation. Adding any external compensation circuitry changes the frequency response, but this change will be located in the area below the open loop response curve. On the Bode plot, the sum of the open loop error amplifier $A_{EA}(f)$ and output stage of the regulator Apt(f) outlines the maximum achievable gain and bandwidth of the regulator's overall feedback loop. One can see from the summing plot A(f) in Figure 4 that the maximum dc gain is limited to 100 dB, and the unity bandwidth is limited to 150 kHz.

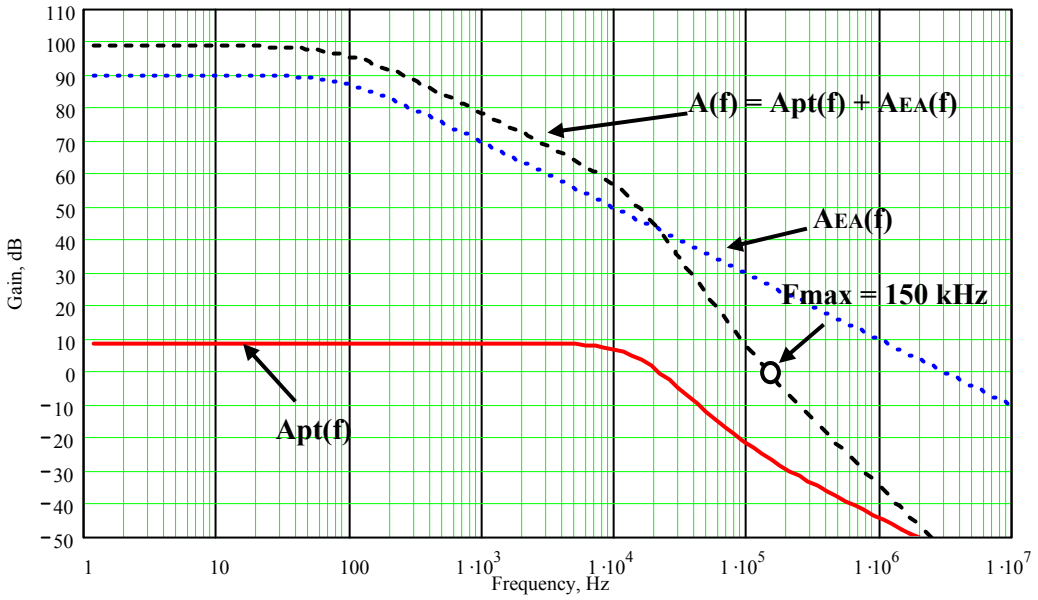


Figure 4. Sum (A(f) = Apt(f) + A_{EA}(f)) of Gains of Regulator Output Stage and Error Amplifier

The next step is to design a compensation circuit providing maximum bandwidth and gain without jeopardizing stability. The type 3 compensation circuit is recommended because of its flexibility (see Figure 5).

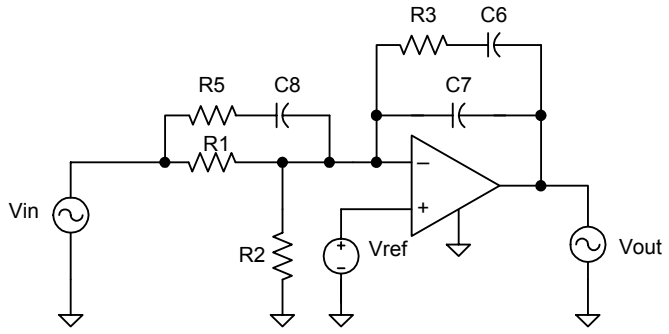


Figure 5. Type 3 Compensation

The transfer function of an error amplifier with the type 3 compensation is defined as

$$W1(s) = \frac{\left[1 + s \cdot C8 \cdot (R1 + R5)\right] \cdot (1 + s \cdot C6 \cdot R3)}{s \cdot (C6 + C7) \cdot R1 \cdot (1 + s \cdot C8 \cdot R5) \cdot \left[1 + s \cdot R3 \cdot \left(\frac{C6 \cdot C7}{C6 + C7}\right)\right]}$$

This transfer function has two zeros and three poles at frequencies defined as

$$Fz1 = \frac{1}{2 \cdot \pi \cdot C8 \cdot (R1 + R5)}$$

$$Fz2 = \frac{1}{2 \cdot \pi \cdot C6 \cdot R3}$$

$Fp0 = \frac{1}{2 \cdot \pi \cdot (C6 + C7) \cdot R1}$ is pole at the origin

$$Fp1 = \frac{1}{2 \cdot \pi \cdot C8 \cdot R5}$$

$$Fp2 = \frac{1}{2 \cdot \pi \cdot R3 \cdot \left(\frac{C6 \cdot C7}{C6 + C7}\right)}$$

It was mentioned that the overall feedback loop bandwidth in this design could not exceed 150 kHz because of limitations set by the error amplifier bandwidth. There is another limitation based on the switching frequency of the regulator Fs as well. The overall bandwidth Fbw usually has to be selected within the following range 1/10 Fs < Fbw < 1/3 Fs or 70 kHz < Fbw < 230 kHz for this particular application where Fs = 700 kHz. Taking these two limits into account, the bandwidth frequency 150 kHz is selected. The output stage of the regulator has –124 degree phase lag at 50 kHz (see Figure 3). It is important to get maximum gain at frequencies below the crossover point Fbw. If the compensation of error amplifier provides –20 dB/decade slope in this region, that will add –90 degree phase lag to the –124 degree lag from the output stage. An additional –180 degree phase lag is caused by negative feedback. To keep a regulator stable with 45 degree phase margin, a phase boost equal to (360 –180 –90 –124) + 45 = 79 degree has to be provided by the compensation circuitry. The generic approach to do this is to set both zeros Fz1 and Fz2 equal to the corner frequency of the output stage Fo. Both poles Fp1 and Fp2 then have to be selected to get the desirable phase boost at crossover frequency Fbw based on the following equation[7]

$\Theta = 270\deg - 2 \cdot a\tan(K) + 2 \cdot a\tan\left(\frac{1}{K}\right)$ where Θ is desirable phase boost and K is defined as

K = Fbw/Fz = Fp/Fbw

This approach works well with the underdamped filter. The output filter of SWIFT regulators is overdamped and a crossover frequency is limited to 150 kHz. In this case, location of one of the zeros below the corner frequency Fo and the other one above provides better results in terms of higher gain and phase margin below the crossover frequency Fbw.

Finding the optimal solution might require a few iterations, so it is better to use software, such as Mathcad for example. The final values of compensation circuitry are shown below:

R1 = 1.5 KΩ, R2 is open, R3 = 10 KΩ, R5 = 39 Ω, C6 = 470 pF,

C7 = 470 pF, C8 = 12000 pF.

The final Bode plots and location of zeros and poles are shown in Figure 6.

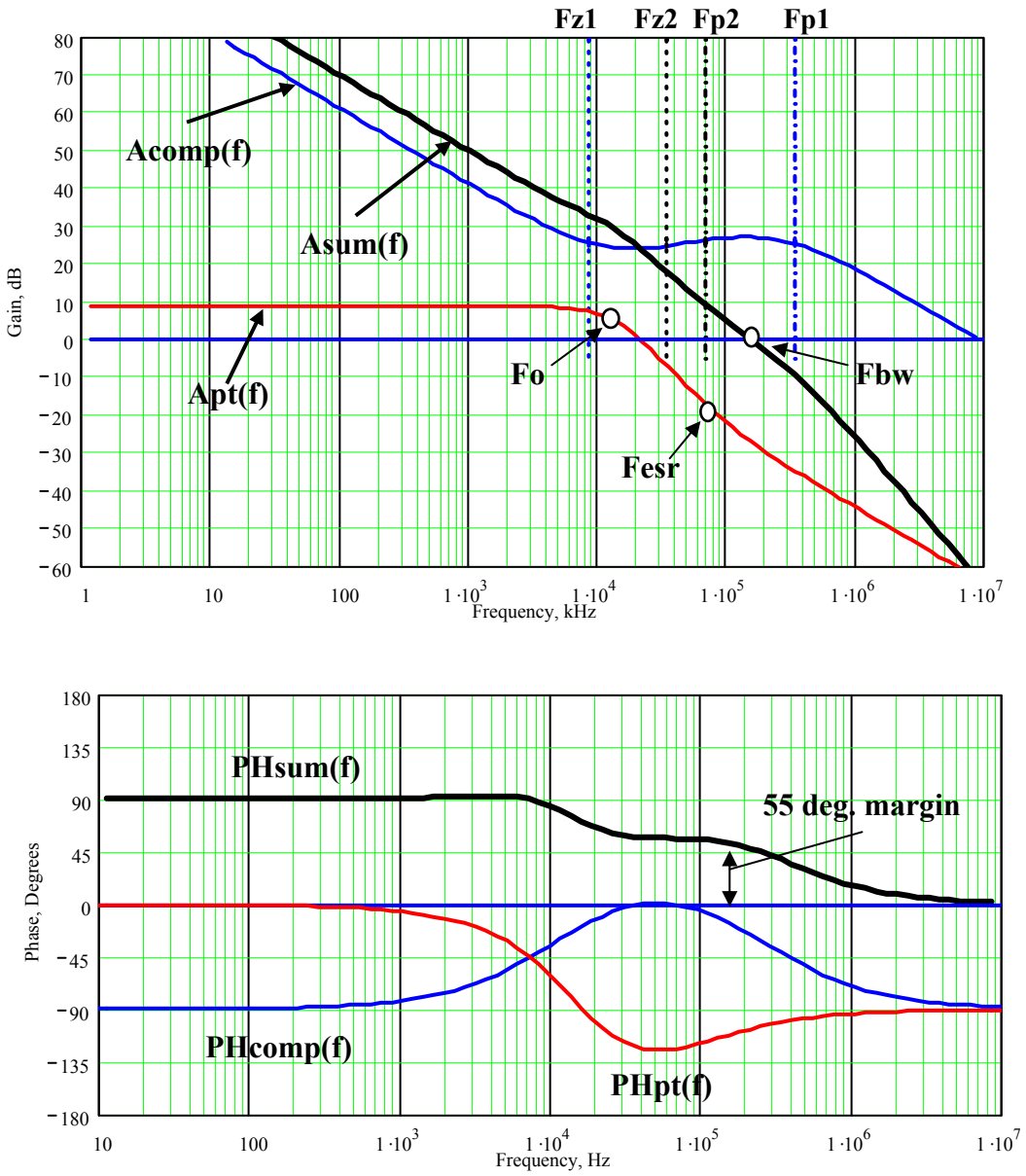
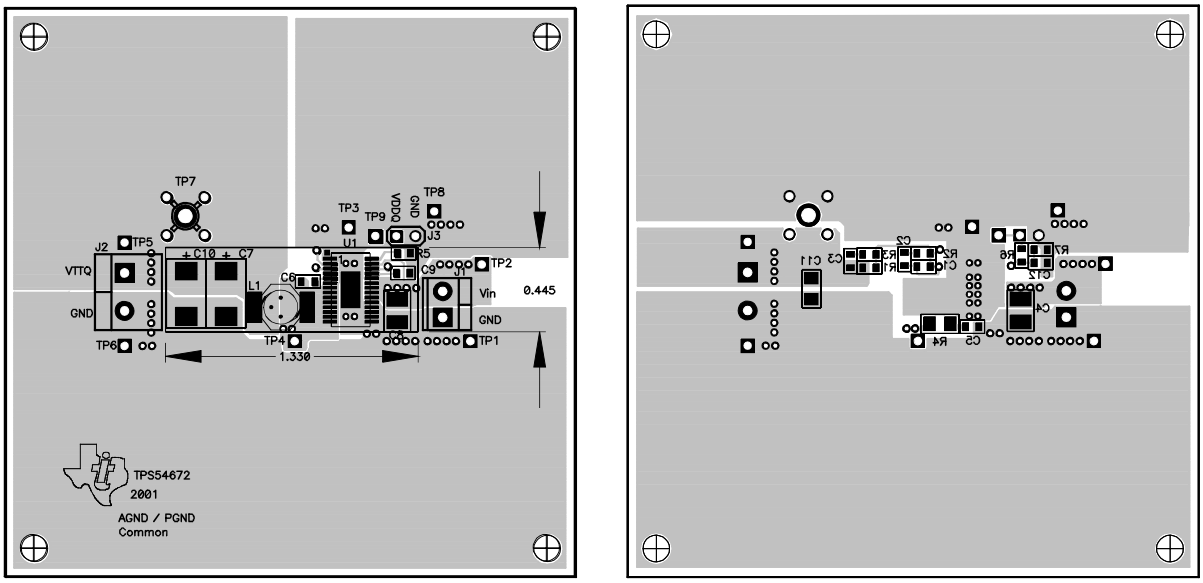


Figure 6. Overall Feedback Loop Bode Plots

It can be seen that zeros Fz1 and Fz2 are located below and above the corner frequency Fo correspondingly. The pole Fp2 is close to Fesr and the pole Fp1 is at about half of the switching frequency. This location provides maximum gain below the 150-kHz crossover frequency with a comfortable phase margin of 55 degrees. Transient tests have shown that this compensation decreases the peak to peak output voltage dynamic tolerance almost twofold. The SWIFT regulator with this compensation reacts to the load transient in the second switching cycle. This is a good achievement for the voltage mode control. Detailed transient waveforms are shown in the next section dedicated to the evaluation module TPS54672EVM-200.

Evaluation Module TPS54672EVM - 200

The evaluation module TPS54672EVM-200 is built and tested based on the described design procedure. The top and bottom assembly of the module is shown in Figure 7. The regulator itself occupies only 1.33 inches by 0.445 inches area and the total height is below 0.3 inches. The input voltage is specified from 3 V to 6 V. The output voltage is defined by the external reference. It is set at 1.25 V in accordance with the requirements for DDR SDRAM termination voltage[8]. The 6-A output current is sufficient to supply two standard memory modules.



Top Assembly Bottom Assembly

Figure 7. Evaluation Module TPS54672EVM-200

Schematic and Bill of Materials

The electrical schematic of the module is shown in Figure 8. This is a highly integrated solution that requires minimum external parts. The bill of materials is shown in Table 2. It includes only the mandatory parts of the circuit. Test point standoffs and terminal blocks that are only used for test purposes are excluded from the list. The input filter includes low ESR ceramic capacitors C4 and C8. The output filter includes the inductor L1 and capacitors C7, C10, C11. If a regulator is integrated into the system board, the required amount of capacitors in accordance with the Table 1, needs to be populated close to the memory module.

The divider R6, R7, C12 provides tracking reference voltage, which is equal to the half of V_{DDQ}. This divider is needed only for tracking regulator TPS54672. No other SWIFT family regulators need it. The feedback loop compensation circuitry R2, C1, C2, R1, R3, C3 forms the required frequency response that has been discussed in the Design Procedure section.

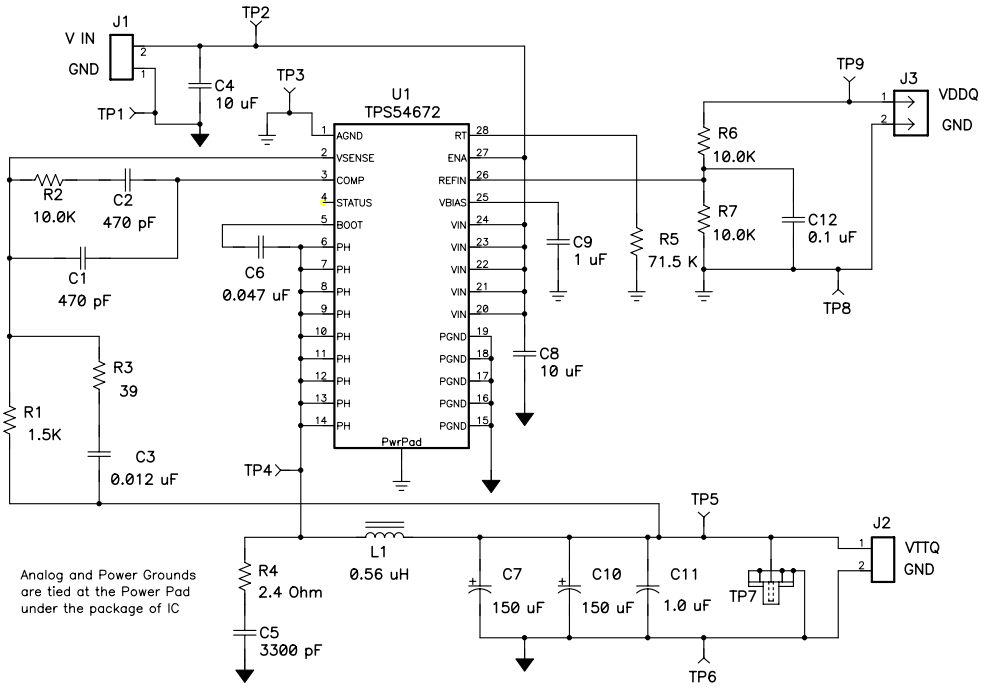


Figure 8. Electrical Schematic of Evaluation Module TPS54672EVM-200

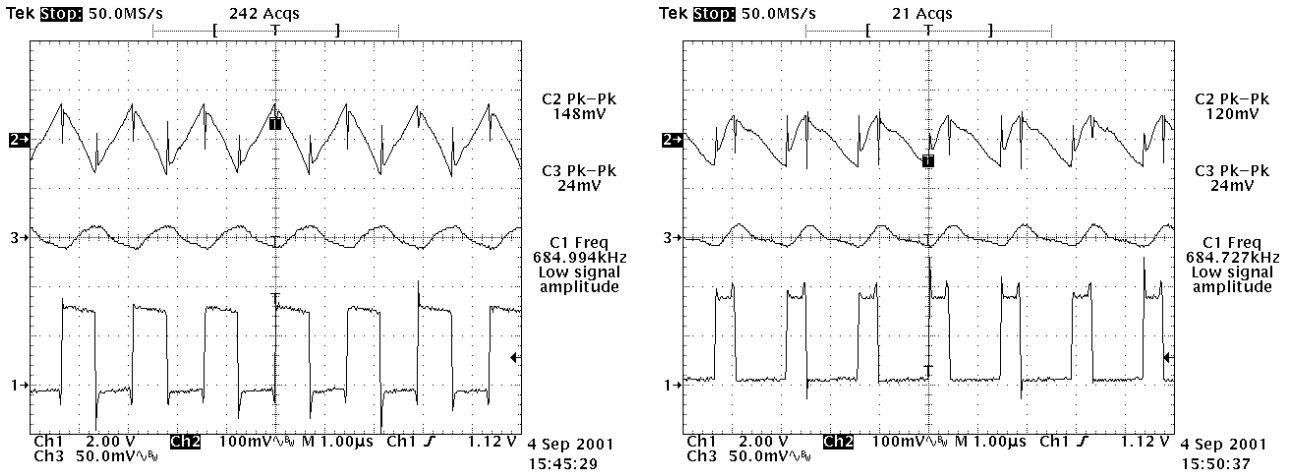
Table 2. Bill of Materials

QTY	RefDes	DESCRIPTION	SIZE	MFR	PART NUMBER
1	C1	Capacitor, Ceramic, 470-pF, 50-V, X7R, 10%	603	Panasonic	ECU-V1H471KBV
1	C11	Capacitor, Ceramic, 1.0-uF, 16-V, X7R, 10 %	1206	Panasonic	ECJ-3YB1C105K
1	C2	Capacitor, Ceramic, 470-pF, 50-V, X7R, 10%	603	Panasonic	ECU-V1H471KBV
1	C3	Capacitor, Ceramic, 0.012 uF, 16-V, X7R, 10%	603	Panasonic	ECJ-1VB1C123K
2	C4, C8	Capacitor, Ceramic, 10-uF, 10-V, X5R, 20%	1210	Taiyo Yuden	LMK325BJ106MN
1	C5	Capacitor, Ceramic, 3300-pF, 50-V, X7R, 10%	603	Panasonic	ECJ-1VB1H332K
1	C9	Capacitor, Ceramic, 1.0-uF, 10-V, X5R, 20%	603	TDK	C1608X5R1A105K
1	C12	Capacitor, Ceramic, 0.1-uF, 25-V, X7R, 10%	603	Murata	GRM39X7R104K25
1	C6	Capacitor, Ceramic, 0.047-uF, 25-V, X7R, 10%	603	Murata	GRM39X7R473K25
2	C7, C10	Capacitor, Polymer Aluminum, 150-uF, 6.3-V	62100	Cornell Dubilier	ESRE151MO6R
1	L1	Inductor, SMT, 0.56-uH, 7.7-A, 10-milliohm		Coilcraft	DO1813P-561HC
3	R2, R6, R7	Resistor, Chip, 10K-Ohms, 1/16-W, 0.1%	603	Panasonic	ERJ-3EKF1002
1	R1	Resistor, Chip, 1.5 K-Ohms, 1/16-W, 0.1%	603	Panasonic	ERJ-3EKF1501
1	R3	Resistor, Chip, 39 Ohms, 1/16-W, 0.1%	603	Panasonic	ERJ-3EKF0390
1	R4	Resistor, Chip, 2.4-Ohms, 1/8-W, 1%	1206	Panasonic	ERJ-8RQF2R4
1	R5	Resistor, Chip,71.5 K-Ohms, 1/16-W, 0.1%	603	Panasonic	ERJ-3EKF7152
1	U2	IC, IFET Termination Synchronus PWM switcher	PWP28	TI	TPS54672PWP
1	--	PCB, 3 In x 3 In x .062 In		Any	PMP067

Main Waveforms and Performance Curves

Test results of the evaluation module TPS54672EVM-200 confirm that it meets the standards and specifications for the SSTL-2 termination-voltage power supply in this particular application[8]. However, this design procedure for a minimum size and fast transient response application can be used with similar performance for any 6-A SWIFT family regulator. The switching and output/input ripple waveforms are shown in Figure 9 for the source and sink mode. The difference between the switching modes can be seen in channel 1 of Figure 9. During the source mode the internal diode of the low-side FET conducts during the dead time, while during the sink mode the internal diode of the high-side FET is conducting. Therefore, the high-side switch turns on, having switching losses at the source mode associated with the reverse-recovery of an internal diode in the low-side switch. At the sink mode, the low-side switch turns on with the switching losses. Although the switching processes are different at source and sink modes, the measured power losses are almost the same, as will be shown later.

Vin = 3.3V, Vout = 1.25V, Iout = 6A, Ch.2: Vin p-p [100mV/div.], Ch.3: Vout p-p [50mV/div.], Ch.1: Vph [2V/div.]



Source Mode **Sink Mode**

Figure 9. Switching and Output/Input Ripple Waveforms

The line and load regulation of the output voltage V_{TT} with an input voltage range from 3.3 V to 5 V, and output current range from -9 A (sink) to +9 A (source) is shown in Figure 10. Although the nominal current of this family of SWIFT regulators is 6 A, it can be extended depending on temperature and cooling conditions for a particular application. This regulator is self protected from the overload and overtemperature with the maximum load current threshold around 12 A. The line regulation is lower than 0.04% and the load regulation is better than 0.12%. JEDEC[8] specifies the termination voltage as 1.25 V ± 0.04V (±3.2%); so the dc accuracy of TPS54672 regulator is well within the specification.

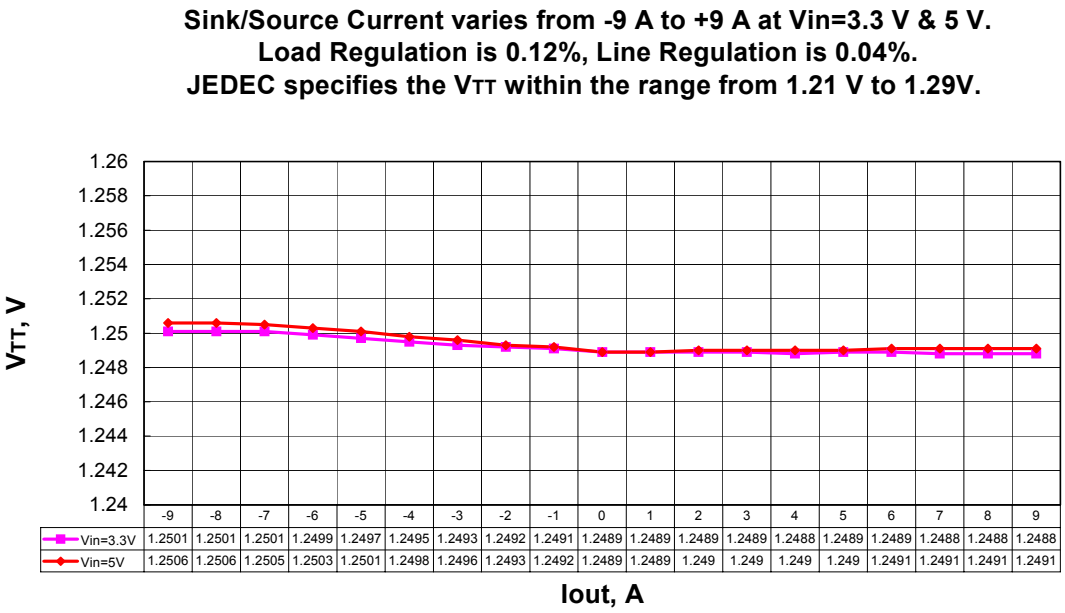


Figure 10. Line and Load Regulation

Power losses inside the IC package both at the sink and source mode are shown in Figure 11.

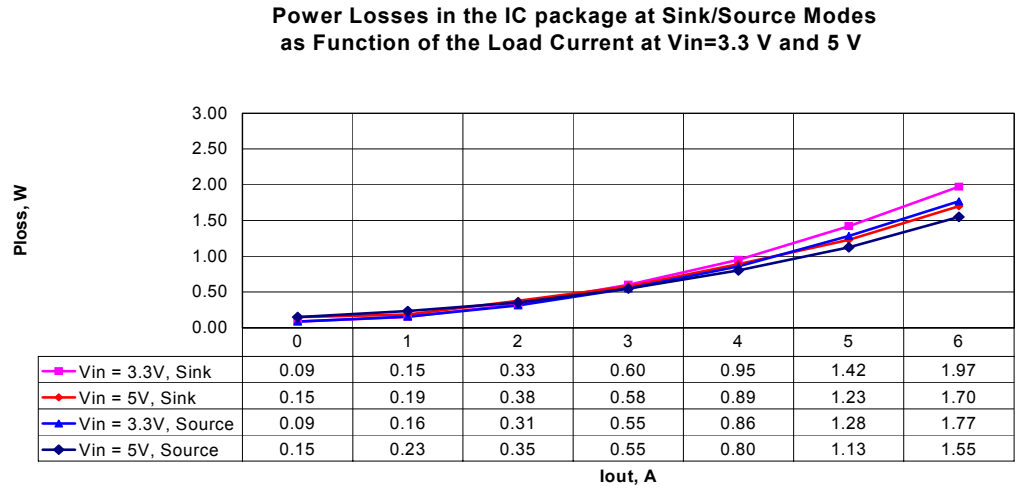
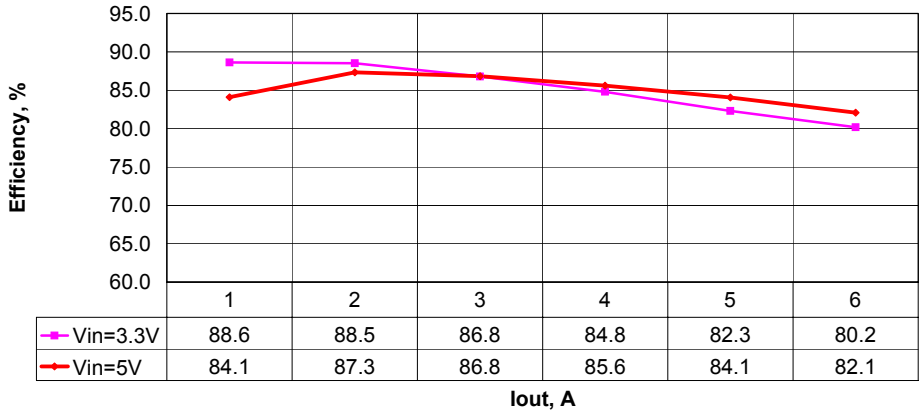


Figure 11. Power Losses Inside the Package

One can see that dissipation is almost the same both for sink and source mode. The maximum difference is only 0.2 W at 6-A sink current. The measured maximum dissipated power is slightly below 2 W for 3.3-V input and 6-A sink current. The thermally enhanced PowerPad package of this regulator can dissipate 3.58 W at ambient temperature 25^{O} C and 1.96 W at 70^{O} C. This gives a large margin to avoid the thermal shutdown of the regulator at normal operation.

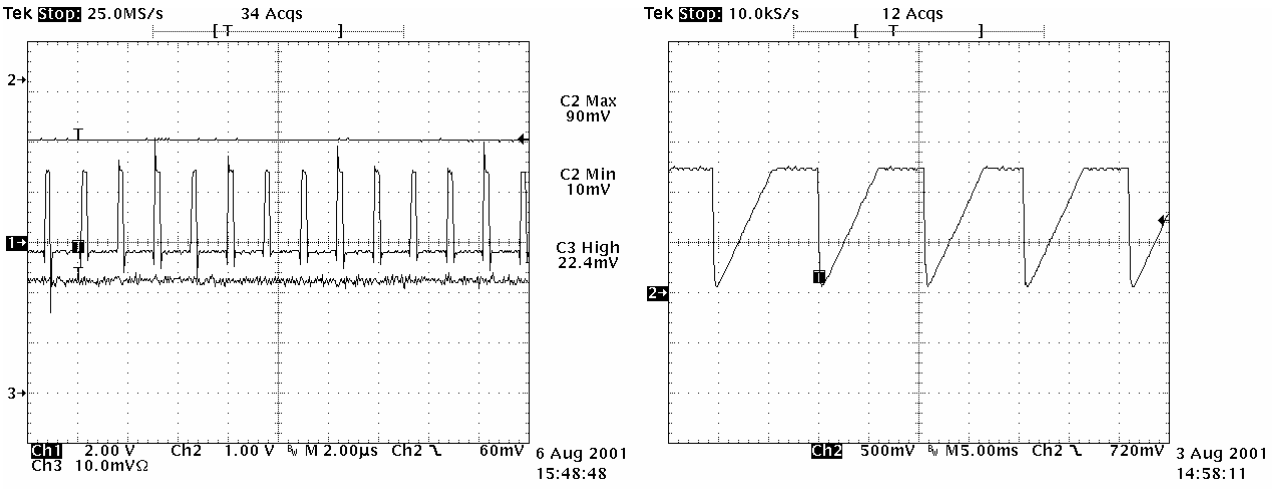
The efficiency curves for the input voltages 3.3 V and 5 V are shown in Figure 12. At load current below 3 A, the efficiency for 5-V input is lower in comparison with 3.3-V input because of higher switching losses. It is higher at load currents above 3 A because the higher gate drive voltage provides lower Rdson of the integrated FETs. In both cases the efficiency is relatively high and equals 86.8% for the output voltage 1.25 V and the current 3 A.



	1	2	3	4	5	6
Vin=3.3V	88.6	88.5	86.8	84.8	82.3	80.2
Vin=5V	84.1	87.3	86.8	85.6	84.1	82.1

Figure 12. Efficiency Curves at the Source Mode

The cycle by cycle current limit and thermal protection waveforms are shown in Figure 13. The cycle by cycle current limit provides very fast protection by decreasing the on time of the high-side FET (see channel 1, PH pin of the regulator). This forces the output voltage (channel 2) to drop down to almost zero. Notice that the voltage at channel 2 is below the ground because 1.25-V offset is applied to this channel. The output current at this mode is about 12 A, which is the channel 3 trace. After some time, the die temperature may reach the thermal shutdown limit which is 150^{O} C. This forces the regulator to shut down and initiates the soft-start again when the die temperature drops down by the amount of temperature hysteresis. Eventually the regulator starts and shuts down periodically with the frequency defined by the thermal shutdown hysteresis and the thermal conditions, as is shown at the output voltage waveform (channel 2) in the thermal protection waveform.



Cycle by Cycle Current Limit **Thermal Protection**

Figure 13. Two Types of Overcurrent Protection

The load-current transient waveforms when current steps from the negative 2 A (sink mode) to the positive 2 A (source mode) and backwards, are shown in Figure 14.

Vin = 3.3V, Vout = 1.25V, Ch.2: Vout p-p [50mV/div.], Ch.1: Iout [2A/div.], Time: [20µs/div.]

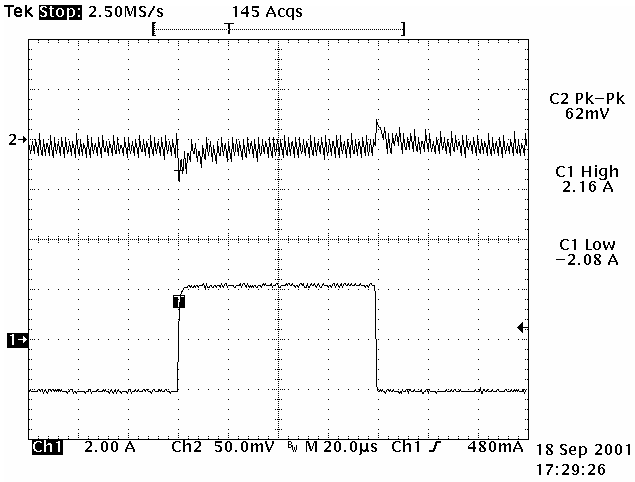
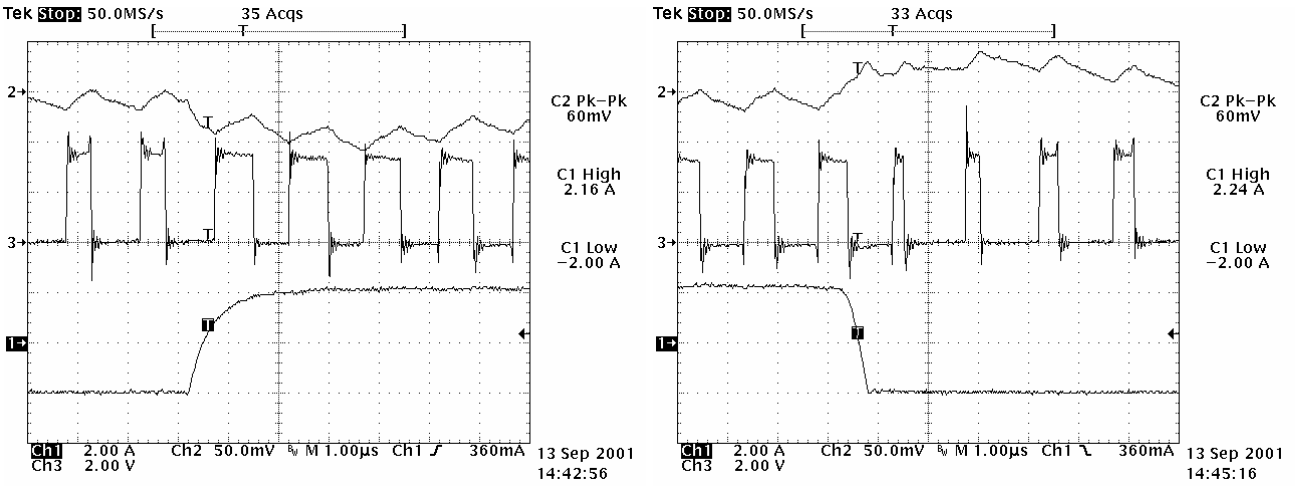


Figure 14. Load Current Transient Response

The peak-to-peak dynamic tolerance of the output voltage is only 62 mV, which is lower than the required 80 mV. The output voltage returns to its original level within 5 µs. The waveforms in Figure 15 show how fast the regulator reacts on transient. It changes the duty cycle immediately in the switching cycle following the transient. These high dynamic characteristics for the voltage mode control were achieved by optimizing the output filter and compensation circuit.

Vin = 3.3V, Vout = 1.25V, Ch.2: Vout p-p [50mV/div.], Ch.1: Iout [2A/div.], Ch.3: PH pin [2V/div.], Time: [1μs/div.]



Load Current Step Up **Load Current Step Down**

Figure 15. Expanded Load Current Transient Waveforms

The other important dynamic characteristic of the tracking regulator is how fast the output voltage follows the reference input. These waveforms for an abrupt reference voltage rise and fall are shown in Figure 16. The regulator output takes only 40 μs during the reference input rise time and 30 μs during fall time to reach a new level. Practically speaking, the rise and fall times do not depend on load current.

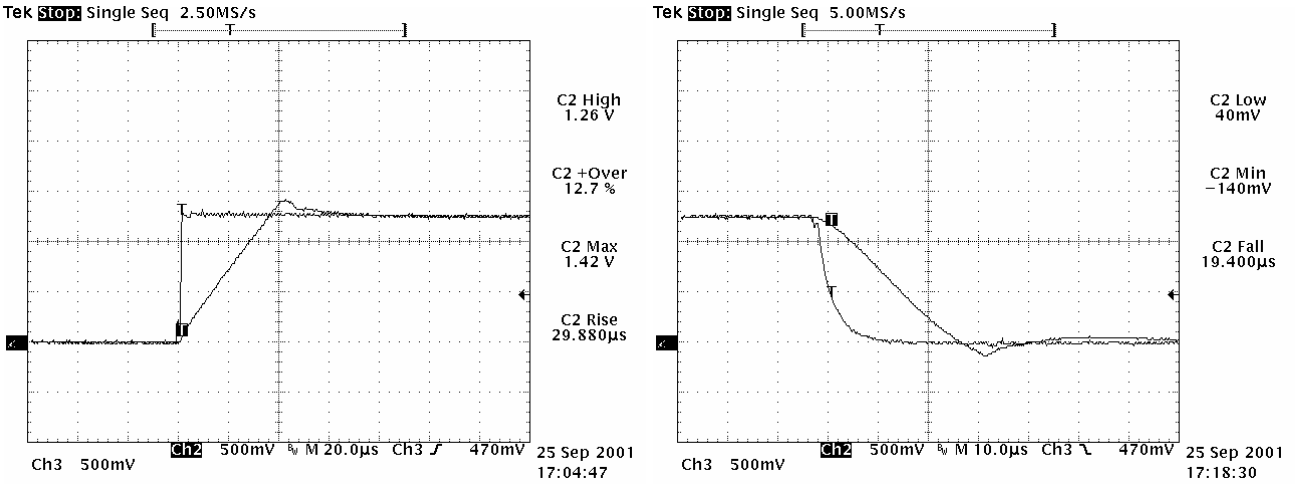


Figure 16. Output Voltage Response to the Reference Voltage Step Transient

Usually the reference input (REFIN pin) is connected to the V_{DDQ} regulator output through the resistor divider. The tracking regulator output voltage needs to follow the V_{DDQ} regulator output for example during a start-up, which is typically in the ms range. The fast tracking capability allows the TPS54672 regulator to follow the V_{DDQ} regulator very accurately. Figure 17 shows that the output voltage exactly coincides with the reference input when it changes at a typical slew-rate for an actual application.

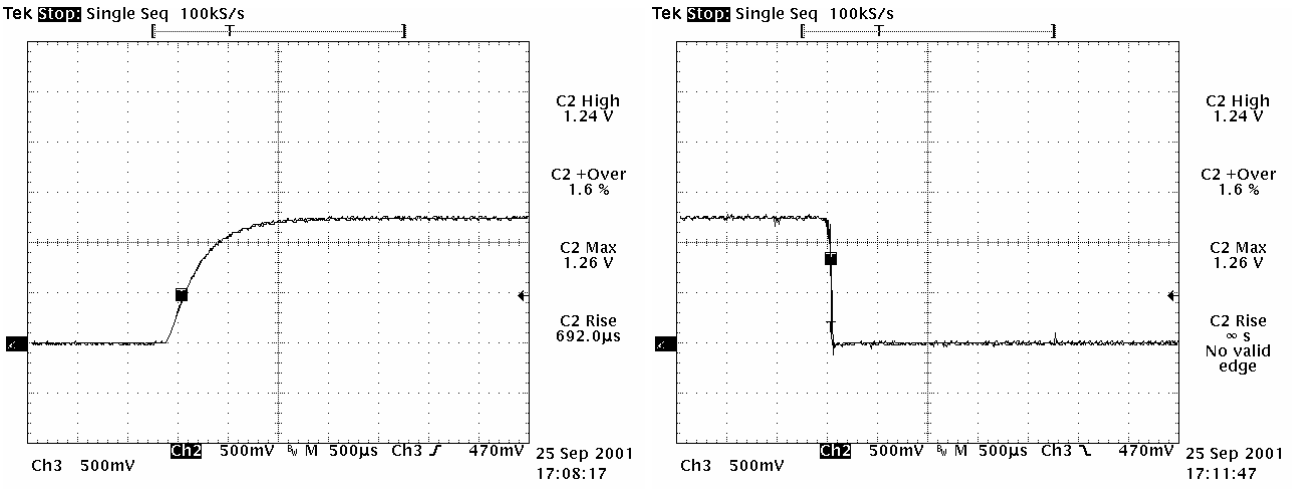


Figure 17. Output Voltage and Reference Input at Typical Slew-Rate

Figure 18 shows the start-up waveform when applying the input voltage. When the input voltage (channel 1) reaches the 2.96 V undervoltage lockout threshold, the start-up process, which goes under control of the internal slow-start circuitry, is initiated. The rise time of the output voltage (channel 2) is about 3 ms. It is practically the same for any load current within the specified range. For this particular application, the output voltage is 0.9 V.

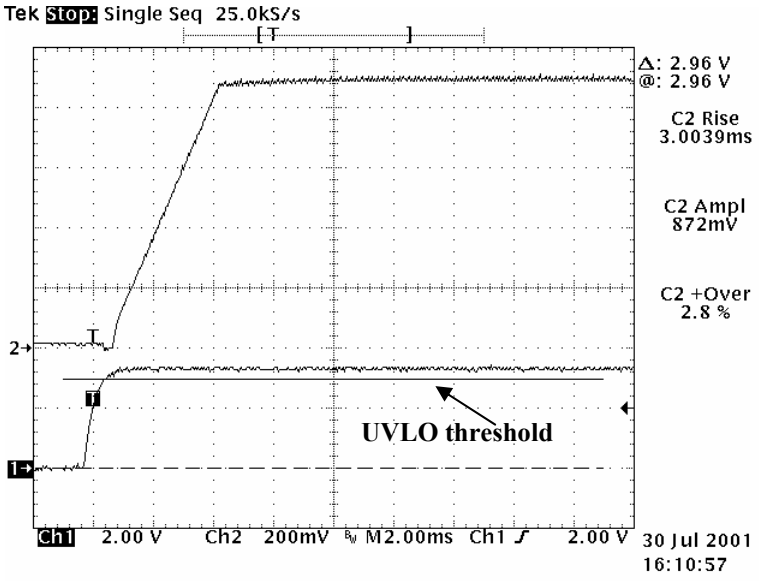


Figure 18. Start-Up Waveform by Applying the Input Voltage

Conclusion

The design procedure for minimum size and fast transient response application by using SWIFT family regulators is described. It is shown that the optimal output filter selection, along with the proper feedback-loop compensation, provides fast-transient response using the voltage mode control.

The design example of low-size, high frequency tracking regulator for the termination voltage of DDR SDRAM memory, using the highly integrated TPS54672 regulator illustrates this design approach. All requirements of the JEDEC specification for this type of logic are fulfilled with good margin.

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