Application Report
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Optimizing the Layout for the TPS54424/TPS54824 HotRod™ QFN Package for Thermal Performance

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ABSTRACT

Achieving the best thermal performance is an important aspect of the PCB layout for DC/DC converters. This is especially important for applications with high ambient temperatures which causes tough thermal requirements. End equipment's that often have these thermal challenges are active antenna systems (AAS), remote radio units (RRU), base band units (BBU), data center switches, metro data center interconnects, and broadband fixed line access. This application note examines how different layouts affect the thermal performance of the TPS54424 and TPS54824 converters. These converters use the HotRod™ QFN package for high power density and to minimize the parasitic resistance and inductance of the package. However, a difference with this package compared to a standard QFN is there not a large thermal pad on the bottom of the package. This raises the question on how to get the best thermal performance from the HotRod QFN package. Layout factors evaluated in this application note are thermal via placement, thermal via rules, and copper area.

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Trademarks

1 Introduction

The TPS54824 and TPS54424 are synchronous buck converters typically used with a nominal input voltage or 5 V or 12 V. The TPS54824 supports up to 8-A load current and the TPS54424 supports up to 4-A load current. The HotRod QFN package is used for high power density, high efficiency and to minimize switching node ringing. This package does this by attaching the die directly to the lead frame instead of using traditional bond wires. This reduces the parasitic resistance and inductance of the package. These low impedance connections between the die and the lead frame also provide a path for heat to flow from the die through every pin of the IC. However the lack of a thermal pad raises the question on how to get the best thermal performance.

Thermal performance is an important consideration for all ICs because operating at high junction temperatures can reduce their reliable lifetime. The reliable lifetime can be reduced because many of the common failure modes of ICs are accelerated by increased temperature. For a DC/DC converter thermal performance is doubly important because it can cause a limit to the load current it can support in a given application. For example RRUs typically have very high ambient temperature requirements of 100 °C and data center switches can have ambient temperatures of 70°C. In order to support these high ambient temperatures the maximum current the part can be used for may be limited in order to limit the junction temperature rise.

The first two sections of this application note go through the test setup for measuring the temperature and the circuit used for this evaluation. The remaining sections give the results of the layouts that were evaluated and the conclusions that can be made from the results.

2 Measuring Junction Temperature of the ICs

To evaluate the thermal performance, the temperature of the IC must be measured. Typical ways to measure temperature include a thermal camera, thermocouple, fiber optic probe and a temperature sensor integrated in the IC. Measurements taken using a thermal camera, thermocouple and fiber optic probe do not measure the junction temperature (T_J) directly. Instead these techniques measure the case temperature (T_C). This is where the junction-to-top characterization parameter (Ψ_{JT}) given in the data sheets is useful. The junction temperature of the IC can be calculated from the case temperature measurement using Equation 1. Typically Ψ_{JT} is very small so the junction temperature of the IC is very close measured case temperature. More details on this parameter can be found in the application note SPRA953.

$$T_J = T_C + \Psi_{JT} \times P_{LOSS\_BUCK} \quad (1)$$

For the calculation of the IC junction the power loss in the IC (P_{LOSS_IC}) is required. The power loss of the buck converter (P_{LOSS_BUCK}) is very easily found by measuring the input voltage, input current, output voltage and output current. The input power ($V_{IN} \times I_{IN}$) minus the output power ($V_{OUT} \times I_{OUT}$) gives the power loss of the buck converter. However not all of the power loss is in the IC. There is also power loss in the inductor, PCB, and the input and output capacitors. To get the power loss in the IC, the power loss from these other sources must be subtracted from the total power loss. Typically it is sufficient to only account for the power loss in the inductor because the other power losses are very small. When calculating the power loss of the inductor both conduction loss (P_{LOSS_DCR}) and AC loss (P_{LOSS_AC}) should be accounted for. Most inductor vendors have a tool to get the AC loss.

$$P_{LOSS\_BUCK} = V_{IN} \times I_{IN} - V_{OUT} \times I_{OUT} \quad (2)$$

$$P_{LOSS\_L} = P_{LOSS\_DCR} + P_{LOSS\_AC} \quad (3)$$

$$P_{LOSS\_IC} = P_{LOSS\_BUCK} - P_{LOSS\_L} \quad (4)$$

The measurements in this application note were taken with the test set up shown in Figure 1. Fiber optic probes touching the case of the IC are used to measure the case temperature. The EVM is also placed inside a box to prevent airflow within the lab from affecting the measurement. This test set up ensures the only airflow is from natural convection. The ambient temperature is measured by another fiber optic probe within the box placed away from the EVM. Lastly, there is a 10-minute soak time before each measurement to ensure that thermal equilibrium is reached.

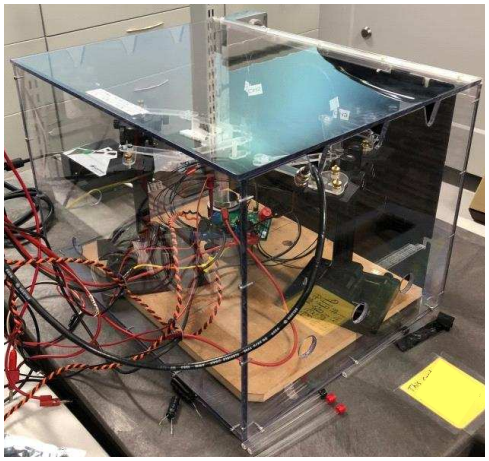


Figure 1. Picture of Test Setup - Box

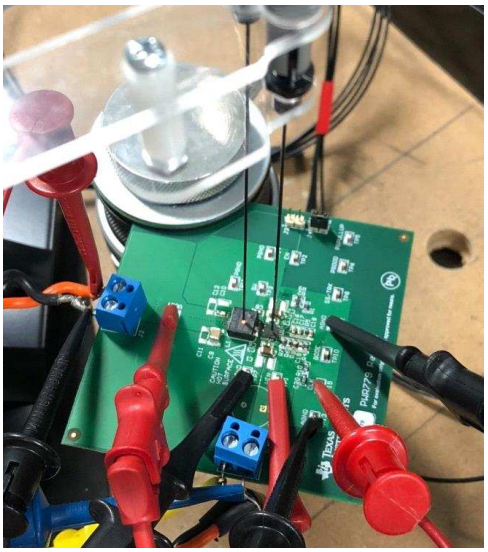


Figure 2. Picture of Test Setup - Fiber Optic Probes

3 Schematic Evaluated and Example TPS54824 Layout

The schematic used for evaluating the TPS54824 on different layouts is shown in Figure 7. The nominal input voltage is 12 V, the output voltage is 1.8 V, and the fsw is 700 kHz. An application with different input voltage, output voltage and fsw will change the power loss in the IC so different temperature rise can be expected. The evaluation is done up to the full 8 A load current supported by the TPS54824.

The typical PCB layout is shown in Figure 3 to Figure 6. All components are placed on the top layer. Some important aspects of this layout relevant to the thermal performance are listed below.

- PGND area should be maximized on the top layer conduct heat away from the IC and provide a larger surface area for heat to escape the PCB through convection.
- Multiple vias are placed near the PGND pins of the IC to conduct heat from the IC to the other layers of the PCB.
- The VIN trace must be wide to conduct the input current and to conduct heat away from the IC through the VIN pins.
- The inductor is placed near the IC and connected to the SW node with a trace that is as short and wide as possible. The SW node trace conducts the output current and conducts heat between the IC and the inductor.
- The VOUT area should be maximized to help conduct heat away from the inductor. It is important to conduct heat away from the inductor because the IC and inductor will experience thermal coupling. They are thermally coupled because they have a significant amount of power loss, are electrically connected through the SW node and are placed next to each other. The VOUT plane must also be wide to minimize its resistance because it will conduct the output current.
- The two internal layers and the bottom layer are filled with PGND to help conduct heat away from the IC.
- The PGND area is cut up on the third layer by PVIN and VOUT planes used to conduct the input current and output current. On this layer there is also a trace connecting the BOOT pin to the BOOT

capacitor.

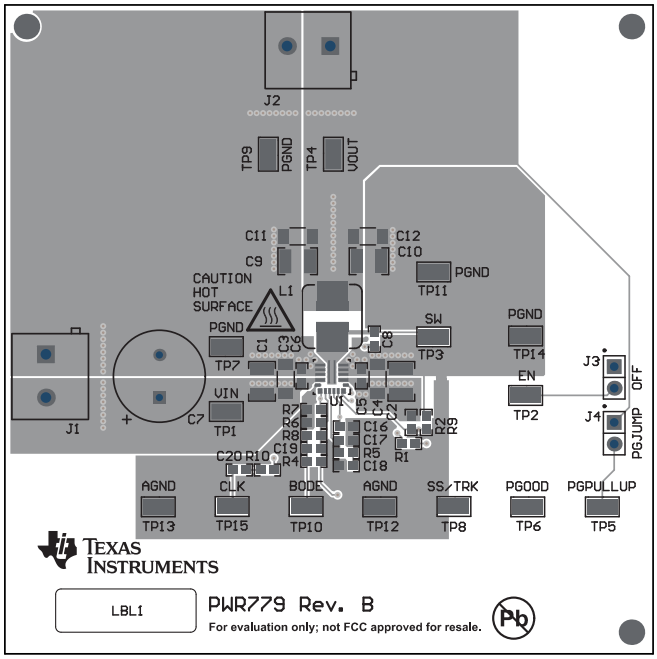


Figure 3. TPS54824EVM-779 Rev. B Top Layer

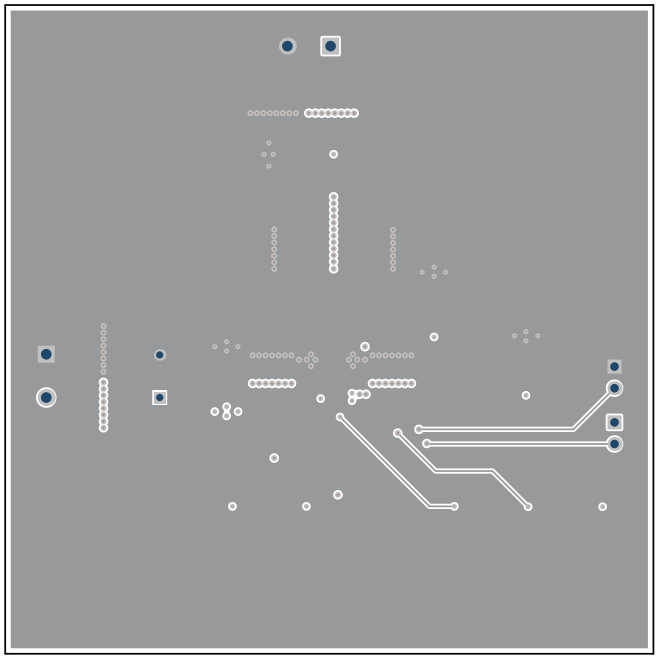


Figure 4. TPS54824EVM-779 Rev. B Mid Layer 1

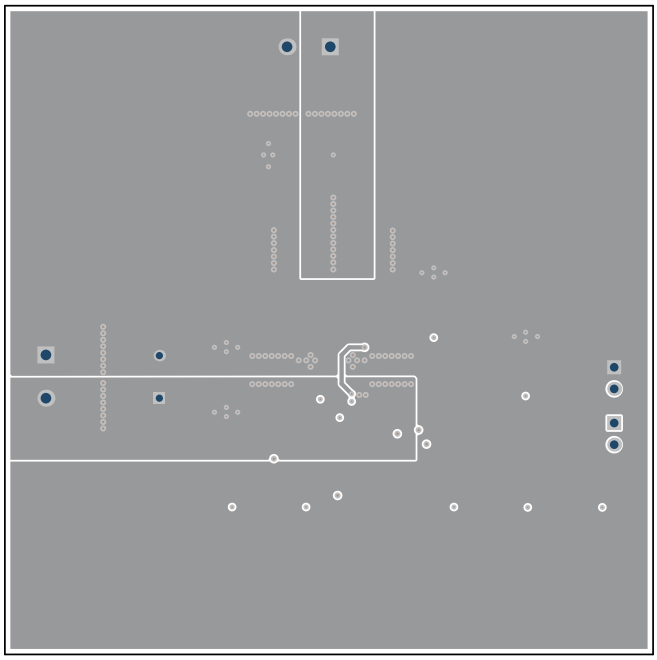


Figure 5. TPS54824EVM-779 Rev. B Mid Layer 2

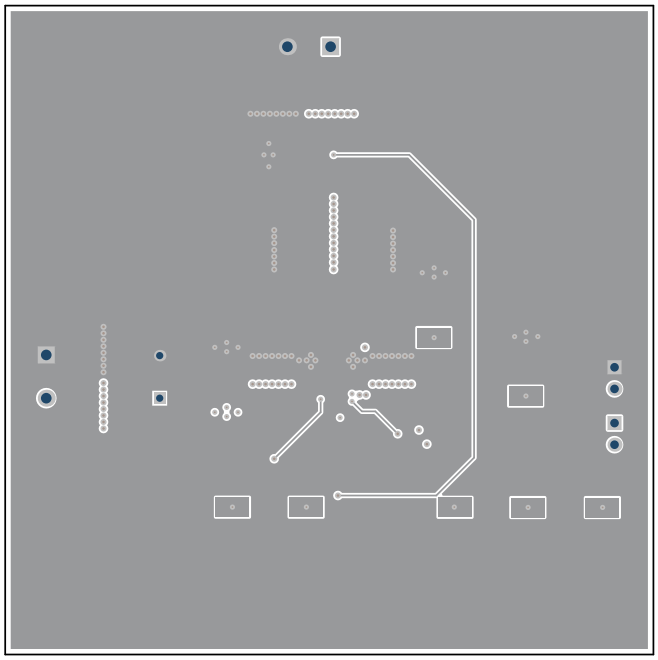


Figure 6. TPS54824EVM-779 Rev. B Bottom Layer

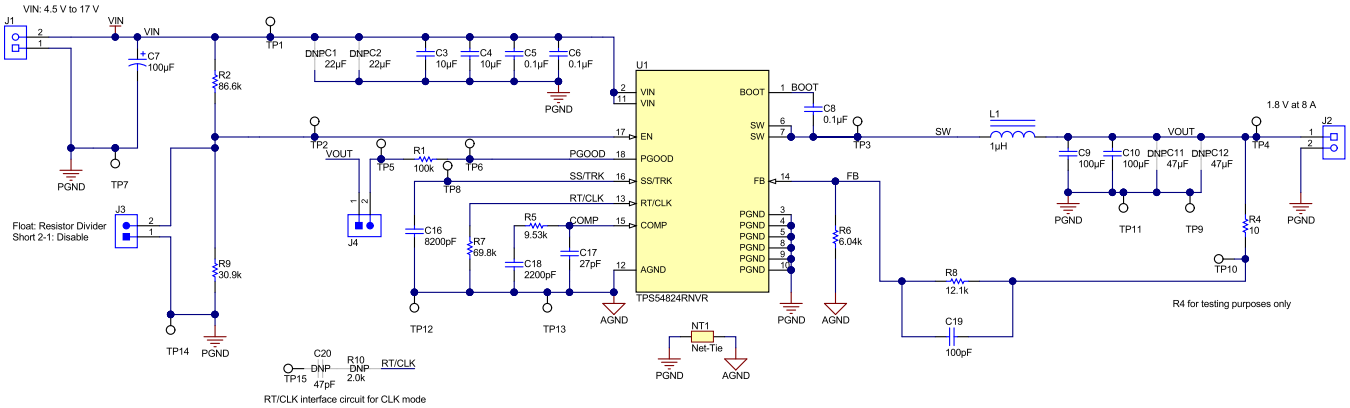


Figure 7. TPS54824EVM-779 Rev. B Schematic

4 Thermal Performance With Different PCB Layouts

Four different layout comparisons were done to test how different variables affect thermal performance. The first one compares different thermal via placement by comparing the two revisions to the TPS54824EVM-779. The second compares the effect of different via rules and different number of vias while keeping the placement of the vias as similar as possible. The third discusses the effect of putting thermal vias in pads and between pads. The fourth and last compares the effect of copper area. Variables that were not tested and kept fixed was PCB layer count of 4 layers and copper weight of 2 ounces.

4.1 Thermal Via Placement Comparison

The first comparison is between two revisions of the TPS54824EVM-779, revision A and revision B. New builds of the EVM use the revision B layout. Both revisions have the copper planes filling an area of 3 in x 3 in, via hole diameter of 12 mils, via pad diameter of 24 mils and minimum hole to hole clearance of 20 mils. This via hole diameter and pad diameter results in a via annular ring of 6 mils. With 12 mil hole vias, the 20 mil hole-to-hole clearance results in a via center-to-center spacing of 32 mils. Figure 8 shows the revision A and revision B top layer layout side-by-side. The main improvement made in the revision B EVM was in the placement of the thermal vias. The revision A EVM had only 2 thermal vias next to the IC placed near the corners of the IC. On revision B these two thermal vias near the corners of the IC were moved closer to pin 5 and 8. Two additional thermal vias were also added, one near pins 4-5 and one near pins 8-9. The improved thermal via placement and the additional vias help to conduct heat from the top layer to the other layers of the PCB.

In addition to the change in thermal vias, there are two other differences between revision A and revision B that may affect the thermal performance. In revision B the BOOT capacitor was moved so that the PGND copper connected to pins 3-5 has a slightly wider connection to the rest of the PGND copper on the top layer. This can help heat conduct from the IC to the rest of the top layer. With the BOOT capacitor moved in revision B, the inductor was also moved closer to the IC.

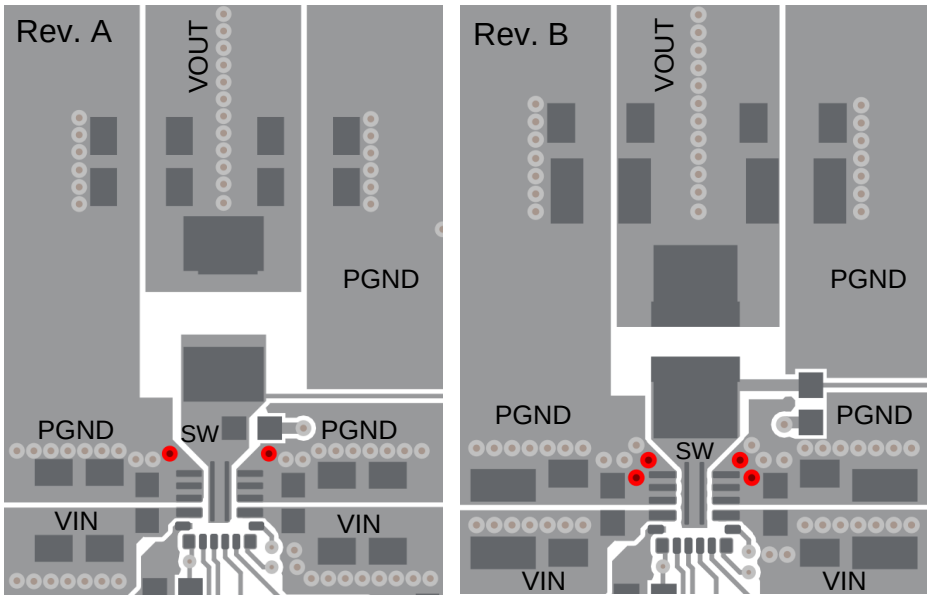
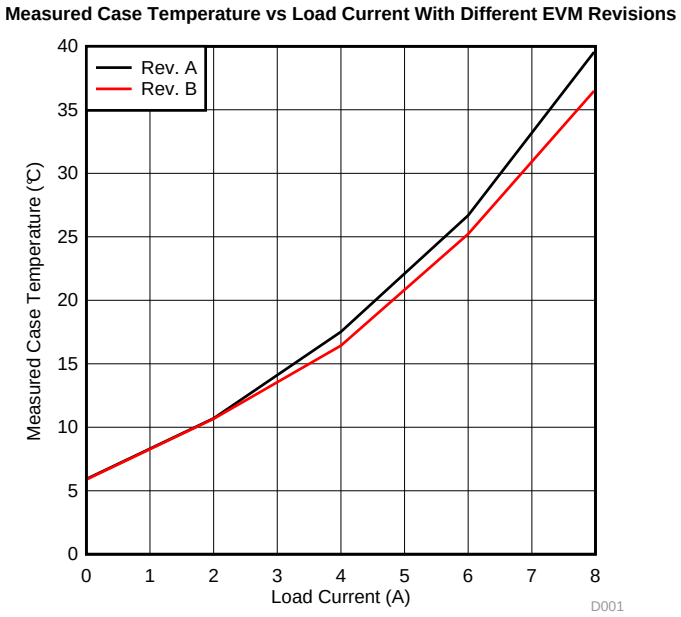


Figure 8. TPS54824EVM-779 Rev. A vs Rev B. Top Layer Layout

Figure 9 shows the IC case temperature rise vs load for the two revisions of the EVM. At the full 8-A load current, the revision B EVM has 3 °C lower temperature rise. This improvement in the revision B EVM shows the importance of having a few well-placed thermal vias as close as possible to the IC for the best thermal performance.



V_{IN} = 12 V V_{OUT} = 1.8 V f_{SW} = 700 kHz
T_A = 23 °C 10-minute soak time

Figure 9. TPS54824EVM-779 Rev. A vs Rev B. Case Temperature Rise

4.2 Thermal Via Design Rules

The next variable tested was different via rules. Generally using smaller via hole diameter, smaller hole-to-hole clearance and more vias can increase the cost of the PCB fabrication. The via rules tested are summarized in Table 1. Figure 10 to Figure 13 show the details of the top layer for layouts tested. The vias being counted as thermal vias are colored red. Each layout has vias placed next to PGND pins 3-5 and 8-10 to get the best thermal performance. Figure 10 shows the layout with a medium via density for this comparison, Figure 11 shows the layout with the lowest via density, and Figure 12 shows the layout with the highest via density. The layout shown in Figure 13 uses the same via density as that of Figure 10. The difference in the layout of Figure 13 is 4 additional thermal vias were added. This layout was evaluated to test the effectiveness of having more vias that are further from the IC. The copper planes for all 4 of these layouts are within an area of 2 in × 2 in.

Table 1. Via Design Rules Evaluated

Name	Via hole/pad diameter	Annular ring	Minimum spacing (center to center)	Minimum spacing (hole edge to hole edge)	Number of PGND vias near IC
Medium via density	10/22 mil	6 mil	30 mil	20 mil	10
Lower via density	10/30 mil	10 mil	55 mil	45 mil	6
Higher via density	8/20 mil	6 mil	20 mil	10 mil	20
Medium via density - additional vias	10/22 mil	6 mil	30 mil	20 mil	14

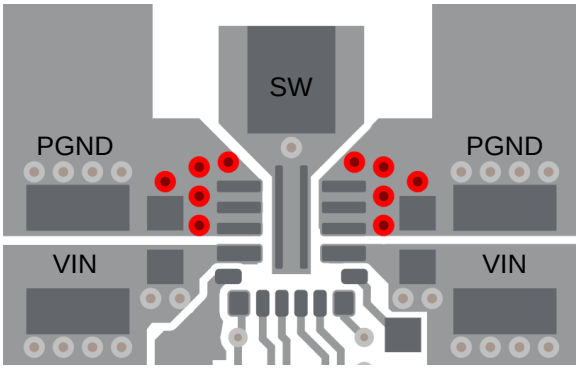


Figure 10. Medium Via Density

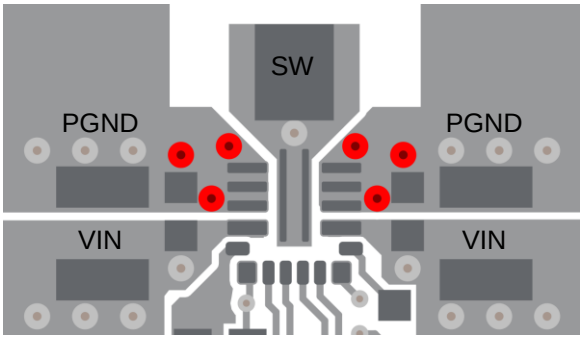


Figure 11. Lower Via Density

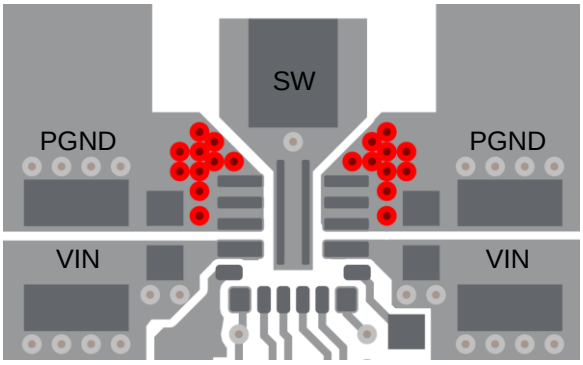


Figure 12. Higher Via Density

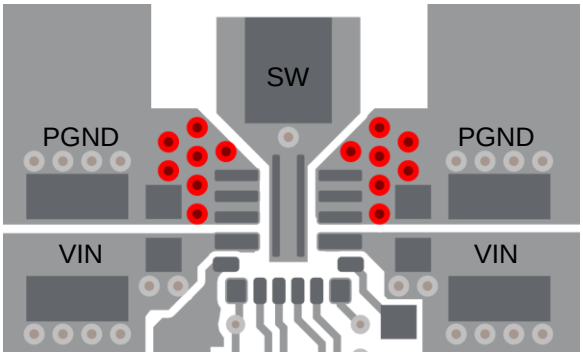
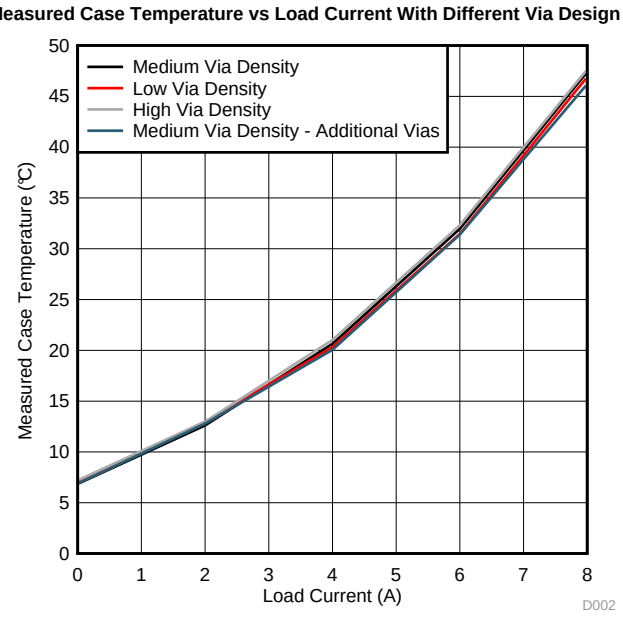


Figure 13. Medium Via Density - Additional Vias

Figure 14 shows the resulting case temperature rise vs load current with each of these via design rules. This curve shows that all 4 layouts had very similar thermal performance up to 8 A load. The layout in Figure 13 was only slightly better than the other layouts and the layout in Figure 12 was slightly worse. However the difference is so small that this could be caused by variations in components or measurement accuracy. Additionally the difference in the measured case temperature remains approximately the same from 4-A to 8-A load current. These results show that it doesn't take a more PCB fabrication process to get good thermal performance. Having at least one row of vias as close to the IC as design constraints will allow is what is important. Additionally, for the TPS54824, adding more vias further from the IC does not give a significant improvement.

The placement of the vias next to the IC should still be done with care. Too many vias may hurt thermal performance because the vias cuts up the planes and may begin to add thermal resistance. They can also hurt electrical performance because the cuts can also add parasitic resistance and inductance between the input bypass capacitors and the PGND pins. The layout shown in Figure 10 and Figure 11 has a good balance.



V_{IN} = 12 V V_{OUT} = 1.8 V f_{SW} = 700 kHz
T_A = 23°C 10 minute soak time

Figure 14. Case Temperature Rise Comparison With Different Via Design Rules

4.3 Placing Thermal Vias in Pads or Between Pads

To get the best thermal performance it is desirable to put the thermal vias below the IC. This means the vias need to be placed in the pad or between the pads of the IC. Design rules for reliable PCB fabrication and assembly may not allow this. If the via is placed in the pad it can wick solder away from the pad reducing the solder coverage of the pin. Reduced solder coverage can hurt the thermal and electrical performance. Using the minimum finished hole size can help to limit solder wicking. The only way to prevent wicking is to fill or plug the vias but filled vias increase the cost of the PCB fabrication.

In addition to the added cost of filled vias, the TPS54824 package does not have large enough pads to fit drilled vias. A common minimum pad size of a drilled via is 18 mil and this must fit in the pads or between the pads in the land pattern for the IC. In the recommended land pattern for the TPS54824 in the datasheet, the IC pads with the largest width in the recommended footprint for the TPS54824 are the ones for the VIN pins. They have a width of 0.4 mm (~16 mil) and this is smaller than the minimum 18 mil via pad size. The spacing between the PGND pins is 0.25 mm (~10 mil) so there is not enough space for the minimum 18 mil via pad between the IC pads. The 18 mil via pad does not fit and many applications have design rules that require even larger via pads. Vias can only be placed in the pads or between the pads for the IC if the PCB fabrication process being used allows for laser drilled microvias.

Since via-in-pad and vias between pads is not practical with the TPS54824 using drilled vias, their effect on thermal performance was not evaluated. Instead an alternate footprint was evaluated that meets the design rules for drilled vias. In the footprint shown in Figure 16 the length of the solder mask opening for pins 3-4 and pins 9-10 was made smaller to allow placing 4 vias beneath the IC. The size of these additional vias is 8 mil hole with a 20 mil pad. Besides this change in the footprint, the PCB layout is the same as Figure 10.

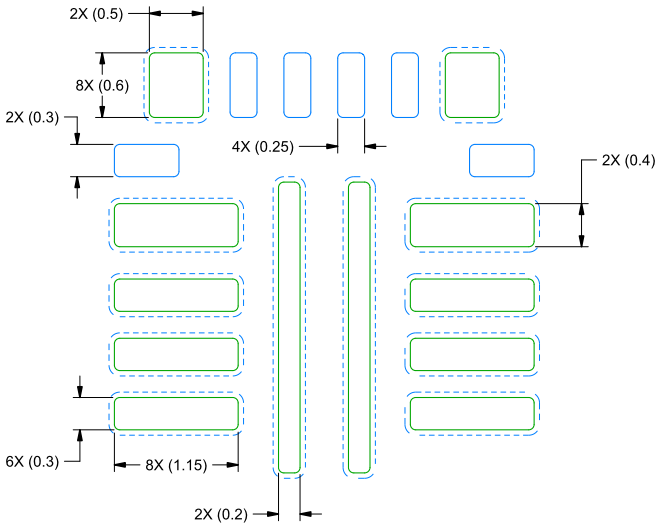


Figure 15. TPS54824 Pad Widths in Recommended Land Pattern

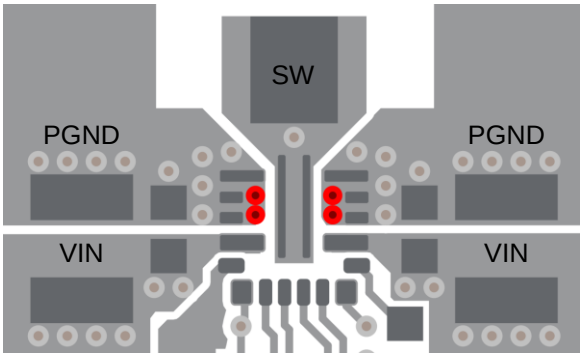
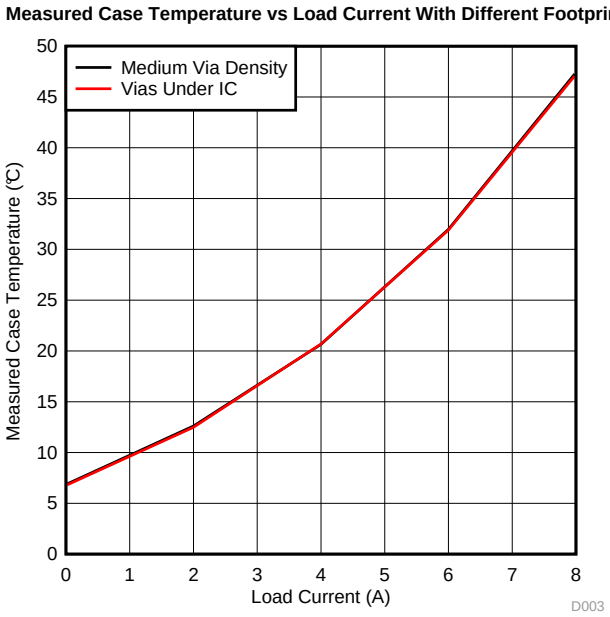


Figure 16. Alternate Footprint With Vias Under IC

Figure 17 shows the results. This alternate footprint gave almost no change in the thermal performance. The measured case temperature of the IC was only 0.2 °C lower than the medium via density footprint. This difference so small that it could have been caused by component variation or measurement accuracy. This alternate footprint does not give a significant improvement in thermal performance most likely because it comes with the tradeoff of having less of the IC pad soldered to the PCB. With less of the IC pad soldered to the PCB there is higher thermal resistance and electrical impedance between the IC and the PCB. This alternate footprint is **not** recommended and placing thermal vias next to the IC gives a better layout.



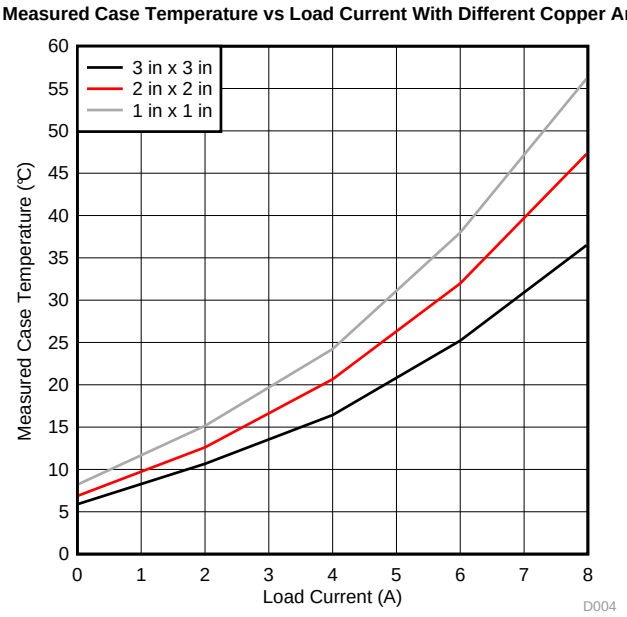
V_{IN} = 12 V V_{OUT} = 1.8 V f_{SW} = 700 kHz
T_A = 23°C 10-minute soak time

Figure 17. Vias Under IC Measured Case Temperature Rise Comparison

4.4 Copper Area

The final variable tested was the area the VIN, PGND and VOUT power planes covered on the PCB layout. The different plane dimensions tested were varied from 1 in × 1 in, 2 in × 2 in and 3 in × 3 in. The 3 in × 3 in layout tested was the TPS54824EVM-779 Rev B. The top layer of the 1 in × 1 in and 2 in × 2 in layouts are shown in Figure 19 and Figure 20. For these two layouts the copper area on the internal planes is kept within the same area. The only copper outside this area is for connecting VIN, VOUT and PGND to the screw terminals at the edge of the PCB.

Figure 18 shows the resulting temperature rise vs load current. At full 8 A load the measured rise in the case temperature of the IC was 56 °C for the 1 in × 1 in layout and 37°C for the 3 in × 3 in layout. This is a difference of 19°C. These results very clearly show the importance of maximizing copper area to get the best thermal performance. Increasing the copper area increases the amount of heat that can leave the PCB through convection and helps to conduct heat further away from the IC.



V_{IN} = 12 V V_{OUT} = 1.8 V f_{SW} = 700 kHz
T_A = 23°C 10-minute soak time

Figure 18. Copper Area Measured Case Temperature Rise Comparison

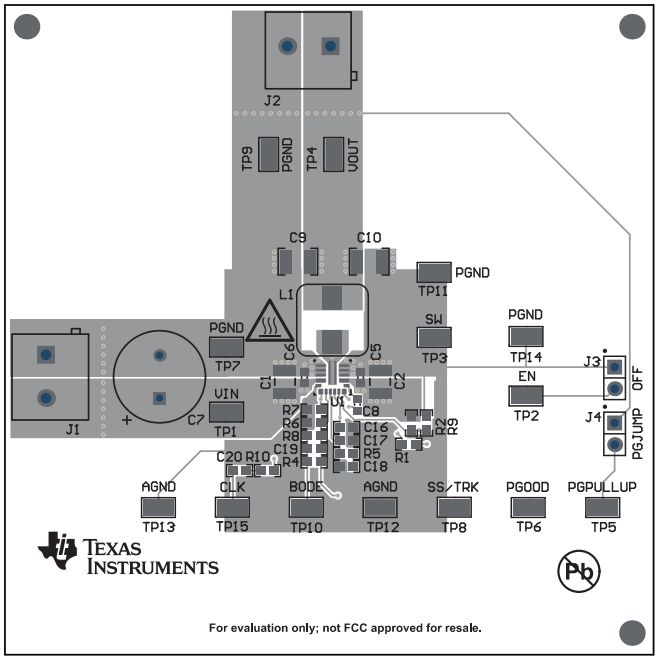


Figure 19. 1 in × 1 in Copper Area Top Layer

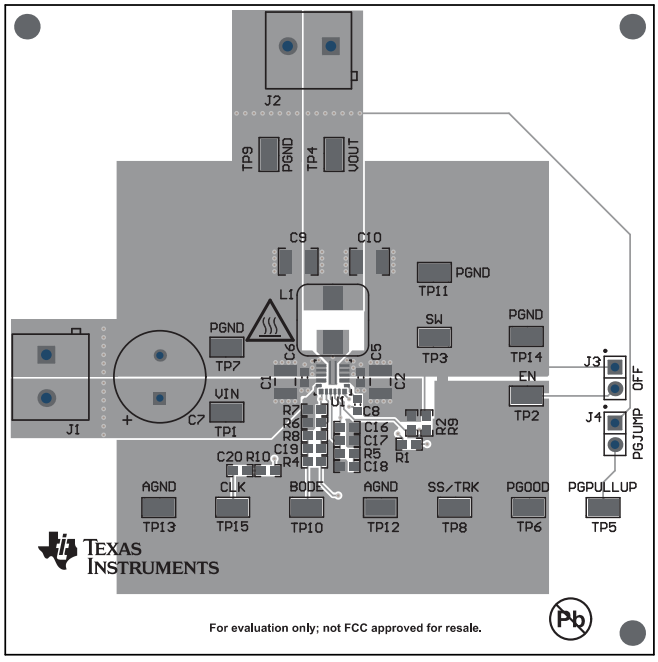


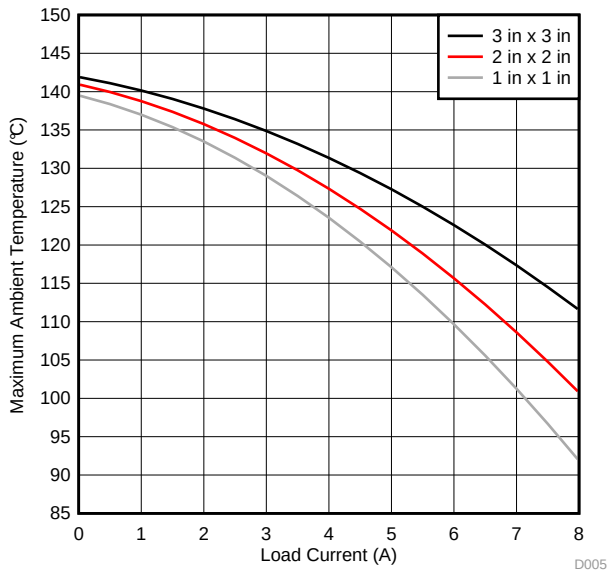
Figure 20. 2 in × 2 in Copper Area Top Layer

5 Summary

The layouts evaluated in this application note can be used as reference to get the best thermal performance from the TPS54824 HotRod QFN package. The comparison done in Section 4.1 shows that placing thermal vias as close as possible to the IC helps to get the best thermal performance. Section 4.2 shows that the thermal performance does not vary much with different via design rules. This means a layout using typical via design rules can get the best thermal performance from the TPS54824. This section also shows that having more than one row of vias next to the TPS54824 does not give a significant improvement in the thermal performance. A single row of thermal vias is sufficient. These vias also often fit in the space between components caused by minimum component-to-component spacing design rules. As a result these thermal vias do not add to the overall solution area. The layouts in Figure 10 and Figure 11 are the recommended thermal via patterns. Lastly Section 4.4 shows the most effective way to improve the thermal performance is to maximize the copper area on the PCB.

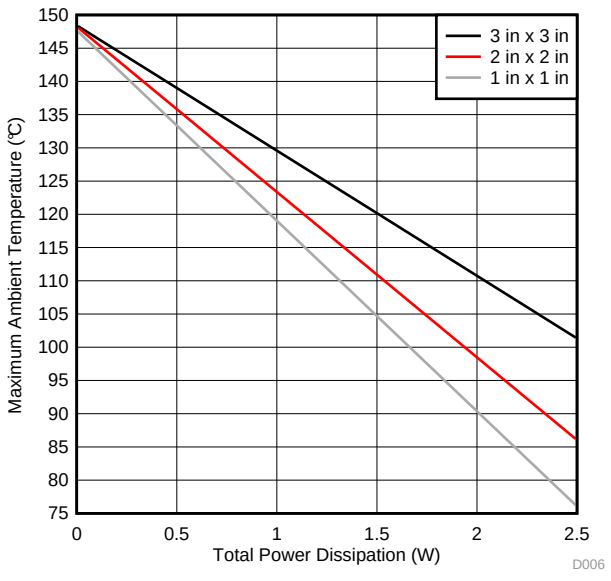
Variables of the PCB layout that were not tested but are important to keep in mind are copper weight and PCB layer count. Increasing either of these increases volume of copper on the board and this should improve the thermal performance. Additionally the environment in the board is placed in will affect the thermal performance. For example the enclosure the PCB is placed in and any airflow across the PCB will affect the IC's thermal performance. Lastly thermal coupling with any components placed nearby the IC will influence the thermal performance.

The graph shown in Figure 21 shows an example safe operating area (SOA) curve using the data from the tests with different copper area. These curves can be used as a reference point for the maximum load current the TPS54824 can support in a given maximum ambient temperature. This curve is estimated from the measurements taken at 23°C ambient temperature. This curve does not account for the ratings of external components, such as the inductor and capacitors that are often rated for 125°C or lower. The maximum load current will vary significantly with PCB layout and the application environment. Additionally the maximum load current for an application will vary with power dissipation in the application. This means changes to V_{IN}, V_{OUT}, f_{SW}, and the inductor also changes the maximum load current. Figure 22 formats this data in another way where the maximum ambient temperature can be estimated from a given power dissipation. The power dissipation used for this curve includes all loss in the buck converter (P_{LOSS_BUCK}). The power dissipation can be measured on the bench or estimated using WEBENCH.



V_{IN} = 12 V V_{OUT} = 1.8 V f_{SW} = 700 kHz
10-minute soak

Figure 21. Safe Operating Area vs Load Current



10-minute soak

Figure 22. Safe Operating Area vs Power Dissipation

6 References

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