

Unified Ground Connection Recommendation on TPS53K-Integrated FET-Converter Devices

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ABSTRACT

This document provides the unified ground connection recommendation for TPS53K-integrated FET-converter devices.

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1 Introduction

Since 2010, TI has introduced several generations of TPS53K-integrated FET converters with current rating ranging from 1.5 A to 40 A. This particular family of devices targets the enterprise computing applications; therefore, the devices share the same competitive performance goals in terms of efficiency, thermal, and transient response. Many design considerations simplify the system design and layout as well as reduce overall bill of materials (BOM).

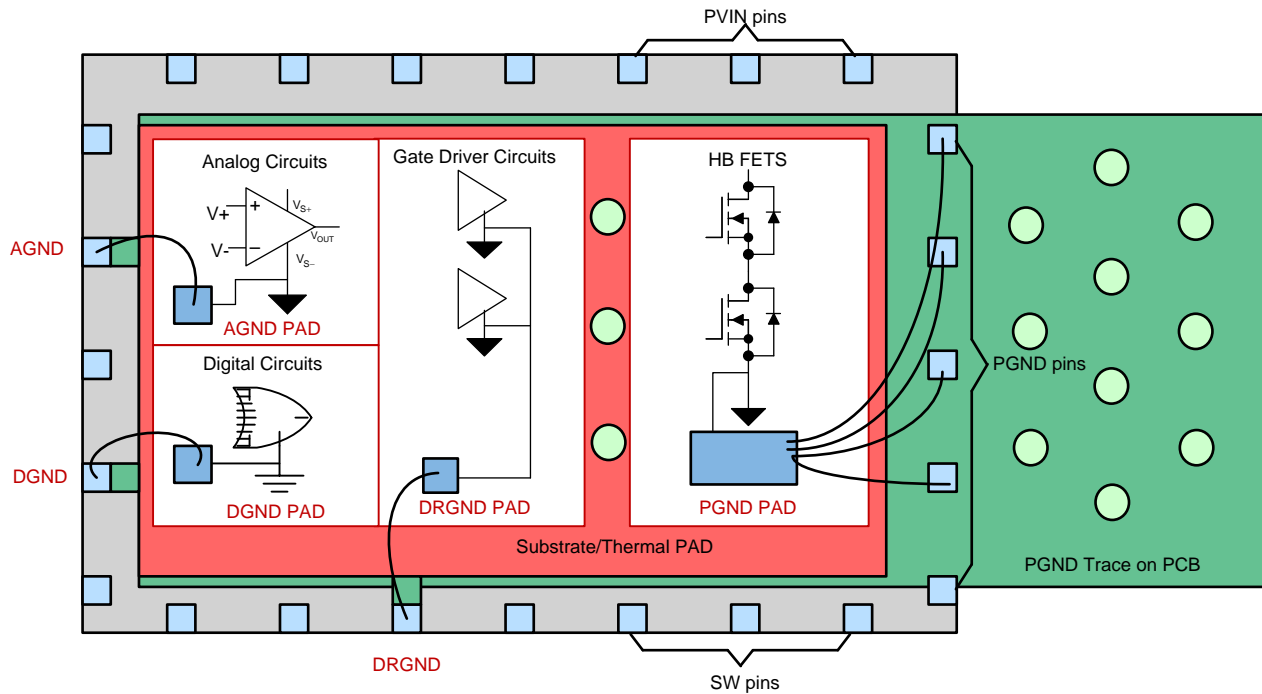
Table 1 summarizes the TPS53K converter devices in terms of their applications.

Table 1. TPS53K Device Details

PART NUMBER	CURRENT RATING	VIN RANGE (V)	VOOUT RANGE	PACKAGE SIZE AND STYLE	GROUND PINS
TPS53310	3 A	2.9 V to 6 V	0.6 V to 4.2 V	3 × 3 QFN-16	AGND, PGND
TPS53311	3 A	2.9 V to 6 V	0.6 V to 4.2 V	3 × 3 QFN-16	AGND, PGND
TPS53316	5 A	2.9 V to 6 V	0.6 V to 5.5 V	3 × 3 QFN-16	AGND, PGND
TPS53321	5 A	2.9 V to 6 V	0.6 V to 4.2 V	3 × 3 QFN-16	AGND, PGND
TPS53511	1.5 A	4.5 V to 18 V	0.75 V to 5 V	3 × 3 QFN-16	GND, PGND
TPS53312	3 A	4.5 V to 18 V	0.75 V to 5 V	3 × 3 QFN-16	GND, PGND
TPS53313	6 A	4.5 V to 16 V	0.6 V to 10 V	4 × 4 QFN-24	GND1, GND2, PGND
TPS53314	6 A	4.5 V to 25 V	0.6 V to 5.5 V	5 × 7 QFN-40	GND1, GND2, PGND
TPS53315	12 A	3 V to 15 V	0.6 V to 5.5 V	5 × 7 QFN-40	GND1, GND2, PGND
TPS53318	8 A	1.5 V to 22 V	0.6 V to 5.5 V	5 × 6 QFN-22	NA
TPS53319	14 A	1.5 V to 22 V	0.6 V to 5.5 V	5 × 6 QFN-22	NA
TPS53353	20 A	1.5 V to 15 V	0.6 V to 5.5 V	5 × 6 QFN-22	NA
TPS53355	30 A	1.5 V to 15 V	0.6 V to 5.5 V	5 × 6 QFN-22	NA
TPS53513	8 A	1.5 V to 18 V	0.6 V to 5.5 V	3.5 × 4.5 QFN-28	GND, PGND
TPS53515	12 A	1.5 V to 18 V	0.6 V to 5.5 V	3.5 × 4.5 QFN-28	GND, PGND
TPS53915	12 A	1.5 V to 18 V	0.6 V to 5.5 V	3.5 × 4.5 QFN-28	GND, PGND
TPS548A20	15 A	1.5 V to 20 V	0.6 V to 5.5 V	3.5 × 4.5 QFN-28	GND, PGND
TPS549A20	15 A	1.5 V to 20 V	0.6 V to 5.5 V	3.5 × 4.5 QFN-28	GND, PGND
TPS548B22	25 A	1.5 V to 18 V	0.6 V to 5.5 V	5 × 7 QFN-40	AGND, DRGND, PGND
TPS548D22	40 A	1.5 V to 16 V	0.6 V to 5.5 V	5 × 7 QFN-40	AGND, DRGND, PGND
TPS549D22	40 A	1.5 V to 16 V	0.6 V to 5.5 V	5 × 7 QFN-40	AGND, DRGND, PGND
TPS548D21	40 A	1.5 V to 16 V	0.6 V to 5.5 V	5 × 7 QFN-40	AGND, DRGND, PGND

In the integrated converter designs, where controller, gate driver, and half bridge (HB) FETs are uniquely integrated and fit into a small semiconductor device package, ground treatment is a very sensitive matter. To understand how different grounds are defined, connected, and used in an integrated circuit (IC), the environment should give insight how to create the ground layout in a system or printed circuit board (PCB) environment. Unfortunately, no two ICs are ever laid out the same way. There are many different approaches IC designs can employ in regards to ground layout, similar to that of system or PCB board. In the case of TPS53K device family, the ground treatment was created in a similar working fashion, which results in a uniformed ground layout recommendation possible.

Figure 1 illustrates conceptually how the grounds (including thermal pad – red rectangle) of the internal IC are allocated, distributed, and connected.



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Figure 1. Ground Arrangement Diagram of TPS53K-Integrated FET Converter

Generally speaking in each integrated-FET converter design, there are a few essential circuit elements or blocks. As shown in Figure 1, the entire IC is broken down into analog circuit, digital circuit, gate drivers, and HB FETs. In most cases there is a dedicated ground assignment for each of the major circuit blocks. For example, analog ground (AGND) is used to serve the analog circuits, digital ground (DGND) to digital circuits, driver ground (DRGND) to gate drivers, and PGND to HB FETs. In the ideal situation where pin count is sufficient, all of the ground assignments can be brought outside of the IC through dedicated GND pins. In situations where pin count is of concern, the arrangement can be made at the IC layout to combine and merge the ground assignments.

For quad flat no-leads (QFN) packaged devices, there is also a thermal pad sitting on the bottom of the package (see [Figure 2](#)). The silicon die (analog circuit, digital circuit, gate driver, and HB FETs) is attached onto the thermal pad using thermally conductive adhesive. [Figure 3](#) shows a cross-sectioned view of a typical QFN package. The exposed thermal pad is made of electrically conductive material, and when soldered on the PCB, the material makes a good electrical and thermal connection with the PCB.

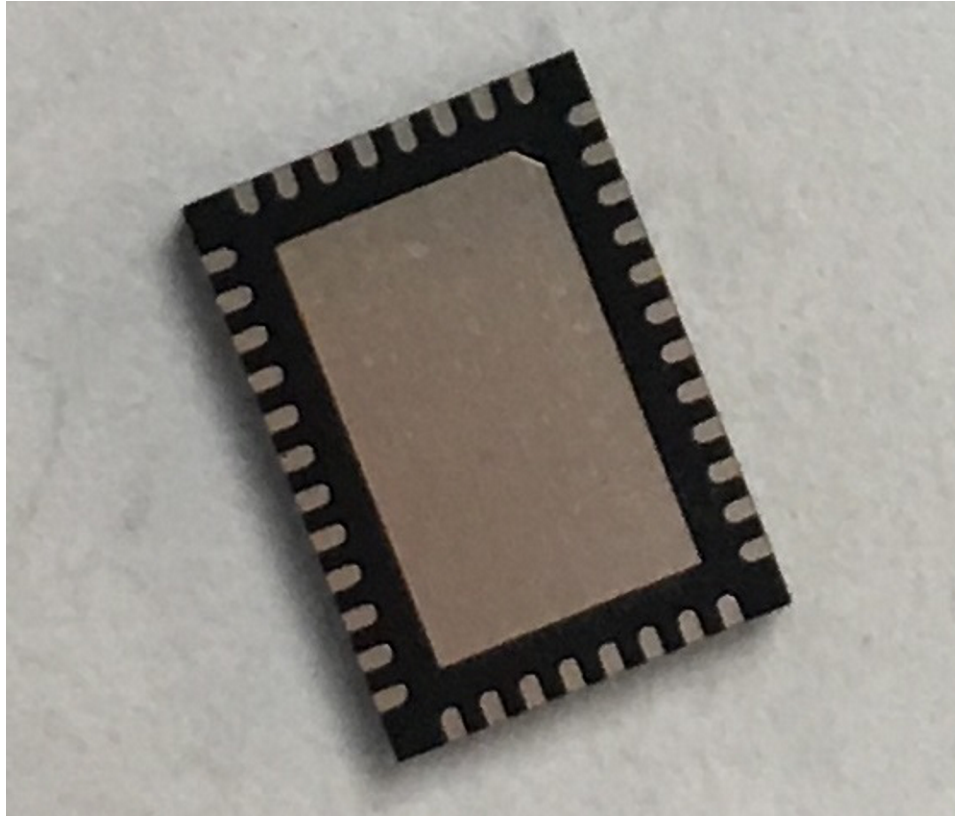
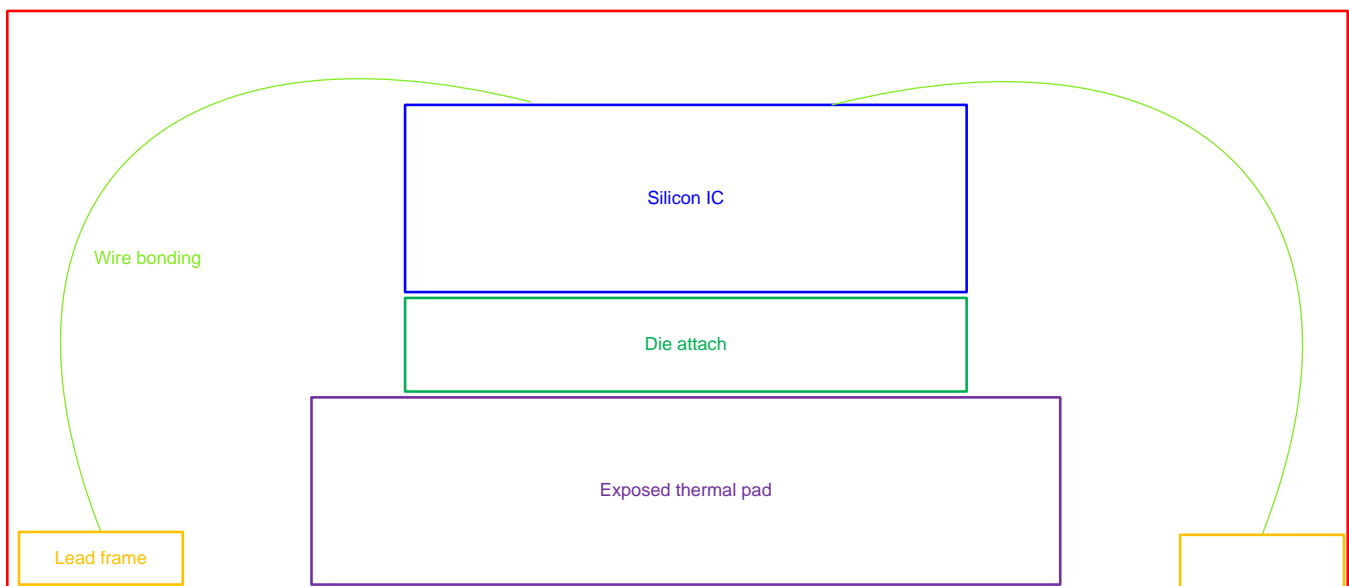


Figure 2. Thermal Pad of Upside Down 40-pin 5-mm x 7-mm QFN



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Figure 3. Section View of QFN Package

Once soldered down on the PCB, the thermal pad and the land pattern forms a strong connection electrically and thermally. It is strongly recommended that multiple thermal vias are placed on the land pattern. The vias should be made through hole and with an electrical connection to system or PCB general ground. The light green vias on the red thermal pad in [Figure 1](#) are drawn to illustrate the above connection. The green land pattern with multiple vias is electrically connected to the system ground. All the ground assignments of the device are connected to the green ground land pattern underneath the device. The single point of ground connection is achieved by tying analog ground, digital ground, gate driver ground, and HB FETs ground together at the thermal pad land pattern, as illustrated in [Figure 1](#).

For TPS53K-integrated FET converters, the uniformed ground connection recommendation is to take advantage of the thermal pad and tie all ground pin assignments to the thermal pad from underneath of the device (see green trace and copper fill in [Figure 1](#)).

2 References

1. Wikipedia, [Quad Flat No-leads package](#), Article

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