Application Report
SLVA874–May 2017

Calculating Output Capacitance to Meet Transient and Ripple Requirements of an Integrated POL Converter Design Based on D-CAPx™ Modulators

Xiao Xu

ABSTRACT

This document provides guidance on how to calculate the amount of output capacitance needed to meet the transient and ripple requirements of a general buck converter design. D-CAPx modulators are used in the example.

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

Since 2010, TI has introduced several generations of TPS53K-integrated FET converters with current ratings ranging from 1.5 A to 40 A. This particular family of devices was created to target the enterprise computing applications, therefore sharing the same competitive performance goals in terms of efficiency, and thermal and transient response. Many considerations were taken to simplify the system design and layout, and to reduce the overall bill of material (BOM).

Table 1 lists the TPS53K converter devices in terms of their applications.

Table 1. TPS53K Device Details

Part Number	Current Rating	V_{IN} Range	V_{OUT} Range	Package Size and Style	Control Topology
TPS53310	3 A	2.9 V to 6 V	0.6 V to 4.2 V	3 × 3 QFN-16	Voltage mode control
TPS53311	3 A	2.9 V to 6 V	0.6 V to 4.2 V	3 × 3 QFN-16	Voltage mode control
TPS53316	5 A	2.9 V to 6 V	0.6 V to 5.5 V	3 × 3 QFN-16	Voltage mode control
TPS53321	5 A	2.9 V to 6 V	0.6 V to 4.2 V	3 × 3 QFN-16	Voltage mode control
TPS53511	1.5 A	4.5 V to 18 V	0.75 V to 5 V	3 × 3 QFN-16	D-CAP2™
TPS53312	3 A	4.5 V to 18 V	0.75 V to 5 V	3 × 3 QFN-16	D-CAP2
TPS53313	6 A	4.5 V to 16 V	0.6 V to 10 V	4 × 4 QFN-24	Voltage mode control
TPS53314	6 A	4.5 V to 25 V	0.6 V to 5.5 V	5 × 7 QFN-40	Voltage mode control
TPS53315	12 A	3 V to 15 V	0.6 V to 5.5 V	5 × 7 QFN-40	D-CAP™
TPS53318	8 A	1.5 V to 22 V	0.6 V to 5.5 V	5 × 6 QFN-22	D-CAP
TPS53319	14 A	1.5 V to 22 V	0.6 V to 5.5 V	5 × 6 QFN-22	D-CAP
TPS53353	20 A	1.5 V to 15 V	0.6 V to 5.5 V	5 × 6 QFN-22	D-CAP
TPS53355	30 A	1.5 V to 15 V	0.6 V to 5.5 V	5 × 6 QFN-22	D-CAP
TPS53513	8 A	1.5 V to 18 V	0.6 V to 5.5 V	3.5 × 4.5 QFN-28	D-CAP3™
TPS53515	12 A	1.5 V to 18 V	0.6 V to 5.5 V	3.5 × 4.5 QFN-28	D-CAP3
TPS53915	12 A	1.5 V to 18 V	0.6 V to 5.5 V	3.5 × 4.5 QFN-28	D-CAP3
TPS548A20	15 A	1.5 V to 20 V	0.6 V to 5.5 V	3.5 × 4.5 QFN-28	D-CAP3
TPS549A20	15 A	1.5 V to 20 V	0.6 V to 5.5 V	3.5 × 4.5 QFN-28	D-CAP3
TPS548B22	25 A	1.5 V to 18 V	0.6 V to 5.5 V	5 × 7 QFN-40	D-CAP3
TPS548D22	40 A	1.5 V to 16 V	0.6 V to 5.5 V	5 × 7 QFN-40	D-CAP3
TPS549D22	40 A	1.5 V to 16 V	0.6 V to 5.5 V	5 × 7 QFN-40	D-CAP3
TPS548D21	40 A	1.5 V to 16 V	0.6 V to 5.5 V	5 × 7 QFN-40	D-CAP3

In a typical D-CAPx converter design, there are three primary considerations for deciding the value of the output capacitance: transient (which includes load step and slew rate of the load step), output ripple, and stability. In applications where the load transient is stringent, the output capacitance is predominantly driven by the transient requirement. Today, tight ripple specification is becoming critical in some high-end, high-performance application-specific integrated circuit (ASIC) and field-programmable gate array (FPGA) designs. The LC output power stage must be designed to meet the ripple criteria. For a D-CAPx-based design, there is also a minimum capacitance requirement in terms of small signal stability. This requirement is in place to prevent subharmonic, multiple-pulsing behavior in all D-CAPx modulators. Even though the minimum capacitance requirement is critical in determining the final output capacitance value, this application report does not intend to provide an in-depth analysis on this criterion. If interested, see the *Design Advantage of D-CAP Control Topology* blog.

2 Design Specifications

In the following section, two calculations are covered. The first calculation is based on ripple specification and the second one is based on transient specification of a converter design example.

Table 2 lists the converter design example specifications using the TPS548D22 device (detailed information of this device is available on TI.com).

Table 2. Design Example Specifications

Parameter	Detailed Description	Specification	Unit
V_{IN}	Input voltage	12	V
V_{OUT}	Output voltage	1	V
V_{PP}	Peak-to-peak output ripple voltage (FCCM)	10	mV
V_{OT}	Transient overshoot – V_{OUT}	+30	mV
V_{UT}	V_{OUT} – transient undershoot	–30	mV
I_{CC_MAX}	Maximum load current	30	A
F_{SW}	Switching frequency	650	kHz
di/dt	Slew rate of load transient	10	A/µs
ΔI	Load step of load transient	18	A

Based on V_{IN}, V_{OUT}, I_{CC_MAX}, and F_{SW} in Table 2, the output inductance value can be calculated fairly quickly. Targeting 20% of I_{CC_MAX} to be the inductor ripple current, the inductance value is calculated to be 0.24 µH. Equation 1 is used to calculate the output inductance value.

$$L_{OUT} = \frac{V_{OUT}}{(V_{IN} \times F_{SW})} \times \frac{V_{IN} - V_{OUT}}{(I_{CC\_MAX} \times K_{IND})} \quad (1)$$

where

- K_{IND} = 20%

Taking into consideration thermal and saturation current, core material, size, and availability, the final inductor is chosen to be the 0.25 µH, DCR 0.615 mΩ, Wurth ferrite P/N 744309024. This inductor is rated for 50-A thermal and 48-A saturation currents.

For a low-duty cycle (V_{IN} – V_{OUT}) >> V_{OUT} D-CAPx-based converter design, the overshoot requirement dominates the output capacitance value.

During load step-up: When the voltage across the inductor is large (V_{IN} – V_{OUT} for undershoot), it takes a relatively shorter time for the inductor to make up the current step. Similarly, a smaller amount of deficit energy is drained from the output capacitors. This is especially true if D-CAPx topology is used. The delay from load step to PWM starts to respond, but is minimized due to the absence of the error amplifier.

During load step-down: When the voltage across the inductor is small (–V_{OUT} for overshoot), it takes a longer time to make up the current step. Therefore, a greater amount of excess energy is dumped into the output capacitors.

Equation 2 is derived based on energy conservation of the LC tank at two different operating current points. Equation 2 can be used to estimate the worst-case capacitance needed for a given dynamic load release.

$$\frac{1}{2} L_{OUT} I_2^2 - \frac{1}{2} L_{OUT} I_1^2 = \frac{1}{2} C_{OUT(min\_over)} \left(V_{OUT} + V_{OT}\right)^2 - \frac{1}{2} C_{OUT(min\_over)} V_{OUT}^2 \quad (2)$$

where

- $C_{OUT(min\_over)}$ is the minimum output capacitance to meet the overshoot requirement.
- L_{OUT} is the output inductance value (0.25 µH).
- I_2 is the initial DC load current + half of the inductor ripple current.
- I_1 is the final DC load current + half of the inductor ripple current.
- V_{OUT} is the output voltage value (1 V).
- V_{OT} is the overshoot requirement (30 mV).

The minimum output capacitance to meet the overshoot requirement is 2640 µF. This application report shows two examples; the first one is with all multilayer ceramic capacitors (MLCCs) and the second one shows a combination of MLCC and POSCAP.

Equation 3 is used to calculate the steady state ripple.

$$V_{PP} = I_{RIPPLE} \times Z_{out\_eq}(F_{sw}) \quad (3)$$

where

- V_{PP} is the ripple voltage specification 10 mV.
- I_{RIPPLE} is the inductor ripple current, calculated to be 5.64 A (see Equation 4).
- Z_{out_eq} (F_{SW}) is the impedance of the output capacitor bank at switching frequency (Ω) (see Figure 1).

$$I_{RIPPLE} = \frac{V_{OUT}}{(V_{IN} \times F_{SW})} \times \frac{V_{IN} - V_{OUT}}{L1} \quad (4)$$

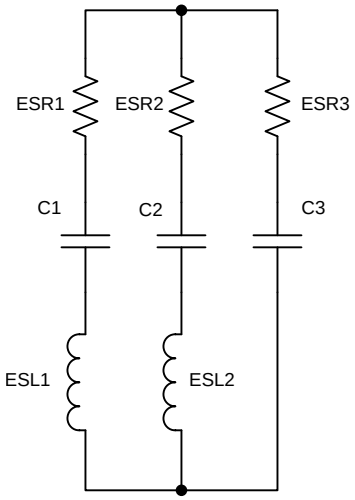

Figure 1. Output Capacitor Combinations

For the purpose of this exercise, both 2-element and 3-element models are used to represent the output capacitors. Therefore, Equation 5, Equation 6, Equation 7, and Equation 8 are used to find the equivalent output impedance value of the capacitor bank.

$$z1(F_{SW}, j) = ESR1 + \frac{1}{(2\pi \times C1 \times F_{SW} \times j)} + 2\pi \times ESL1 \times F_{SW} \times j \quad (5)$$

$$z2(F_{SW}, j) = ESR2 + \frac{1}{(2\pi \times C2 \times F_{SW} \times j)} + 2\pi \times ESL2 \times F_{SW} \times j \quad (6)$$

$$z3(F_{SW}, j) = ESR3 + \frac{1}{(2\pi \times C3 \times F_{SW} \times j)} \quad (7)$$

$$|Z_{out\_eq}(F_{SW})| = \left(\frac{1}{|z1|} + \frac{1}{|z2|} + \frac{1}{|z3|} \right)^{-1} \quad (8)$$

2.1 Example 1

45 × 100 µF 0805 MLCC (2.5 V, X7R, 60% capacitance derating on both DC and AC) is needed to fulfil the overshoot requirement of 30 mV. Using the previous equations, the output impedance at a switching frequency of 650 kHz can be derived as 0.10 mΩ. Using Equation 3, the output ripple voltage is easily calculated to be 1 mV, which is well within the 10 mV peak-to-peak ripple specification (see Table 2).

2.2 Example 2

5 × 100 µF (same as previous) + 5 × 470 µF POSCAP (2.5 V, 6 mΩ ESR) is needed to fulfil the overshoot requirement of 30 mV. Using the same methodology and equations, the output impedance at a switching frequency of 650 kHz can be calculated to be 0.6 mΩ. Using Equation 3, the output ripple voltage is easily calculated to be 3.67 mV, which is also within the 10-mV peak-to-peak ripple specification.

Now that the design can meet the steady state ripple and 18-A load step-down overshoot requirement, we can understand the transient requirement of the load step-up case. Figure 2 shows how D-CAPx topology works in a load transient case.

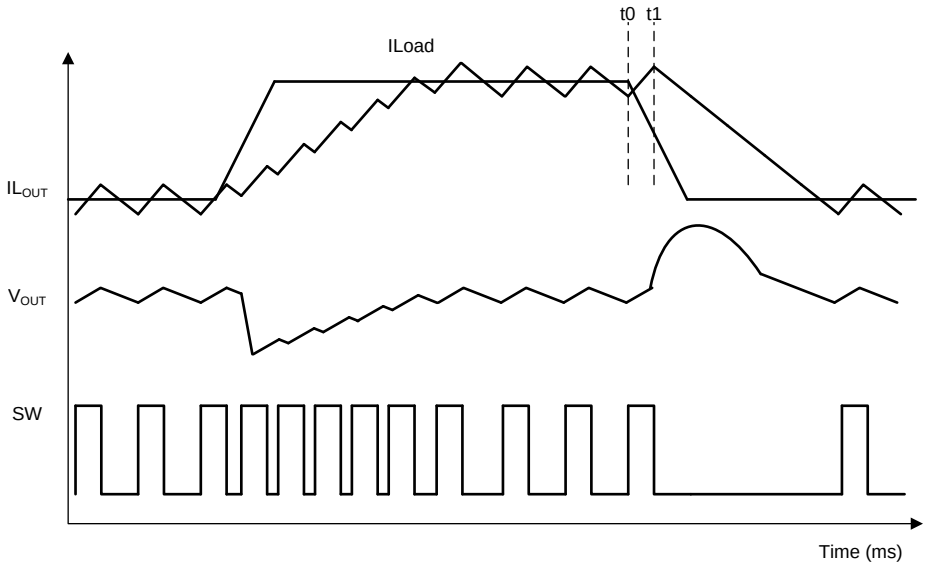

Figure 2. Load Transient Response of D-CAPx Converter

For any load step-up transient, there are two key elements. One element is the load step size and the other is the load slew rate. The output power stage (LC) must be designed to meet the transient requirement. During the load step, the D-CAPx-based converter reacts with reduced off-time response (until the minimum off time is reached) while maintaining the constant on time. The output undershoot is impacted by loop response time, output inductance, capacitance, and minimum off time (if the valley current limit is employed). During the load release, the output overshoot is mainly dominated by output inductance and capacitance. There could also be some extra delay due to the timing of the load release versus the onset of the on-time timer. The worst-case delay could be expected to be 1 × T_{ON} (Duty Cycle x 1 / F_{SW}). In a D-CAPx-based converter design, the overshoot response generally dominates the output LC stage design. Because the transient response is commonly specified symmetrically around the V_{out} set point, if the converter is designed to meet the overshoot specification, that same LC stage is expected to meet the undershoot specification.

Equation 2, the overshoot capacitance, was derived based on the principle of energy balance and conservation in the previous section. The capacitance is the result of the worst-case scenario, assuming the load transient change rate (di/dt slew rate) is infinite. However, the load transient slew rate is generally finite and can vary from mA to A per µs. So how does the slew rate of the load transient impact the amount of required output capacitance needed? In the real-world system and PCB design, the load (microprocessors, ASIC, or FPGAs) is located further away from the bulk capacitors and surrounded by high-frequency decoupling MLCC capacitors. Figure 3 shows this arrangement.

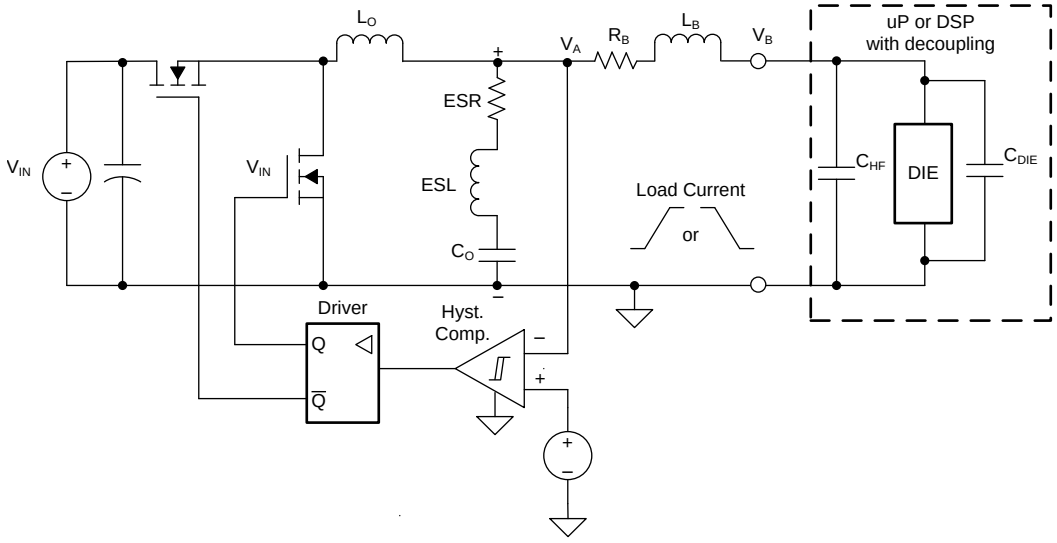

Figure 3. Real-World Output Capacitor Arrangement[2]

The general rule to go by is that if the load transient slew rate is less than or equal to the inductor current charge and discharge slew rate (per switching cycle), then the output voltage change is within the steady state ripple, and therefore as long as the ripple requirement is met, no additional output capacitance is needed.

In the case of an extremely high-load transient slew rate, use Equation 2 to estimate the amount of capacitance needed.

If the load transient slew rate falls in-between, use Equation 9 and Equation 10 to estimate the capacitance needed[1][2][3].

$$N1 = \frac{\frac{ESL1}{t_O} + ESR1 + \frac{t_O}{2 \times C_O1} + (ESR1 + \frac{t_O}{2 \times C_O1}) \times (1 - \frac{t_O}{m \times t_s}) \times KL}{\frac{V_{OT}}{\Delta I} - \frac{L_B}{t_O} - R_B} \quad (9)$$

$$N2 = \frac{\frac{1}{2} \times \left[\frac{m \times t_S}{C_O1} - \frac{t_O}{C_O1} + \left(ESR1 + \frac{ESR1^2 \times C_O1}{m \times t_S} + \frac{m \times t_S}{4 \times C_O1} \right) \times KL + \frac{m \times t_S}{C_O1} \times \frac{1}{KL} \right]}{\frac{V_{OT}}{\Delta I} - R_B} \quad (10)$$

where

- m: For worst-case, step-down transient (in the example), m = 1 – D (D = V_{out} / V_{in}). For worst-case, step-up transient, m = D
- KL: Ratio of inductor ripple current and load step transient, I_{RIPPLE} / ΔI
- C_O1: Individual output bulk capacitor, such as the one derived from the previous calculation, 470 µF, 2.5 V
- ESR1: Individual output bulk capacitor, such as the one derived from the previous calculation, 6 mΩ
- ESL1: Individual output bulk capacitor, such as the one derived from the previous calculation, 1.2 nH
- t_S: Switching frequency, 1 / F_{sw}, (where F_{sw} = 650 kHz)
- R_B: Trace impedance in Figure 3. In this example, we assume R_B 1µΩ (negligible)

Equation 9 is derived for the extreme value of output voltage transient (overshoot) where it includes the effect of output capacitor and supply-path parasitics. Equation 10 is based on resistive components, such as the ESR, trace resistance, output capacitor, inductor, and the converter characteristics, including the switching frequency and type of control. In this application note, we focus on the calculation obtained using Equation 10. For more detailed derivation and explanations on how Equation 9 and Equation 10 are obtained, used, and characterized, see Section 3.

By using Equation 10, we can calculate the total output capacitance to be 2060 µF, assuming an ideal trace impedance of 1µΩ (R_B). Because Equation 10 is derived based on the ideal control method/topology which incurs no delay; in case of load release, the high side is immediately turned off when the load release occurs. Because this application note is mainly written for DCAPx modulators, a slight adjustment is necessary to include the effect of delays. Figure 4 shows the delay effects of a DCAPx modulator. Two delays are commonly found in DCAPx control; one is the comparator delay (t_{DEL}) and the other is on time delay. In any DCAPx control, the on time is always constant. If the load release occurs during the very beginning of the on time, the on time must complete its preprogrammed duration before being turned off. The additional charge increases the peak voltage by –Qextra / Co_total. For the TPS548D22 family of devices, the comparator delay time is about 100 ns and t_{ON} can be calculated by Equation 11, which is 128 ns.

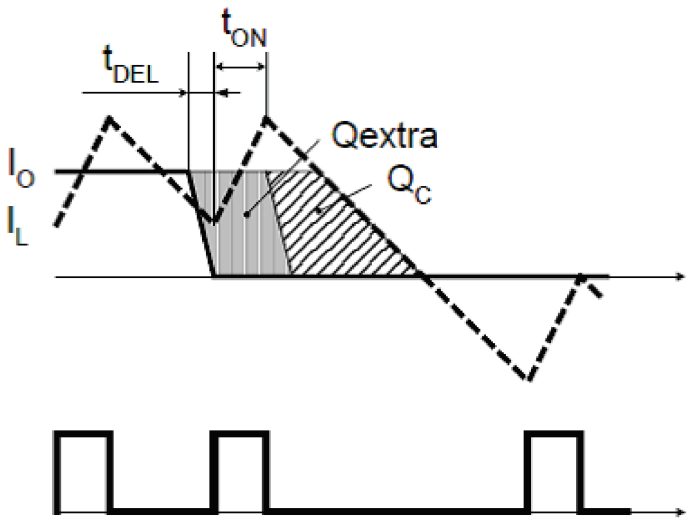

Figure 4. Constant on Time With Delays[3]

$$t_{ON} = (V_{OUT} / V_{IN}) \times T_S \quad (11)$$

$$Q_{DEL} = (t_{ON} + t_{DEL}) \times \Delta I \quad (12)$$

$$\Delta V = Q_{DEL} / 2060\ \mu F \quad (13)$$

By employing Equation 11, Equation 12, and Equation 13 we derived the additional output voltage due to the control topology to be 2 mV. To simplify the calculation, we deduct the 2 mV from the transient voltage allowance, and the new transient voltage deviation is 28 mV. Using Equation 10 again, we can calculate the output capacitance to be 2210 µF. The total output capacitor needed to meet the transient requirement is 4 × 470 µF (POSCAP) + 6 × 100 µF (MLCC).

3 References

1. R. Miftakhutdinov, *Analysis of Synchronous Buck Converter with Hysteretic Controller at High Slew-Rate Load Current Transients*, Proc. of High-Frequency Power Conversion Conference (1999), pp. 55-69
2. R. Miftakhutdinov, *Analysis and Optimization of Synchronous Buck Converter at High Slew-Rate Load Current Transients*, Proc. of Power Electronics Specialist Conference (2000) pp. 714 – 720
3. R. Miftakhutdinov, *An Analytical Comparison of Alternative Control Techniques fo Powering Next-Generation Microprocessors*

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265