Application Report
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Creating an Inverting Power Supply Using a Synchronous Step-Down Regulator

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ABSTRACT

Some applications require a high current negative output voltage to be generated from a positive input voltage. Applications often requiring a negative output voltage are medical ultrasound scanners, semiconductor test equipment, RADAR, oscilloscopes (DSO) and massive MIMO (active antenna systems). This application report presents a solution for creating an inverting power supply using a synchronous buck converter. The purpose of this application report is to discuss how to create a negative power supply using a switching regulator (buck).

The solution schematic is given along with component selection criteria and equations, so that designers can appropriately scale the solution to their own requirements. The document also includes a sample design implementation along with captured waveforms.

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Trademarks

SWIFT is a trademark of Texas Instruments.

1 Description of Application

This application report discusses creating an inverting power supply using a synchronous step-down regulator. The design generates a negative voltage from a positive input voltage. Applications that often require an inverted output voltage from a positive input voltage are those with amplifiers and data converters.

Using a synchronous topology has certain advantages over a nonsynchronous topology like higher efficiency at low voltages. The synchronous topology stays in continuous conduction mode (CCM) even at very low currents as opposed to a nonsynchronous topology which runs into discontinuous conduction mode (DCM) when the current through the inductor is reduced to zero. The disadvantages of nonsynchronous topology in DCM are that it has a slow transient response, it needs slower compensation for the DCM shift, and it has additional component on the EVM board. These disadvantages can be eliminated by using a synchronous topology.

2 Design Restrictions

The design restrictions for the application are listed in Table 1. To power up the board, the input voltage needs to be higher than the minimum required voltage for the device. The maximum allowable output voltage is limited by the maximum Vdev (voltage across the device, between the VIN pin and GND pin on the IC) minus the maximum input voltage. Because the MOSFETs are internal to the IC, the maximum load current cannot be more than the maximum current through the internal switches.

Table 1. Electrical Characteristics for the Inverting Power Supply

INVERTING POWER SUPPLY RESTRICTIONS		SYNCHRONOUS DEVICE USED	TPS54620
Vin (min)	>	Vdev (min)	(4.5 V)
Vin (max) + Vout	<	Vdev (max)	(17 V)
Iout (max)	<	Iswitch (max)	(7 A)

3 Solution and Part Used

To convert a synchronous buck regulator (as shown in Figure 1) into a buck boost topology (as shown in Figure 2), the inductor and output capacitor are connected just like in a buck converter, but the ground and output voltage test points are reversed in order to achieve a negative output voltage.

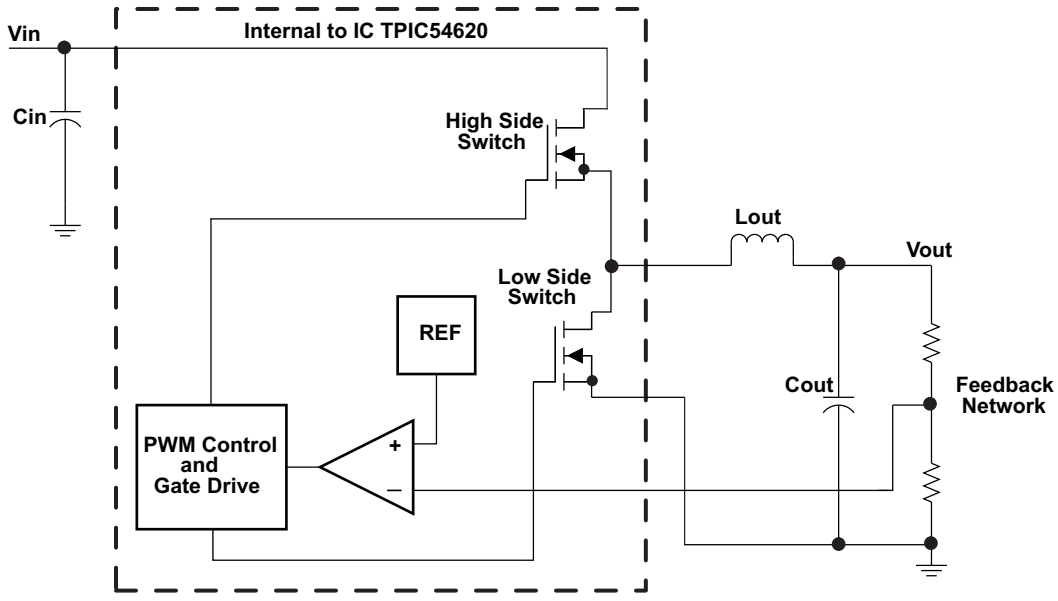

Figure 1. Buck Topology

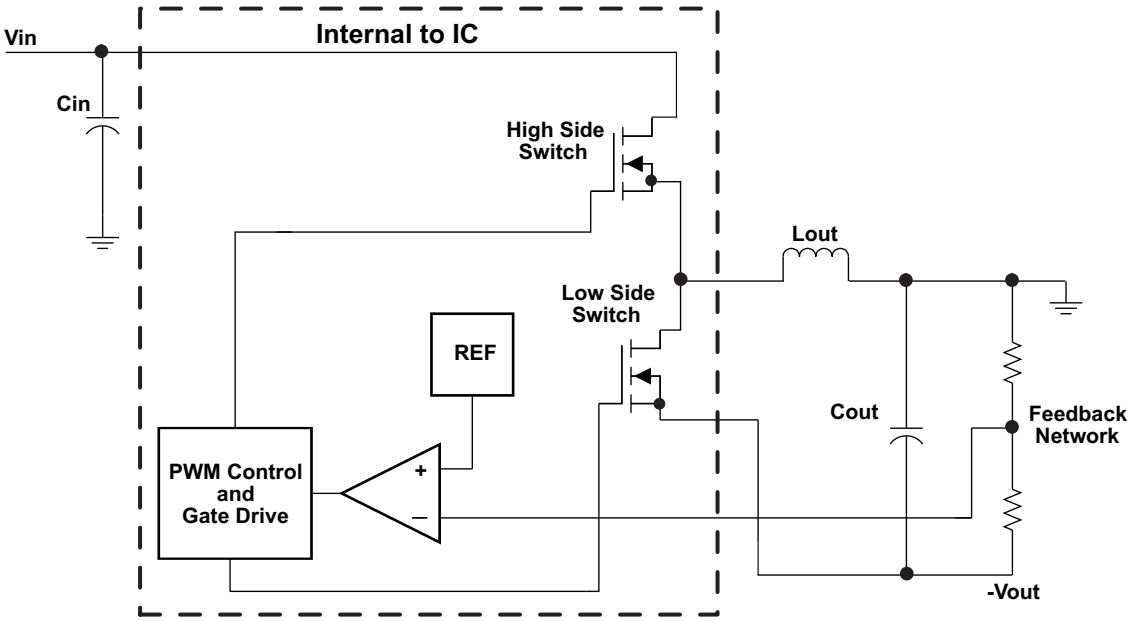

Figure 2. Inverting Buck-Boost Topology

The sample design to create a synchronous inverting power supply is presented in the next section using the TPS54620, which is a 4.5-V to 17-V input, 6-A synchronous step-down SWIFT™ converter. The sample device is used to illustrate the concept, but any buck regulator can be configured this way provided it matches the requirements previously listed.

The electrical requirements of the sample design are listed in Table 2.

Table 2. Inverting Power Supply Requirements

VARIABLE	DESCRIPTION	RANGE / VALUE
Vin	Input Voltage	5 V nominal 4.5 V to 5.5 V
Vout	Output Voltage	–5 V
Vout	Output Voltage Ripple	< 0.5%
Iout	Output Current	2 A
fsw	Switching Frequency	300 kHz

4 Design Restrictions

The design restrictions for the application are listed in Table 3. To power up the board, the input voltage needs to be higher than the minimum required voltage for the device. The maximum allowable output voltage is limited by the maximum Vdev (voltage across the device, between the VIN pin and GND pin on the IC) minus the maximum input voltage. Because the MOSFETs are internal to the IC, the maximum load current cannot be more than the maximum current through the internal switches.

Table 3. Electrical Characteristics for the Inverting Power Supply

Inverting Power Supply Restrictions		Synchronous Device Used	TPS54620
Vin (min)	>	Vdev (min)	(4.5 V)
Vin (max) + Vout	<	Vdev (max)	(17 V)
Iout (max)	<	Iswitch (max)	(7 A)

5 Design Procedures

This section enlists the procedure to design an inverting power supply using the TPS54620 (synchronous step-down SWIFT™ converter). The schematic for the design is presented in Figure 3.

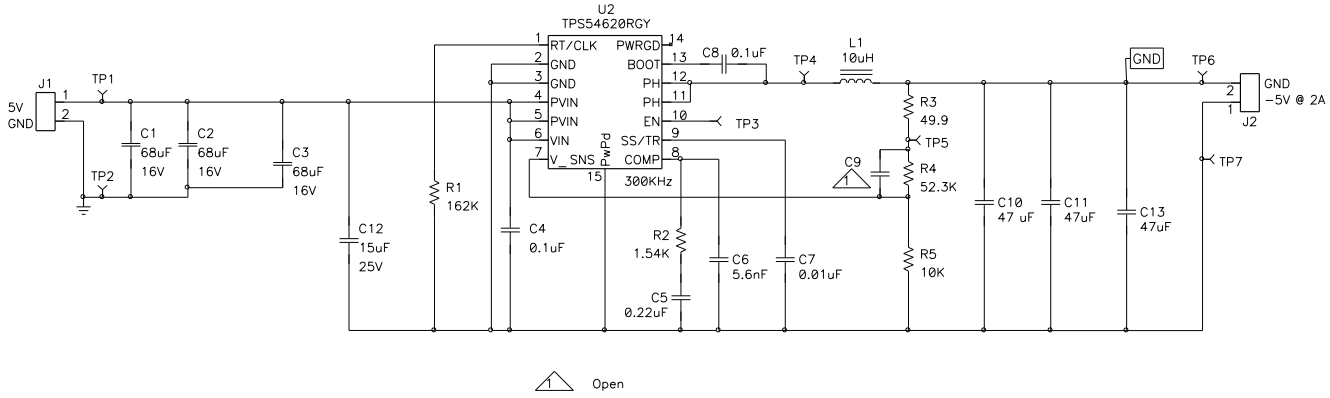

Figure 3. Inverting Power Supply Schematic

5.1 Output Voltage

The difference in the maximum input voltage, Vin (max), and the output voltage, V_O, must not exceed the maximum operating device voltage of the regulator. For the TPS54620, the maximum operating device voltage, Vdev (max), is 17 V.

$$\text{Vin (max)} \geq \text{Vdev (max)} + \text{Vout} \quad (1)$$

$$R4 = R5 \times \left(-\frac{\text{Vout}}{\text{Vref}} - 1 \right) \quad (2)$$

Because Vout for the sample design is –5 V and using Equation 1, the maximum input voltage for the power supply can be as high as 12 V, easily supporting the 5.5-V maximum input requirement in Table 2. Use Equation 2 to determine R4 for the desired output voltage, set R5 equal to 10 kΩ and Vref to 0.8 V for the TPS54620. R4 equals 52.5 kΩ (52.3-kΩ standard value).

5.2 Input Voltage Range

The operating input voltage, Vin (min) of the power supply must be greater than the minimum device voltage, Vdev (min). For TPS54620, the Vdev (min) is 4.5 V. The minimum input voltage requirement for the power supply is 4.5 V, thus, satisfying Equation 3.

$$\text{Vin (min)} \geq \text{Vdev (min)} \tag{3}$$

5.3 Duty Cycle

The ideal duty cycle for the inverting power supply is shown in Equation 4, neglecting the losses of the power switch and inductor. The output voltage, Vout, is negative and the input voltage, Vin, is positive, yielding a positive result for Equation 4.

$$D = \frac{-\text{Vout}}{\text{Vin} - \text{Vout}} \tag{4}$$

The maximum duty cycle, Dmax, is calculated by using the minimum input voltage, Vin (min), as substituted for input voltage, Vin in Equation 4. Assuming 4.5 V for Vin (min) and a Vout of –5 V, the maximum duty cycle, Dmax, is 0.53. Similarly, Dmin is evaluated by using maximum input voltage, Vin (max), and is calculated to be 0.48.

5.4 Output Current

To estimate whether the selected switching regulator is capable of delivering the output current, use Equation 5. The user must know the device's (TPS54620) minimum current limit, Icl (min) (7 A), maximum duty cycle, Dmax, and estimate the inductor ripple current value, ILripple. Using Equation 5, the maximum allowable output current for the design is 3.13 A, which is higher than the needed 2 A.

$$\text{Iout (max)} \leq \left(\text{Icl(min)} - \frac{\text{ILripple}}{2} \right) \times \left(1 - \text{Dmax}\right) \tag{5}$$

5.5 Operating Frequency

The first step is to decide on a switching frequency for the regulator because of the tradeoff between higher and lower switching frequencies. Higher switching frequencies may produce a smaller solution size using lower valued inductors and smaller output capacitors, compared to a power supply than switches at a lower frequency. However, higher switching frequency causes extra switching losses, which hurt the converter's efficiency and thermal performance.

In this design, a moderate switching frequency of 300 kHz is selected to achieve both a small solution size and a high-efficiency operation.

5.6 Inductor

To determine the inductor value, calculate the average inductor current, ILavg, at the maximum output current and minimum input voltage using Equation 6. Assuming maximum output current, Iout as 2 A and using maximum duty cycle Dmax, ILavg is 4.22 A.

The inductor value is calculated, Equation 7, using a ripple current that is 25% of the average inductor current. Using the Dmin to calculate the minimum inductance value gives the largest inductance. Assuming Vin (max) of 5.5 V, Iout of 2 A, and a $f$sw of 300 kHz, the Lo is calculated as 8.22 µH. The nearest standard inductor of 10 µH is used for the inductor. The inductor saturation current must be greater than the 4.62 A of peak current calculated in Equation 8. The inductor rms current must be greater than 4.01 A calculated in Equation 9.

$$ILavg = \frac{Iout}{1 - Dmax} \quad (6)$$

$$Lo = \frac{Vin(max) \times Dmin}{(fsw \times ILavg \times 0.25)} \quad (7)$$

$$ILpeak = \frac{Iout}{1 - Dmax} + \frac{Vin(min) \times Dmax}{2 \times fsw \times Lo} \quad (8)$$

$$ILrms = \sqrt{\left(\frac{Iout}{1 - D}\right)^2 + \frac{1}{12} \times \left(\frac{Vin \times D}{fsw \times Lo}\right)^2} \quad (9)$$

5.7 Output Capacitor

The output capacitor must supply the current when the high-side switch is on. Use the minimum input voltage to calculate the output capacitance needed. This is when the duty cycle and the peak-to-peak current in the output capacitor are the maximum. Using the 0.5% voltage ripple specification, Vout, and Equation 10, Co (min) is 140 µF. Assuming the 0.5% voltage ripple and maximum duty cycle, the Rc, equivalent series resistance must be less than 5.41 mΩ, using Equation 11. The rms current for the output capacitor is 2.11 A using Equation 12. Three 47 µF, 10 V X7R in parallel are used for the output capacitor because of the low ESR and size. The output capacitor is derated by 15% because of the dc voltage.

$$Co\ (min) \geq \frac{Iout(max) \times Dmax)}{fsw \times \Delta Vout} \quad (10)$$

$$Rc \leq \frac{\Delta Vout}{\frac{Iout}{1 - Dmax} + \frac{Vin(min) \times Dmax}{2 \times fsw \times Lo}} \quad (11)$$

$$Icorms = Iout\ (max) \times \sqrt{\frac{Dmax}{1 - Dmax}} \quad (12)$$

5.8 Power Dissipation in Package

The power dissipation in the package is dominated by the conduction losses and switching losses of the power switch and must not exceed the limitations of the package. The conduction and switching losses are calculated using Equation 13. The conduction losses are a function of the duty cycle, D, inductor rms current, ILrms, and on resistance, Rhs and Rls. The switching losses are a function of the turnon, tr, and turnoff, tf, times, switching frequency, output current, and input and output voltage. Pdevice is 0.6613 W assuming a tr and tf of 25 ns.

$$Pdevice = D \times ILrms^2 \times Rhs + (1 - D) \times ILrms^2 \times Rls + \frac{1}{2} \times (Vin - Vout) \times \left(\frac{Iout}{1 - D}\right) \times (tr + tf) \times fsw \quad (13)$$

5.9 Input Capacitors

The input capacitors between the PVIN pins and system ground are used to limit the voltage ripple of the input supply.

Equation 14 to Equation 17 are used to estimate the capacitance, maximum ESR, and current rating for the input capacitor, Ci. Using Equation 14, the estimated average input current is 2.22 A. Using Equation 15 and Equation 16, the minimum required input capacitance is 165 µF and the maximum ESR is 20 mΩ. Using Equation 17, the input capacitor needs at least 2.32-A current rating. Three 68 µF, 10 V X7R in parallel are used for the output capacitor because of the low ESR and size.

$$Iin\ (avg) = \frac{Iout \times Dmax}{(1 - Dmax)} \quad (14)$$

$$Ci = \frac{Iin(avg)}{fsw \times 0.01 \times Vin\ (min)} \quad (15)$$

$$ESRci \leq \frac{0.01 \times Vin\,(min)}{Iin\,(avg)} \tag{16}$$

$$Icirms = \sqrt{\left((ILpeak - Iin(avg))^2 + \frac{\left(\frac{Vin(min) \times Dmax}{Lo \times fsw}\right)^2}{12}\right) \times Dmax + Iin(avg)^2 \times (1 - Dmax)} \tag{17}$$

5.10 Bypass Capacitor

The TPS54620 needs a tightly coupled, ceramic bypass capacitor, connected to the VIN and GND pins of the device. Because the device GND is the power supply output voltage, the voltage rating of the capacitor must be greater than the difference in the maximum input and output voltage of the power supply.

A minimum of 4.7 µF from the VIN pin to GND is recommended for the TPS54620, Cbp is chosen as 15 µF. Another 0.1-µF capacitor has been added as a bypass capacitor to clear high-frequency noise. This capacitor creates an AC path from the input voltage to the output voltage. As a result, transients on the input voltage rail can potentially also appear on the output voltage. For example, when the input voltage ramps up. To minimize this effect, Cbp should be kept relatively small, near the minimum recommended capacitance.

5.11 Slow-Start Time

Placing a small ceramic capacitor on the SS/TR to the chip GND (that is, system Vout) adjusts the slow-start time on the TPS54620. The slow-start capacitor is calculated using Equation 18. The equation assumes a 2.3-µA pullup sourcing current and 10% to 90% measurement for time Tss. Using Equation 18, Css is evaluated as 10 pF.

$$Css = \frac{tss \times 2.3 \times 10^{-6}}{0.8} \tag{18}$$

5.12 Frequency Set Resistor

The switching frequency is set with a resistor, RT, from the RT/CLK pin to the GND of the TPS54620 device. Using Equation 19, the frequency set resistor is 161 kΩ (162-kΩ standard value).

$$RT(k\Omega) = \frac{48000}{fsw(kHz)^{0.997}} - 2 \tag{19}$$

5.13 Frequency Response of the Inverting Regulator

Using a buck regulator as an inverting buck-boost regulator changes the feedback loop characteristic. So, a different design method is needed. The inverting power supply transfer function has two zeroes and a pole. Equation 20 is a simplified transfer function of an inverting power supply. The ESR zero, fz1, is the same as in a buck regulator, Equation 21, and is a function of the output capacitor and its ESR. The other zero is a right half plane zero, fz2. The frequency response of the fz2 results in an increasing gain and a decreasing phase. The fz2 frequency is a function of the duty cycle, output current, and the inductor. Equation 22 calculates the minimum frequency of the fz2 which is used to determine the crossover frequency. The dominant pole, fp1, is a function of the load current, output capacitor, and duty cycle, see Equation 23. Kbb is the dc gain and is used to calculate the frequency compensation components. The gmps variable is the transconductance of the power stage, which is 16 A/V for the TPS54620.

The fz1 is estimated to be 265 kHz. The output capacitor is derated by 15% because of the dc voltage, and the ESR is assumed to be . The fz2 is estimated to be 16.93 kHz. Assuming resistance of the inductor, Rdc is 19 mΩ. The fp1 is estimated to be 796 Hz assuming a nominal duty cycle. Kbb is calculated as 13.33 V/V using Equation 24, assuming nominal input voltage and gmps as 16 A/V .

$$T(s) = Kbb \times \frac{\left(1 + \frac{s}{2 \times \pi \times fz1}\right) \times \left(1 + \frac{s}{2 \times \pi \times fz2}\right)}{\left(1 + \frac{s}{2 \times \pi \times fpl}\right)} \quad (20)$$

$$fz1 = \frac{1}{(Rc \times Co \times 2 \times \pi)} \quad (21)$$

$$fz2 = \frac{(1 - Dmax)^2 \times \left(\frac{-Vout}{Iout}\right) + Rdcx\left((1 - Dmax) - Dmax\right)}{Dmax \times Lo \times 2 \times \pi} \quad (22)$$

$$fp1 = \frac{1 + D}{\left(\left(-\frac{Vout}{Iout}\right) \times Co \times 2 \times \pi\right)} \quad (23)$$

$$Kbb = \frac{Vin \times \left(-\frac{Vout}{Iout}\right)}{\left(Vin + 2 \times (-Vout)\right)} \times gmps \quad (24)$$

The crossover of the power supply should be set between the $fp1$ and 1/3 of $fz2$ frequencies. It is recommended to start with the crossover frequency, fco, given by Equation 25. The fco is estimated to be 3.67 kHz.

$$fco = \left(fp1 \times fz2\right)^{0.5} \quad (25)$$

The compensation resistor, Rcomp, needed to set the compensation gain at the fco frequency is calculated using Equation 26. The Vref is 0.8 V and gmea is 1300 µA/V for the TPS54620.

$$Rcomp = \left(\frac{fco}{Kbb \times fp1}\right) \times \left(\frac{-Vout}{Vref \times gmea}\right) \quad (26)$$

Rcomp is calculated using Equation 26 and is equal to 1.66 kΩ. Use the nearest standard value of 1.54 kΩ. The compensation zero is set to 1/2 of the dominant pole, $fp1$. To calculate the compensation zero capacitor, Czero, use Equation 27. Equation 27 gives 0.26 µF; use the next larger standard value which is 0.22 µF. The compensation pole is set to equal the RHP zero, $fz2$. Use Equation 28, to calculate the frequency compensation pole, Cpole, which gives 6.10 nF. The next standard value is 5.6 nF.

$$Czero = \frac{1}{\left(\frac{fp1}{2}\right) \times 2\pi \times Rcomp} \quad (27)$$

$$Cpole = \frac{1}{fz2 \times 2\pi \times Rcomp} \quad (28)$$

5.14 Synchronizing to an External Clock

The TPS54620 has a CLK pin that can be used to synchronize the power supply switching frequency to an external system clock. A level shift circuit needs to be used to translate a system ground reference clock signal to the device's ground.

6 Evaluation Results

Figure 4 to Figure 10 show the experimental test results of the Figure 1 design.

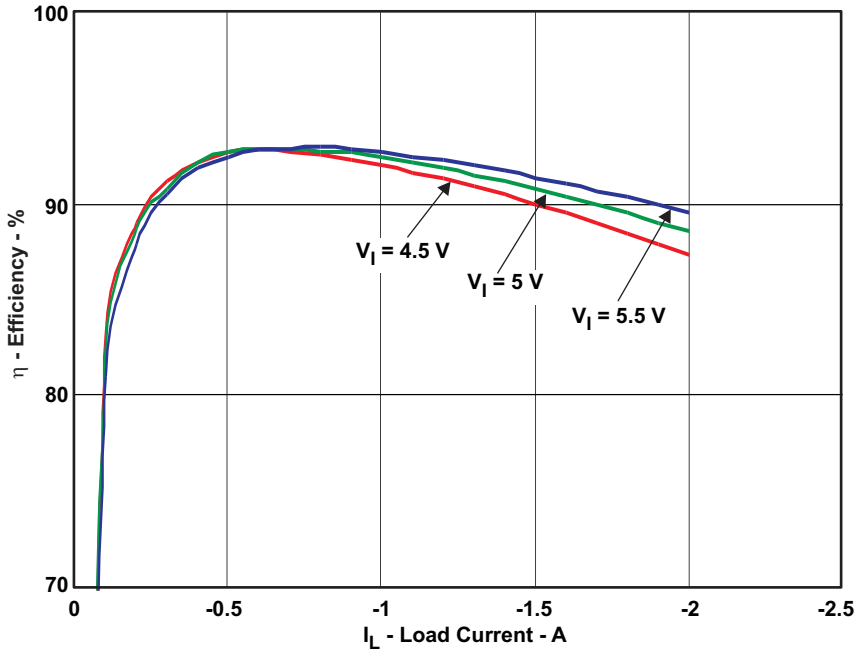

Figure 4. Efficiency Curve

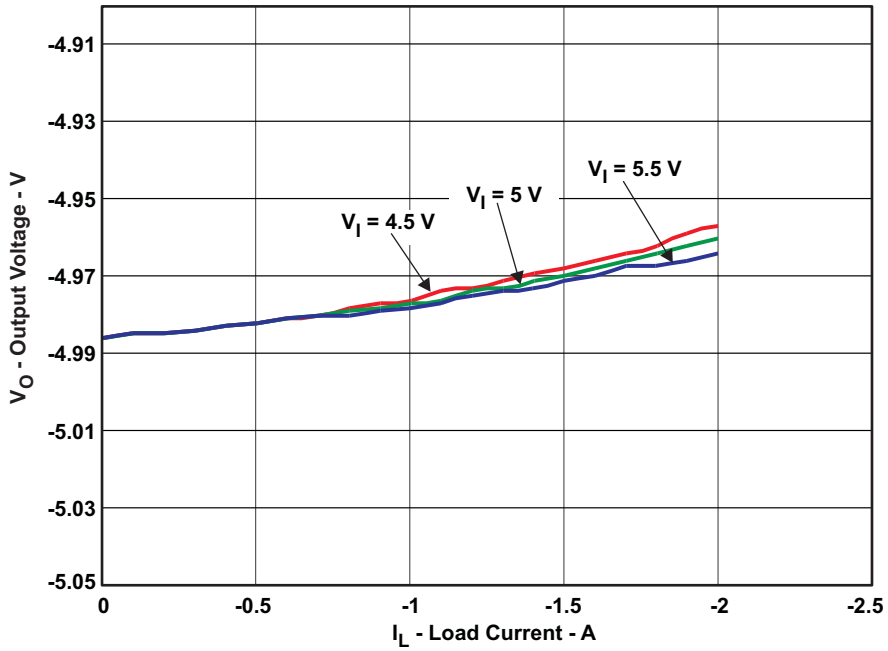

Figure 5. Load Regulation

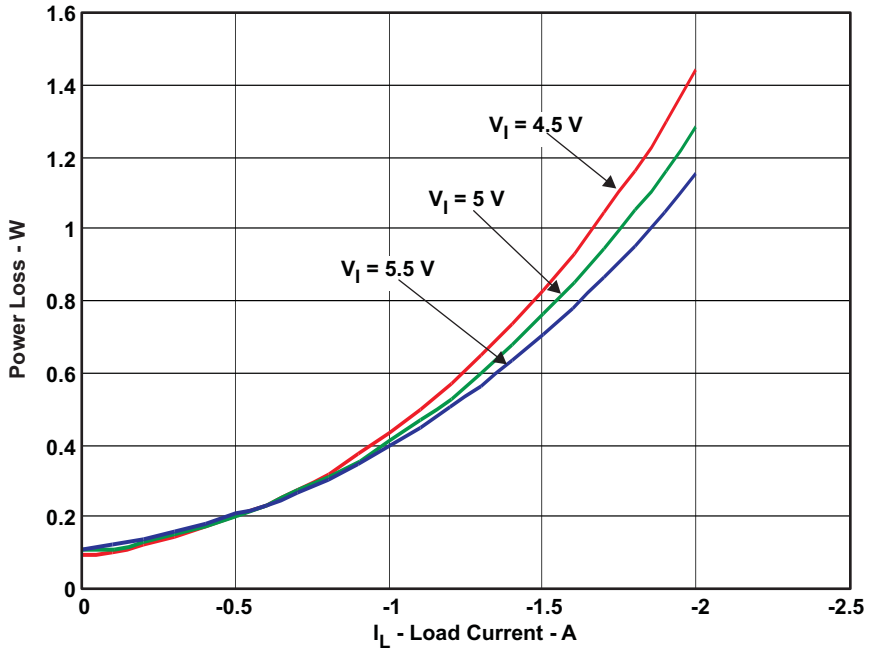

Figure 6. Power Loss vs Load Current

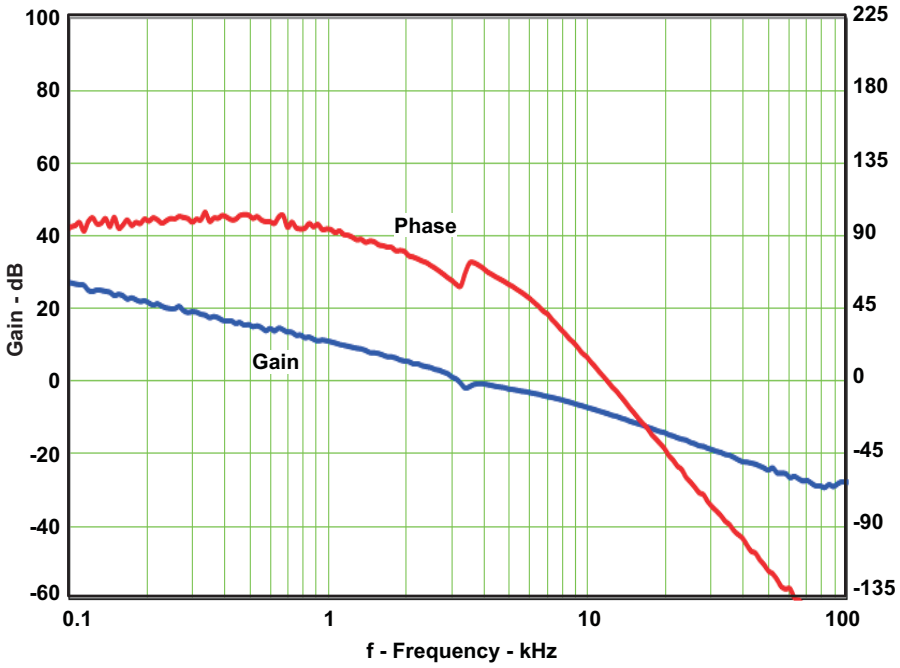

Figure 7. Bode Plot
(BW = 3.2 kHz, PM = 59.4°) (V_{IN} = 5 V, V_{OUT} = –5 V, I_{OUT} = 2 A)

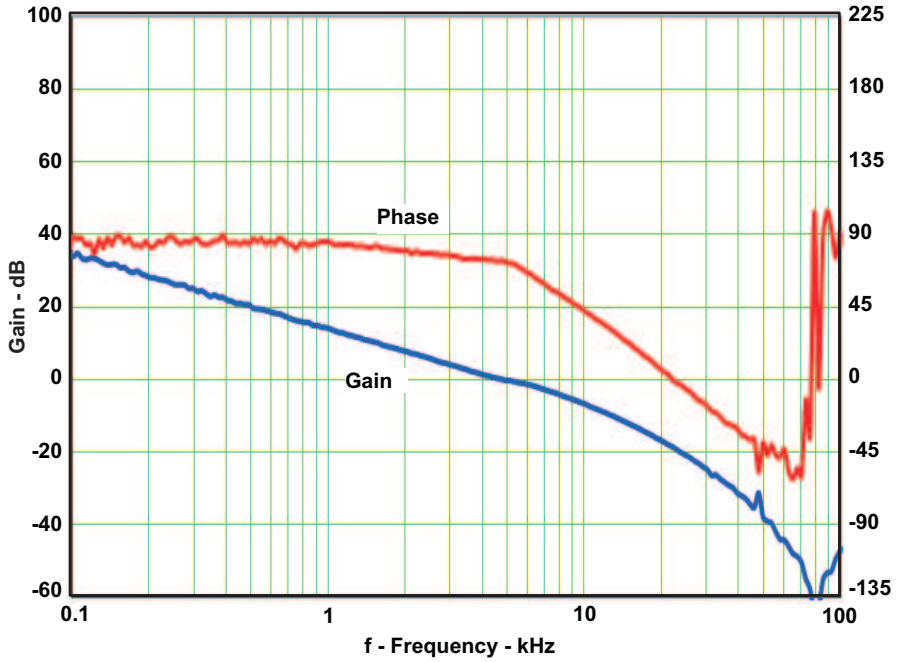

Figure 8. Bode Plot
(BW = 4.9 kHz, PM = 72.5°) (V_{IN} = 5 V, V_{OUT} = –5 V, I_{OUT} = 0 A)

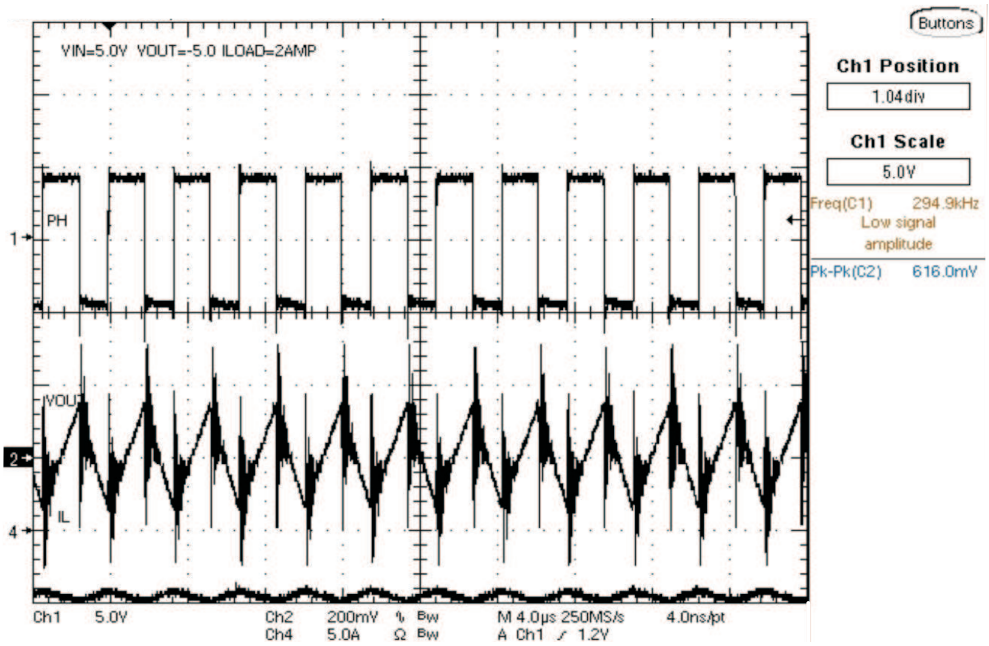

Figure 9. Switch Node
(V_{IN} = 5 V, V_{OUT} = –5 V, I_{OUT} = 0 A)

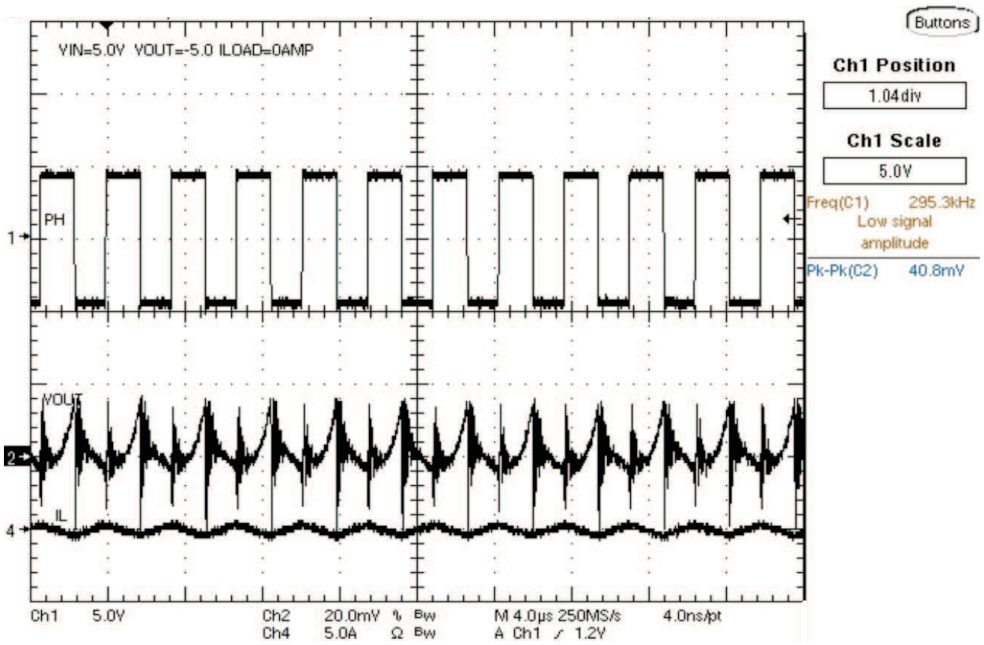

Figure 10. Switch Node Rising
(V_{IN} = 5 V, V_{OUT} = –5 V, I_{OUT} = 0 A)

7 References

1. *Using a Buck Converter in an Inverting Buck-Boost Topology*, (SLYT286), 4Q 2007 Analog Applications Journal, Texas Instruments
2. *Using the TPS5430 as an Inverting Buck-Boost Converter* application report (SLVA257)
3. *Create an Inverting Power Supply From a Step-Down Regulator* application report (SLVA317)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (June 2012) to B Revision	Page
• Added second sentence to Abstract	1
• Changed third sentence of *Section 1*	3
• Changed polarity of capacitor in Figure 2	4
• Added content to last paragraph in *Section 5.10*	8
• Changed first sentence of *Section 5.13*	8
• Changed "ESR is assumed to be 5" to "ESR is assumed to be 5 mΩ"	8
• Changed "Rdc is 19 m" to "Rdc is 19 mΩ"	8

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