Application Report
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Simple Solution for Input Filter Stability Issue in DC/DC Converters

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ABSTRACT

Input filters are a common solution to conducted EMI challenges in DC/DC converters. The most common form of EMI input filter is a simple π-type filter consisting of two capacitors and one inductor. The filter can significantly attenuate the harmonics on the input power line, which means better conducted EMI performance. It is well-known that the component values depend on the expected attenuation. However, there must be more considerations since inappropriate values can cause oscillation on the input. Through the introduction of a real-world design scenario, this application report shows the input oscillation phenomenon, analyzes why the loop becomes unstable after applying the input filter, and discusses methods to fix this issue.

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1 Introduction

LMR14050 is a 4-V to 40-V wide input voltage 5-A step down DC/DC converter. The schematic shown in Figure 1 is designed to output 5 V at 5-A full loading based on the LMR14050. For better EMC performance, a π-type input filter is applied on the input line.

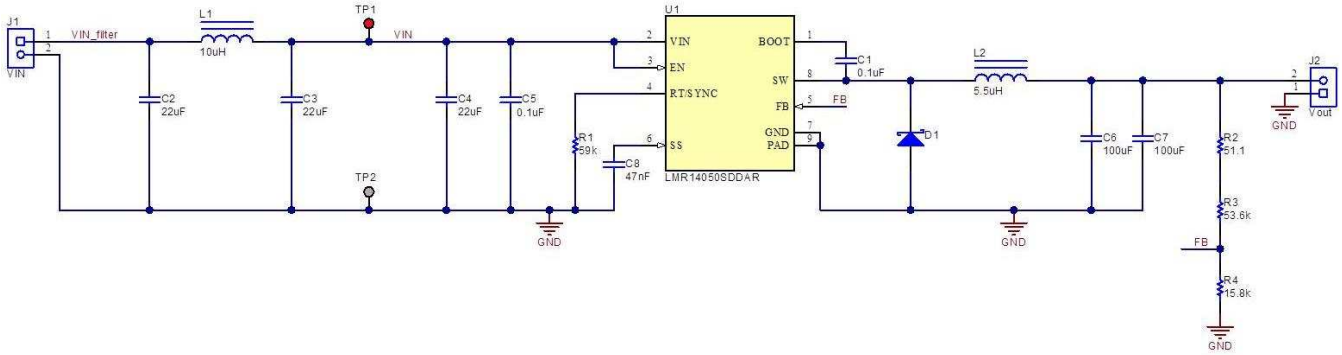

Figure 1. Schematic of LMR14050 Application Circuit with EMI filter (V_{out} = 5 V, I_{out_max} = 5 A)

When the 9-V input voltage is applied across TP1 and TP2,(when the input filter is not involved in the circuitry), it worked well as shown in Figure 2. When the input is applied on input terminal J1, the circuit can work normally with the input filter in light loads. However, when the load current exceeded 3.5 A, the circuit went unstable. Figure 3 shows the input oscillation clearly with bench test waveform.

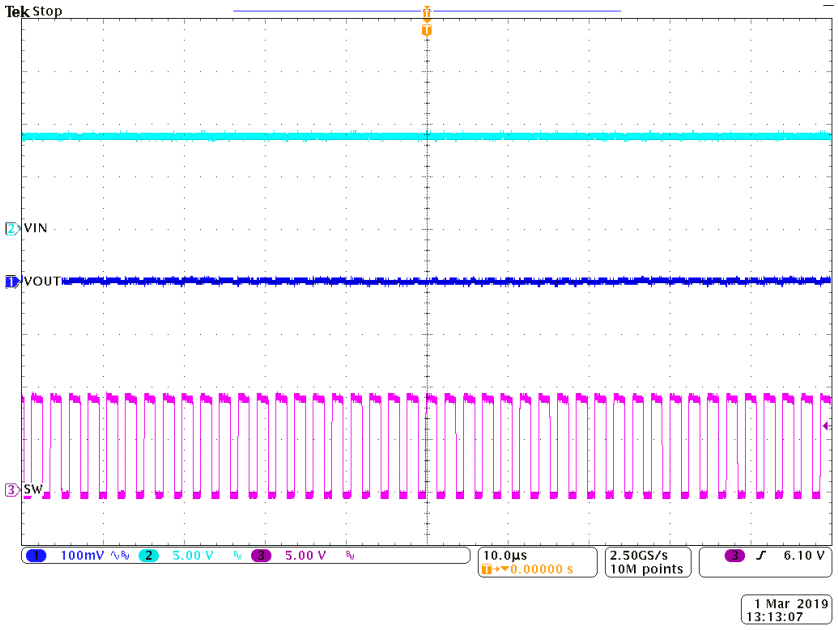

Figure 2. Operating Waveform at VIN = 9 V, I_{out} = 5 A Without Input Filter

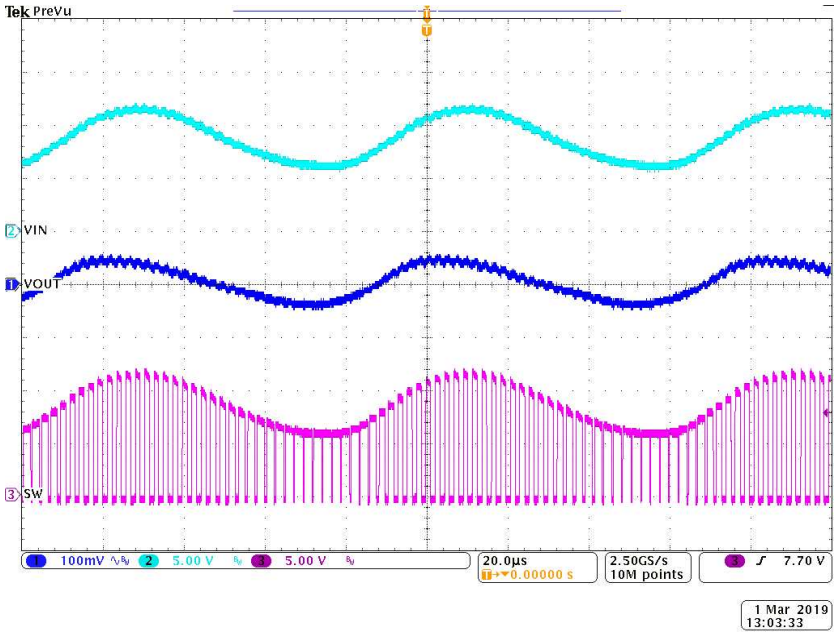

Figure 3. Operating Waveform at VIN = 9 V, I_{out} = 5 A with Input Filter

By comparing the waveforms before and after applying the EMI input filter, the problem was addressed as an instability issue caused by the filter. It is clear that the poorly designed EMI input filter led to a stability issue under some specific operating conditions. This application report aims at revealing this kind of instability phenomenon, analyzing the root cause, and providing solutions for the stability issue caused by π-type EMI filter.

2 Instability Analysis

2.1 Increment Input Impedance of dc/dc Converter

Before any DC/DC modeling effort and mathematical induction, try to understand the issue by intuition. For the input power P_{IN} and output power P_{OUT} of DC/DC converter, you have:

$$P_{out} = \eta \cdot P_{in} \tag{1}$$

Expend P_{IN} and P_{OUT} and you have:

$$V_{out} \cdot I_{out} = \eta \cdot V_{in} \cdot I_{in} \tag{2}$$

In a normal operation, the converter always keeps the V_{OUT} constant. I_{OUT} is also constant as long as the load condition is unchanged. Figure 4 shows the input port power characteristic of the DC/DC converter.

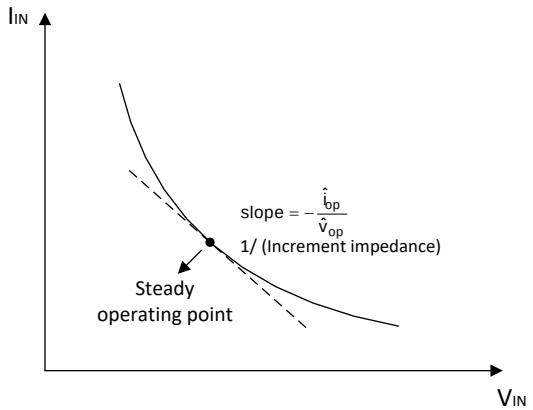

Figure 4. Input Port Power Characteristic of DC/DC Converter

When V_{IN} rises up, supposing there is not much change on efficiency, input current I_{IN} decreases. The increment input impedance of the DC/DC, is defined as:

$$Z_{inc} = \frac{\Delta V_{in}}{\Delta I_{in}} \tag{3}$$

In the equation, ΔV_{in} is positive, while ΔI_{in} is negative, so the increment input impedance is actually a negative value. Keep in mind that it is increment input impedance, which is only applicable for AC small signal analysis.

With an input filter, small input voltage change observed at the entry of the converter is decided by simple voltage dividing between output impedance of the filter and input impedance of the converter, as shown in Figure 5.

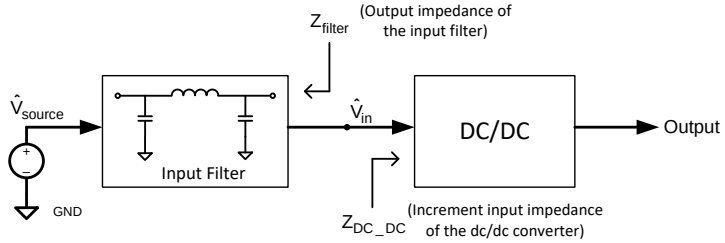

Figure 5. Small Voltage Change Dividing at Entry of DC/DC Converter with Input Filter

Suppose $\hat{V}_{source}$ and $\hat{V}_{in}$ are the small signal of power supply voltage and input voltage observed by the DC/DC converter, respectively. Taking the positive and negative sign into consideration, you have:

$$\hat{V}_{in} = \hat{V}_{source} \cdot \frac{-|Z_{in}|}{Z_{filter} - |Z_{in}|} \tag{4}$$

This means, if there is a positive disturbance on V_{source}, the input voltage change observed by the C/DC converter $\hat{V}_{in}$ can be negative, as long as $|Z_{filter}| > |Z_{dc/dc}|$.

Physically, when V_{IN} ramps up, from the view of steady state, the DC/DC converter must decrease the duty cycle to maintain the voltage regulation. Equation 4 shows entry voltage of the DC/DC converter is decreasing, so the converter tends to increase the duty cycle to keep the output voltage stable. It is something like the DC/DC converter control loop is "cheated" by the division in Equation 4. The loop is too confused to decrease or increase the duty cycle. This dilemma is the root cause for the stability issue when input filter is involved in DC/DC converter circuitry.

2.2 PCM Control Loop Modeling

To analyze how the input filter affects the control loop theoretically, obtain the loop model first. Figure 6 shows the typical block diagram of the PCM control loop. Usually, the control loop model of DC/DC converter can be split into two parts. One is power stage and the other is feedback stage. By multiplying them together, the open loop transfer function can be obtained.

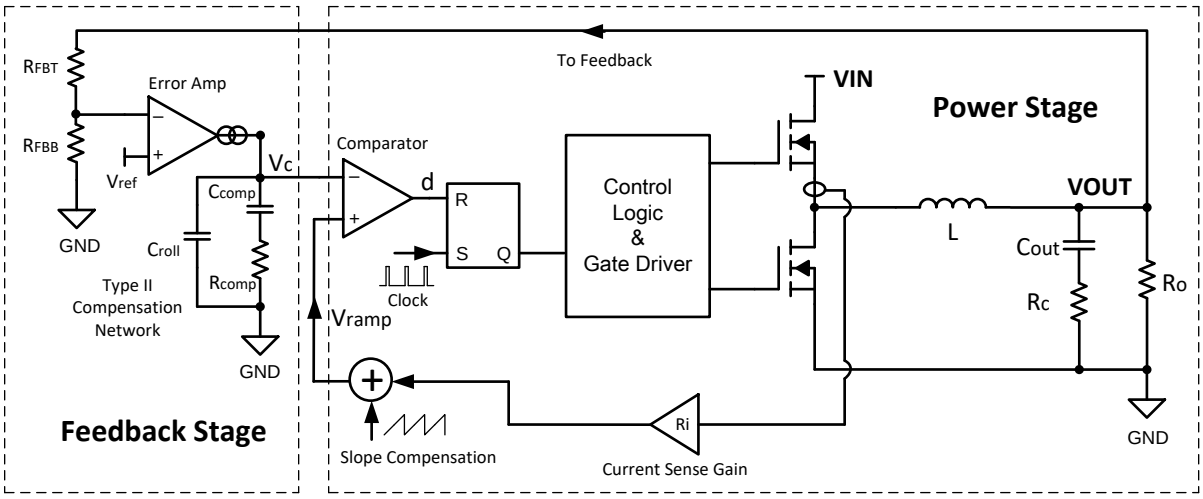

Figure 6. Typical Block Diagram of PCM Control Loop

In the power stage, the LMR14050 employs peak current mode control. The control to output ($\hat{V}_c$ to $\hat{V}_{out}$) transfers function for peak current mode control is:

$$G_{dv}(s) = \frac{\hat{v}_o}{\hat{v}_c} = \frac{R_o}{R_i \cdot (1 + \frac{R_o}{K_m \cdot R_i})} \cdot \frac{(1+\omega_z)}{(1+\omega_p)\cdot(1+\omega_L)}$$

where

- R_o is the loading resistance
- R_i is the current sensing gain in the current loop
- K_m is the modulator voltage gain (5)

This is given by:

$$K_m = \frac{V_{IN}}{(S_e + S_n)\cdot T_s}$$

where

- S_e is the slew rate for slope compensation which is design fixed inside the IC
- S_n is the slew rate of current sense signal, which is given by $S_n = R_i \cdot \frac{V_{IN} - V_O}{L}$ (6)

ω_z is the zero formed by output capacitor ESR and output capacitance, ω_p is the dominant pole formed by loading resistance and capacitance, ω_L is the inductor pole at the frequency where the inductor impedance equals the current loop gain. These zero and poles are given by:

$$\omega_z = \frac{1}{ESR \cdot C_{out}}$$

$$\omega_p = \frac{1}{R_o \cdot C_{out}}$$

$$\omega_L = \frac{K_m \cdot R_i}{L} \quad (7)$$

In the feedback path, the LMR14050 employs a type II compensation network with a trans-conductance error amplifier. The transfer function from $\hat{V}_{out}$ to $\hat{V}_c$ is:

$$G_{vd}(s) = \frac{\hat{v}_c}{\hat{v}_o} = A_{DC} \cdot \frac{1 + \frac{s}{\omega_{z1}}}{(1 + \frac{s}{\omega_{p1}}) \cdot (1 + \frac{s}{\omega_{p2}})}$$

where

- A_{DC} is the DC gain of the feedback network given by $A_{DC} = R_{EA} \cdot gm_{EA} \cdot \frac{V_{out}}{V_{in}}$ (8)

w_{z1} is the zero formed by R_{comp} and C_{comp}. w_{p1} is the pole formed by R_{ea} and C_{comp}, w_{p2} is the pole formed by R_{comp} and C_{roll}. The zero and poles are given by:

$$\omega_{z1} = \frac{1}{R_{comp} \cdot C_{comp}}$$

$$\omega_{p1} = \frac{1}{R_{EA} \cdot C_{comp}}$$

$$\omega_{p2} = \frac{1}{R_{comp} \cdot C_{roll}} \quad (9)$$

The open loop transfer function can be obtained by multiplying the transfer function of power stage and feedback. It can be written as:

$$G(s) = A_{DC} \cdot \frac{R_o}{R_i \cdot (1 + \frac{R_o}{K_m \cdot R_i})} \cdot \frac{(1 + \frac{s}{\omega_z})}{(1 + \frac{s}{\omega_p}) \cdot (1 + \frac{s}{\omega_L})} \cdot \frac{1 + \frac{s}{\omega_{z1}}}{(1 + \frac{s}{\omega_{p1}}) \cdot (1 + \frac{s}{\omega_{p2}})} \quad (10)$$

Table 1 lists some of the internal loop parameters of the LMR14050. For other parameters needed for modeling, refer to the schematic in Figure 1.

Table 1. LMR14050 Internal Loop Parameters

PARAMETERS	DESCRIPTION	VALUE
gm_{EA}	Trans-conductance amplifier gain	45 µA/V
R_{EA}	Trans-conductance amplifier output equivalent resistance	10.5 MΩ
C_{EA}	Trans-conductance amplifier equivalent capacitance	400 fF
R_i	Current sense gain	0.196 Ω
K_m	Modulator voltage gain (at working condition described in Section 1)	25.2

By substituting the parameters listed in Figure 1 and Table 1, the bode plot of the open loop transfer function is drawn in Figure 7 (all the bode plots in this note are done with MATLAB R2017a). Figure 8 shows the bench test result for verification.

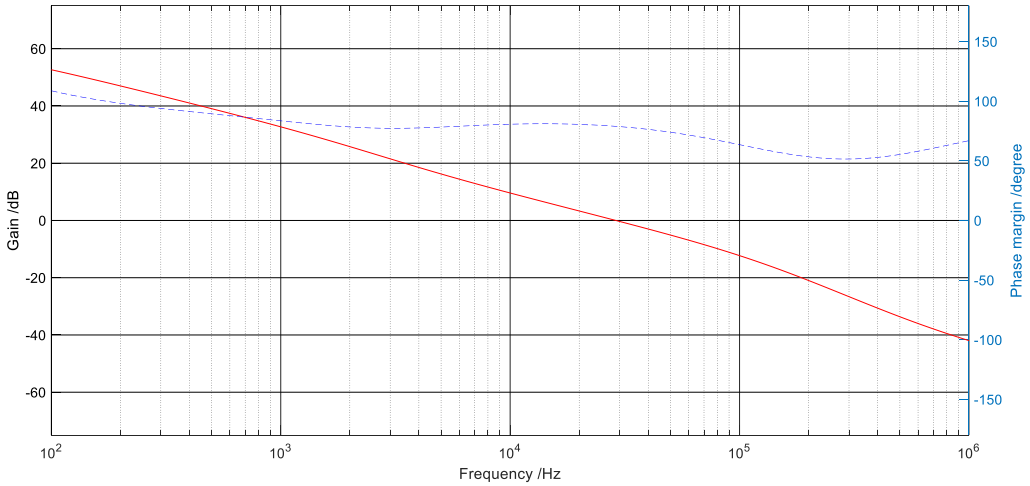

Figure 7. Bode Plot by MATLAB Modeling (VIN = 9 V, Vout = 5 V, Iout = 5 A)

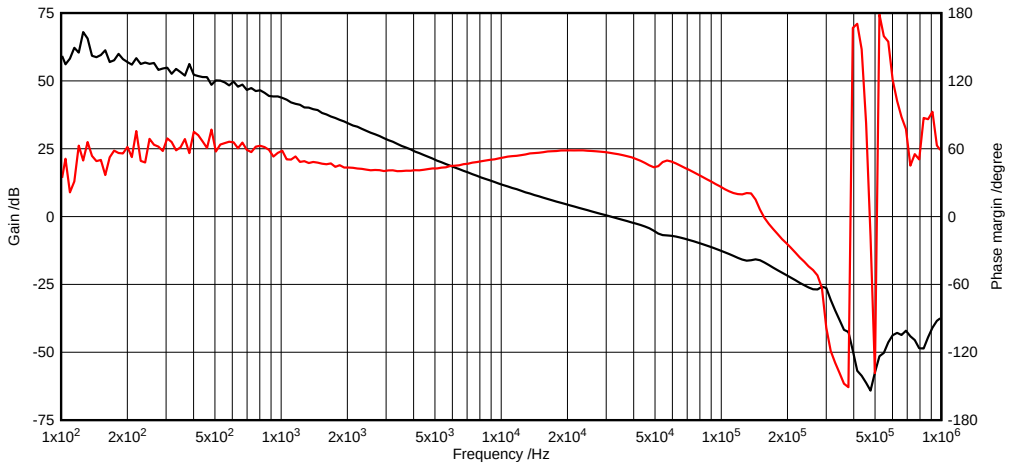

Figure 8. Bode Plot by Bench Test (VIN = 9 V, V_{out} = 5 V, I_{out} = 5 A)

2.3 Middlebrook's Extra Element Theorem

The starting point to look into the impact of applying the EMI filter is Middlebrook's extra element theorem. Figure 9 shows a simple π-type input filter.

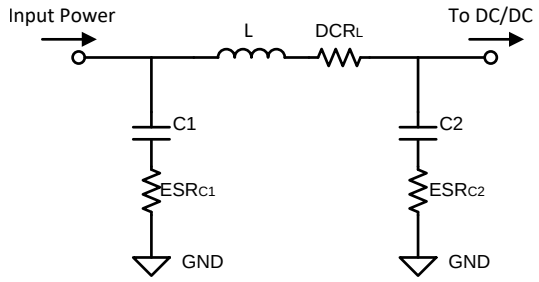

Figure 9. Simple π-type Input Filter

The input filter can be regard as an extra element of the converter circuit. According to the theorem, the extra element changes the circuit loop characteristic, and the impact can be described by introducing a correction factor into the original control to output transfer function of the circuit:

$$G_{vd}(s) = G_{vd}(s)\Big|_{Z_{o\_filter}(s)=0} \cdot \frac{1+\frac{Z_{o\_filter}(s)}{Z_N(s)}}{1+\frac{Z_{o\_filter}(s)}{Z_D(s)}}$$

where

- $G_{vd}(s)|_{Zo\_filter(s)=0}$ is the original control to output transfer function without input filter
- $Z_{o\_filter}(s)$ is the output impedance of the input filter and is given by

$$Z_{o\_filter}(s) = (sL_{filter} + DCR_L)//\left(\frac{1}{sC_2} + ESR_{C2}\right) \quad (11)$$

$Z_D(s)$ is the open loop input impedance of the DC/DC circuit, while $Z_N(s)$ is the closed loop input impedance. For the detail expression of $Z_D(s)$ and $Z_N(s)$, Ridley's small signal equivalent circuit model needs to be referred, as Figure 10 illustrated.

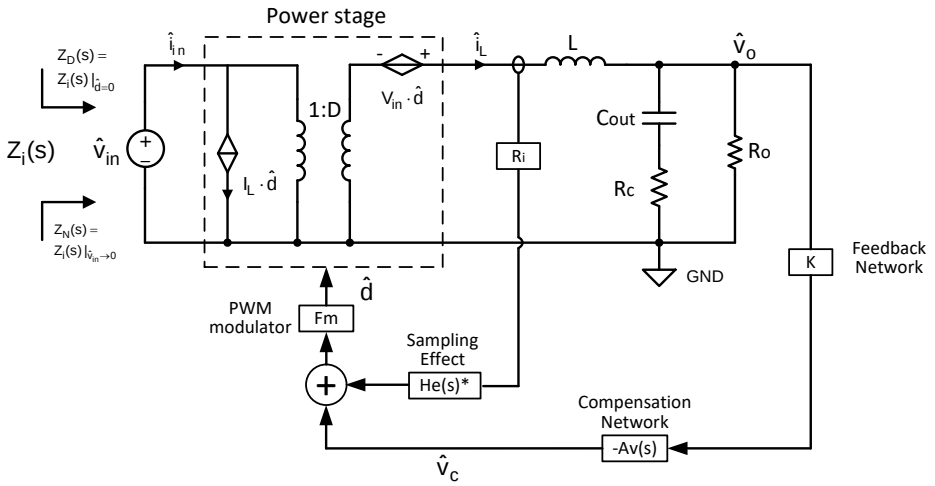

Figure 10. Small Signal Equivalent Circuit Model for PCM DC/DC Circuitry

$Z_D(s)$ represents the open loop input impedance of the dc/dc circuit, defined by:

$$Z_D(s) = Z_i(S)|_{\hat{d}=0}$$

where

- $Z_i(s)$ is the input impedance of the DC/DC circuit
- $\hat{d}$ is the small signal of duty cycle (12)

As the open loop condition, by setting $\hat{d}$=0, you have:

$$Z_D(s) = \frac{1}{D^2}\cdot[Z_L(s) + Z_o(s)]$$

where

- $Z_L(s)$ is the inductor impedance
- $Z_O(s)$ is the impedance of C_{out} and R_o (13)

They are given by:

$$Z_L(s) = ESR_L + sL$$
$$Z_o(s) = \left(ESR_{C_o} + \frac{1}{sC_o}\right) // R_o \quad (14)$$

$Z_N(s)$ is the closed loop input impedance of the dc/dc circuit, defined by:

$$Z_N(s) = Z_i(S)\,|_{\hat{v}_{in}=0}$$

where

- $\hat{v}_{in}$ is the small signal of input voltage (15)

In the simplified model (but accurate enough for the analysis here), it is given by:

$$Z_N(s) = -\frac{R_o}{D^2} \quad (16)$$

It must be noted that the accurate $Z_N(s)$ in current mode control loop is quite complicated and different from the voltage mode control loop. For readers who are interested in accurate see the *Understanding and Applying Current-mode Control Theory Application Report* for information on accurate $Z_N(s)$ expression in the PCM circuit.

In the situation where the oscillation happened, by substituting the variables with parameters in Figure 1 and Table 1, |Zd(s)| and |Zn(s)| are plotted out in Figure 11.

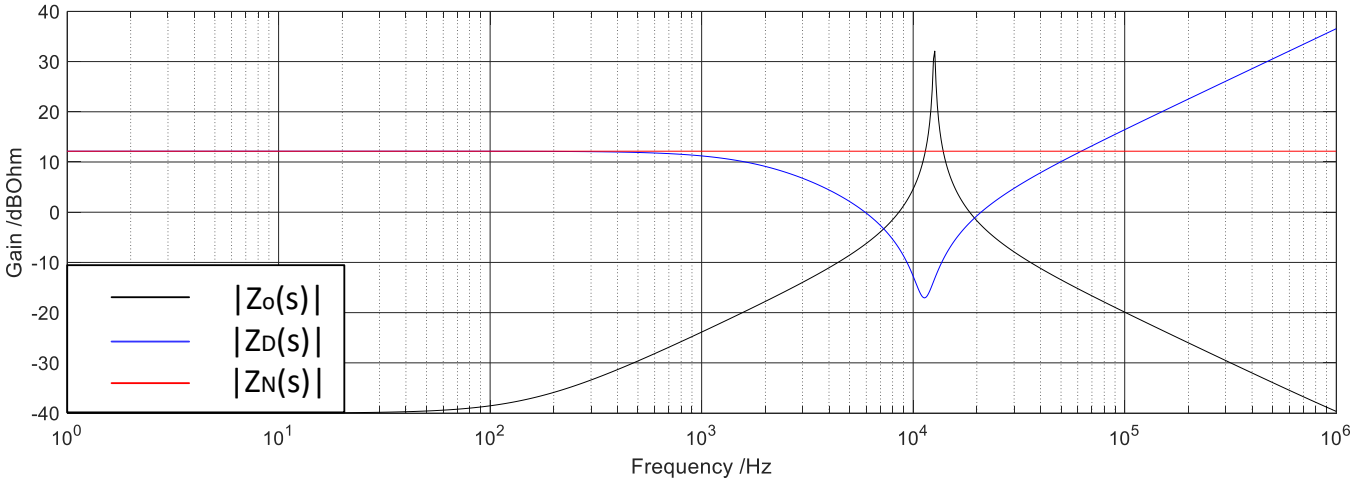

Figure 11. Plot of |Zo(s)|, |Zd(s)| and |Zn(s)|

The transfer function of correction factor can be written as:

$$Correction\_factor = \frac{1 + \frac{Z_{o\_filter}(s)}{Z_N(s)}}{1 + \frac{Z_{o\_filter}(s)}{Z_D(s)}} \quad (17)$$

Figure 12 shows the bode plot for the correction factor.

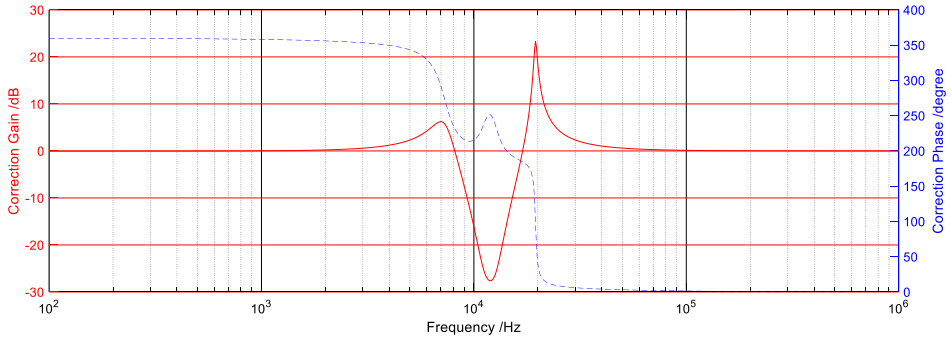

Figure 12. Bode Plot of π-type Filter Correction Factor

Fluctuation can be recognized on both gain and phase curve around the L-C resonant frequency of input filter. This is because the correction factor includes two poles and two right half plane zeros, so it shows a dip and then a quick recovery around the input filter resonant frequency on the gain curve. While on the phase curve, due to the zeros are in right half plane, it shows a 360º degree phase shift in total.

The additional poles and zeros are further introduced into the control loop of the DC/DC circuitry. According to the stability criterion for bode plot, a loop is stable only when it has a positive phase margin at the frequency where gain curve crosses the zero. The fluctuation around input filter resonant frequency may lead to violation to the stability criterion. In Section 2.4, you see how the corrector affects the DC/DC circuitry.

2.4 Open Loop Transfer Function with Input Filter

Combining the control-to output-power stage together with the feedback stage, you are able to do the bode plot for entire loop with the π-type input filter as Figure 13.

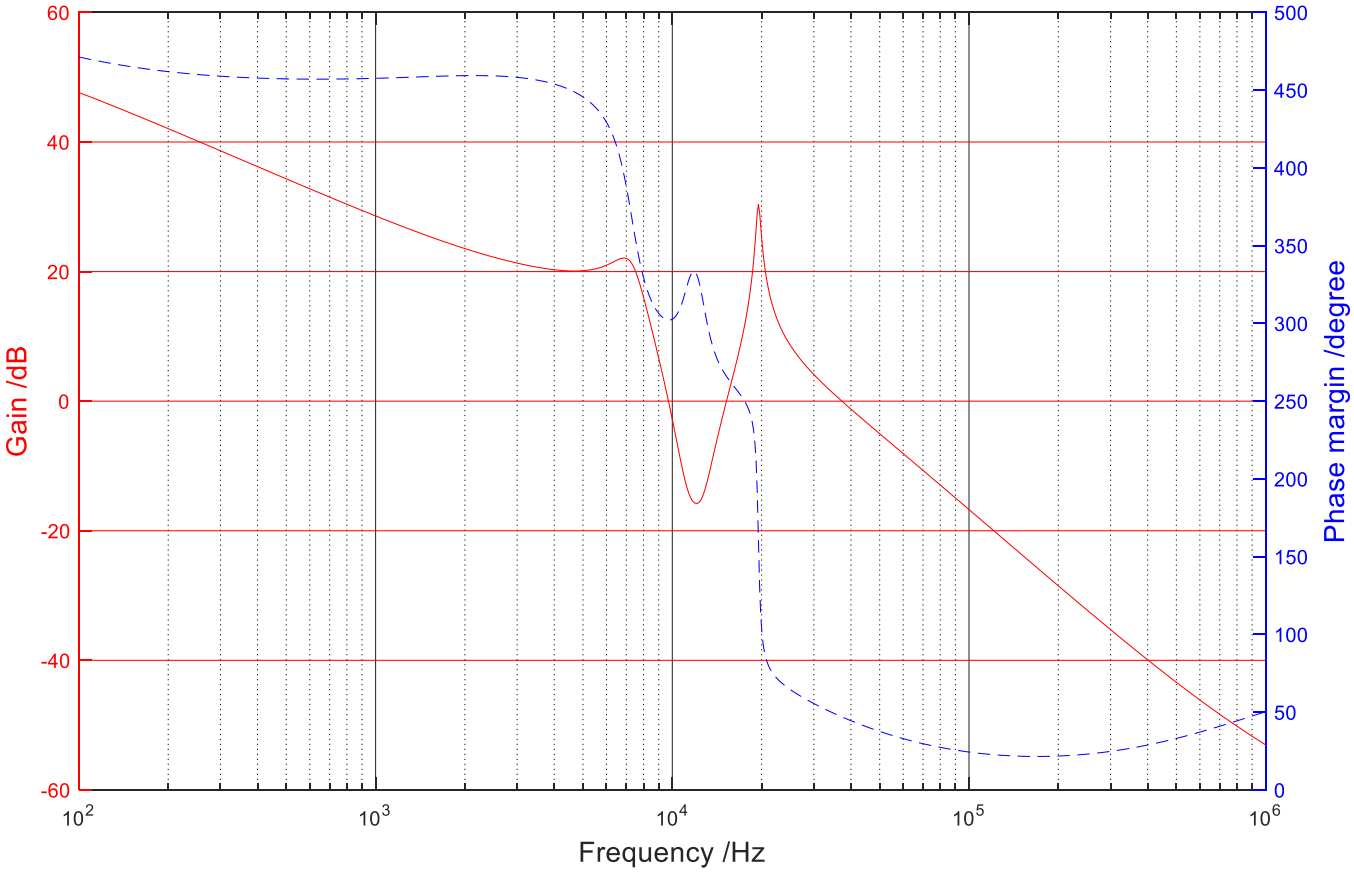

Figure 13. Bode Plot of Whole Open Loop Transfer Function with Input Filter

Compared with the bode plot with input filter shown in docato-extra-info-title (a) Bode plot by MATLAB modeling(b) Bode plot by bench test Figure 8, the additional poles and zeros introduced by the π type input filter changed the bode plot so much, that the loop no longer meets the stability criterion. The fluctuation on the gain curve changed the gain curve crossover frequency and slew rate at the crossover point. Phase shift also happened at the same frequency range, which made the situation even worse.

Judging from Equation 17, when the following inequalities are satisfied, the magnitude of correction factor is more close to unity and the phase shift is smaller, then the less effect brought by the input filter.

$$|Z_o(s)| << |Z_D(s)|$$
$$|Z_o(s)| << |Z_N(s)| \quad (18)$$

In other words, the high magnitude of $|Z_D(s)|$ and $|Z_N(s)|$ makes the loop tend to be unstable. By reviewing the expression of $Z_N(s)$ in Equation 19, $|Z_N(s)|$ tends to decrease with a higher loading current and larger duty cycle, so it is more difficult to satisfy the inequalities in Equation 18.

$$Z_N(s) = -\frac{R_o}{D^2} \quad (19)$$

That is why the instability issue is more likely to happen under heavy loading and large duty cycle condition after applying the poorly designed π-type input filter.

Actually, the issue described in Section 1 did not happen until the loading increased to 4 A. Figure 14 and Figure 15 show the bench test result at 2 A and 3 A loading. It can be seen that the loop is being closer and closer to unstable as the loading current increases.

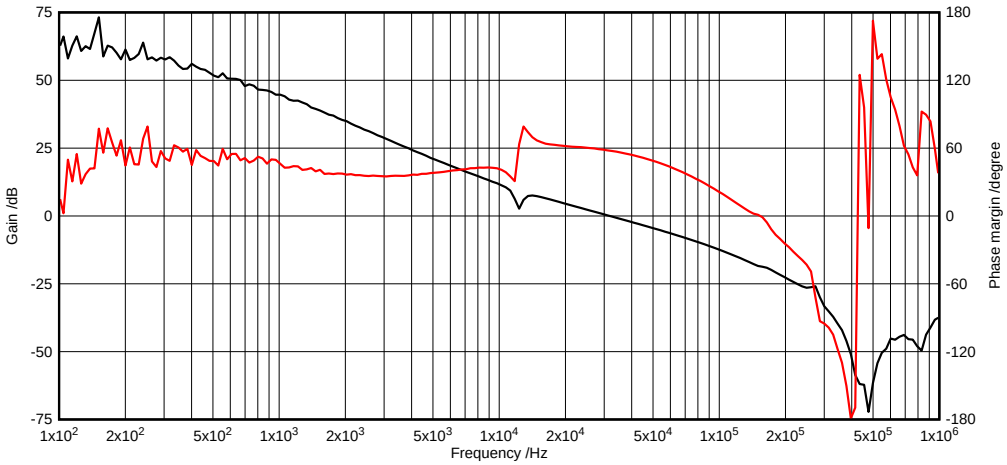

Figure 14. Bode Plot Bench Test Result VIN = 9 V, V_{out} = 5 V, I_{out} = 2 A

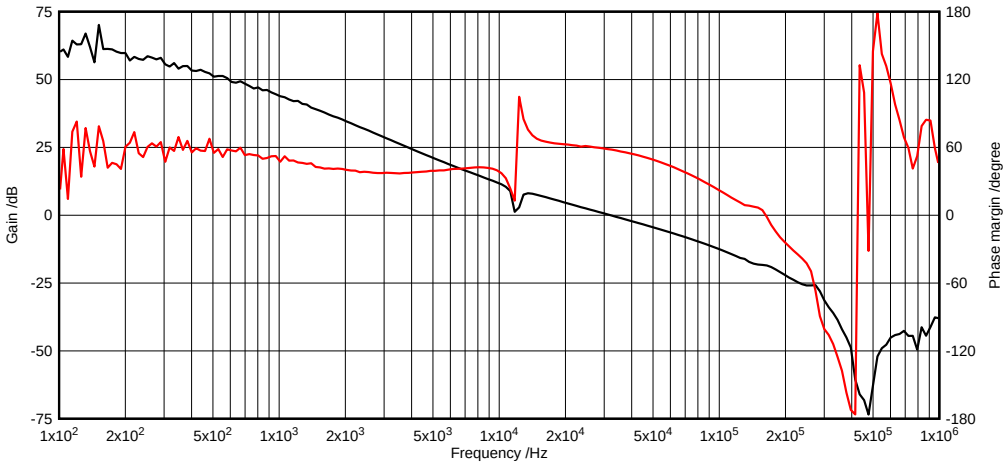

Figure 15. Bode Plot Bench Test Result at VIN = 9 V, V_{out} = 5 V, I_{out} = 3 A

3 How to Fix Input Filter Stability Issue

Based on previous discussion, it is known that there is sudden change on both the gain and phase curve around the resonant frequency of L_{filter} and C_{filter} (the capacitor close to DC/DC input). The basic principle to avoid the stability issue is to minimize the impact of correction factor introduced by the input filter. This can be done from two perspectives as shown in Figure 16.

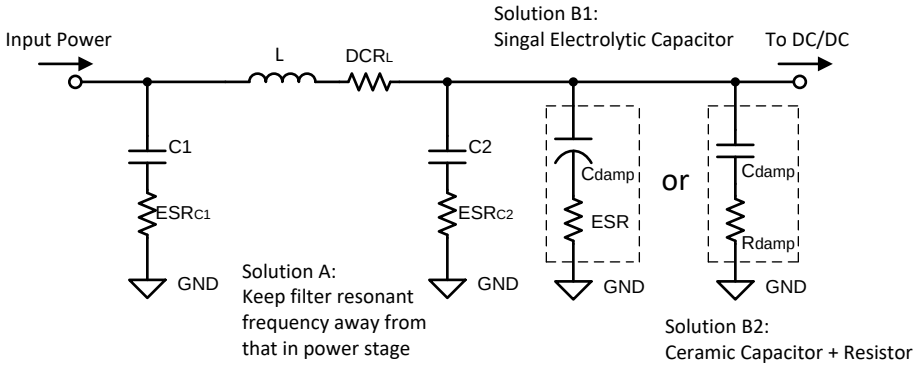

Figure 16. Damping the Filter Output Impedance

Keep the resonant frequency of the filter away from the crossover frequency of the DC/DC loop. This leaves more margin for the gain dip and phase shift around the resonant frequency of the filter, and makes sure that the fluctuating gain and phase does not violate the stability criterion.

From the perspective of Equation 18, decreasing the output impedance of the filter is another way to solve the problem. The simplest way to fix the issue is to apply a resistor in mid-frequency in parallel with the C2 in Figure 16 to damp the resonant of the input filter. This can be implemented by putting a capacitor with large ESR (such as electrolytic capacitor) in parallel with C2. The capacitance is used to block the DC power dissipation, and the ESR is used to damp filter output impedance in mid-frequency. For some solution size sensitive or height limited applications, an electrolytic capacitor might be too large to be assembled on the PCB board. A ceramic capacitor in series with a small resistor can be a good choice. By doing this, $|Z_O|$ has a smaller value in mid-frequency, making the correction factor more close to unified gain. Figure 17 shows the relationship among damped $|Z_O(s)|$, $|Z_D(s)|$ and $|Z_N(s)|$ by adding a 47µF, 100 mΩ electrolytic capacitor. Figure 18 shows the comparison of the correction factor bode plots with and without the damp.

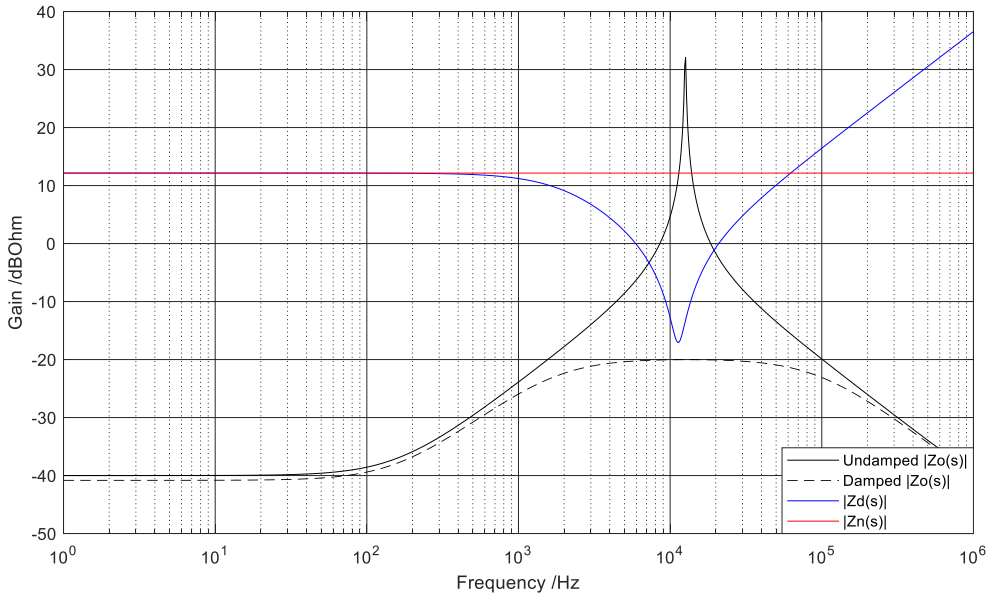

Figure 17. Bode plot for $|Z_O(s)|$, $|Z_D(s)|$ and $|Z_N(s)|$ with Damp

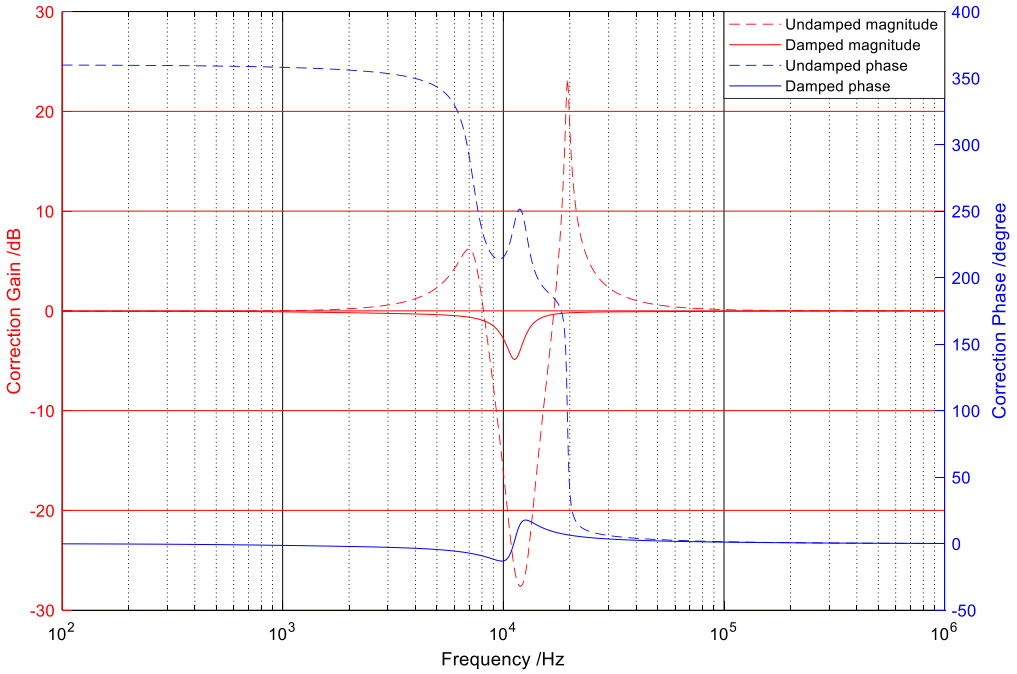

Figure 18. Bode Plot of Correction Factor w, Without Damp

Figure 19 and Figure 20 show the operating waveforms and loop characteristic by applying a 47 µF electrolytic capacitor with 100 mΩ ESR. With this solution, the DC/DC converter circuit in Figure 1 can work well with any loading condition now.

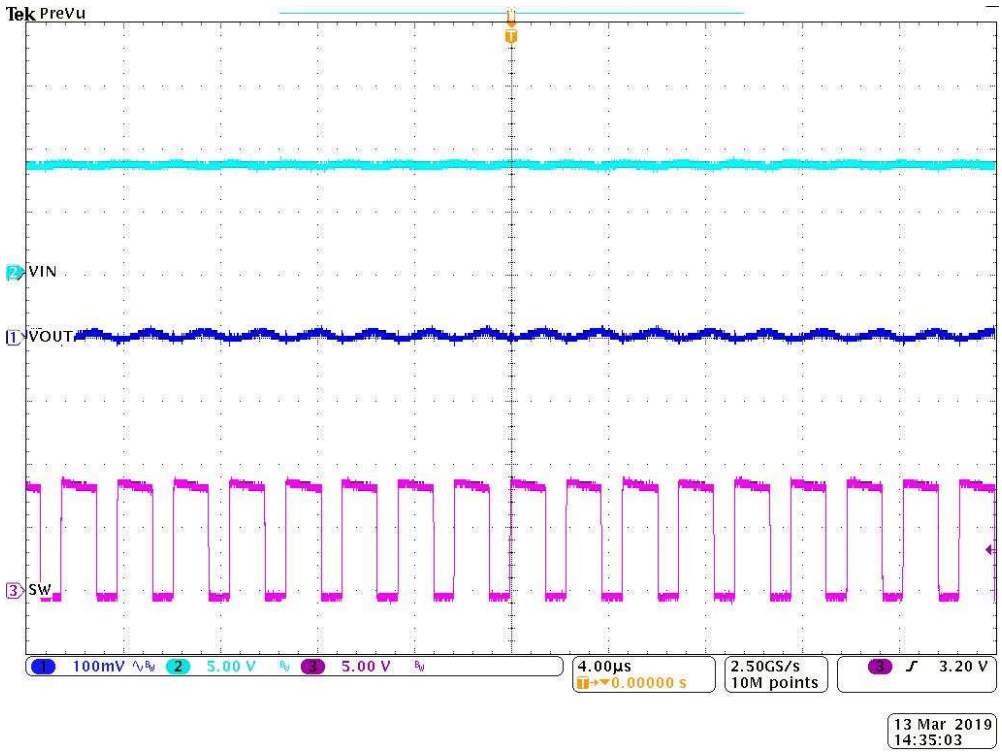

Figure 19. Operating Waveforms by Adding an Electrolytic Capacitor at VIN = 9 V, I_{out} = 5 A

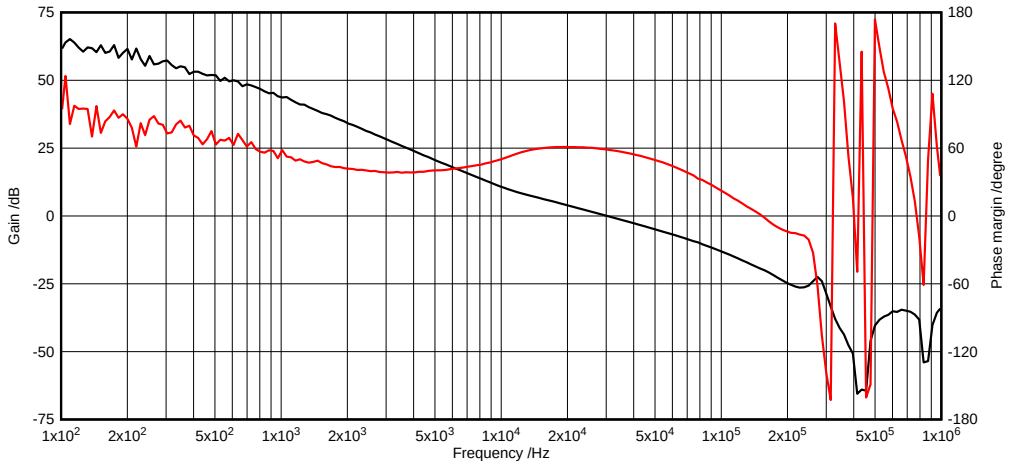

Figure 20. Loop Bode Plot by Adding an Electrolytic Capacitor at VIN = 9 V, I_{out} = 5 A

4 Summary

When designing an input filter for a DC/DC circuit, component values are sometimes selected only by the calculation to get the needed attenuation. Actually it is not enough. This application report shows an input oscillation example caused by a poorly designed input filter and provides insights to the instability and the solutions for this kind of issue.

5 References

- Texas Instruments, *40 V, 5 A SIMPLE SWITCHER, 2.2 MHz Step-Down Regulator with 40 μA IQ Data Sheet*
- Texas Instruments, *Current-Mode Modeling for Peak, Valley and Emulated Control Methods Application Report*
- *Fundamentals of Power Electronics*, Second Edition, by Robert W. Erickson and Dragan Maksimovic.
- Texas Instruments, *Analysis and Design of Input Filter for DC-DC Circuit Application Report*
- *A New Small Signal Model for Current Mode Control*, by Raymond B. Ridley

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2019) to A Revision	Page
• Updated the application report for clarity.	1

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