# *D-CAP2™ Frequency Response Model*

## *based on frequency domain analysis of Fixed On-Time with Bottom Detection having Ripple Injection*

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## ABSTRACT

Hysteretic control [2], which is basically non-linear control, has become an important control method due to its fast transient response. Normal hysteretic control requires a relatively high-ESR output capacitor. Adding ripple injection to hysteretic control allows the use of low-ESR ceramic output capacitors [3]-[6]. A “Fixed on-time with bottom detection having a ripple injection” control topology is shown in Figure 1. This topology, which is a type of hysteretic control, became popular due to pseudo fixed PWM frequency operation along with compatibility with low-ESR ceramic output capacitors. It is interesting that this control method behaves like linear control, showing similarity to a frequency response (bode-plot) of voltage mode control while keeping wide loop bandwidth, $f_{bw}$. The frequency domain analysis of the “fixed on-time with bottom detection having ripple injection” is carried out [1] for the optimal DC-DC converter design based on the assumption of (a) Averaged model is applicable to a “small-signal analysis” for frequencies less than the switching frequency and, (b) injected ripple voltage is small compared to reference voltage. As a result, the comparator with ripple injection shows single zero (1st order lead system) characteristics. The open loop transfer function of the converter is expressed as equation (1). Figure 2 shows the approximated curve of the frequency response (bode-plot) based on equation (1). The phase increases up toward +90 degrees due to the single zero, and is a major contributor for the system stability with wide loop bandwidth. This has advantages compared with conventional linear control such as voltage mode control (Figure 3) or a current mode control (Figure 4). For these linear control types, the phase curve is rolling off below 0 degrees in the high frequency range due to the delay of $e^{-sT}$ of the PWM and error amplifier compensation circuit.

The operation of D-CAP2™ control is similar in concept with this “Fixed On-Time with Bottom Detection having Ripple Injection”. The difference is that the ripple injection circuit is integrated on silicon. Therefore, it is stable.

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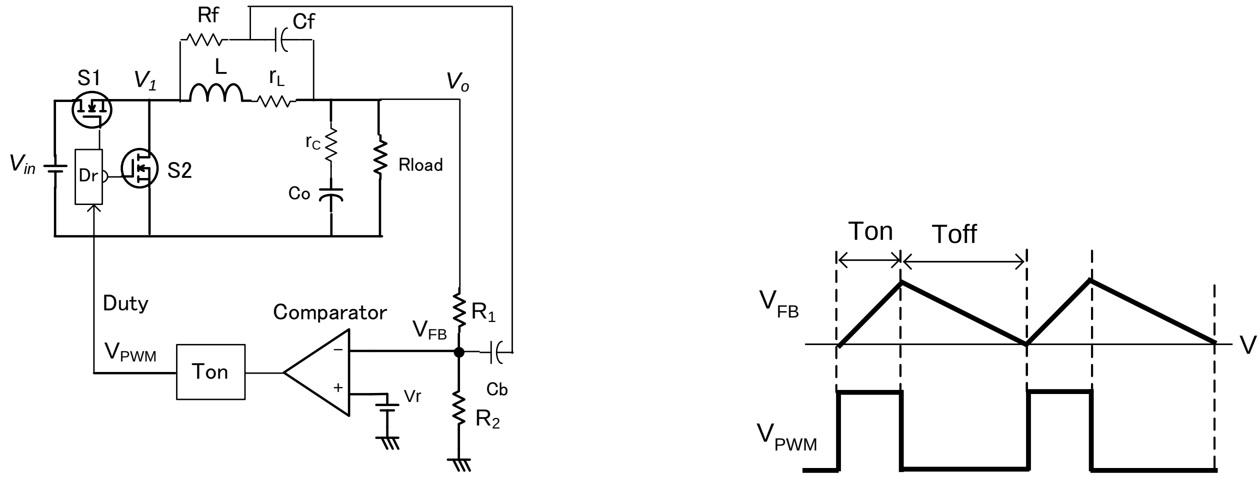

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**Figure 1. Block diagram of “Fixed On-Time with Bottom Detection having a Ripple Injection [1]**

$$G_{open}(s) = G_{dv}(s)\underbrace{\frac{A}{V_{in}}\left(1 + sT_C\right)}_{H_{comp}(s)}H_d(s) \qquad (1)$$

Where $G_{dv}(s)$ is the transfer function from Duty to $V_O$, well known using “state-space averaging model”,

$H_{comp}(s)$: Transfer function of the comparator having ripple injection circuit from $V_O$ to Duty.

$A = \frac{R_f}{R_1}$: Voltage gain of ripple injection circuit

$T_c = R_1 C_f$, Time constant of ripple injection circuit

$H_d(s) = e^{-sT_{on}/2}$: Delay factor of fixed on time

See the Appendix A to derive equation (1).

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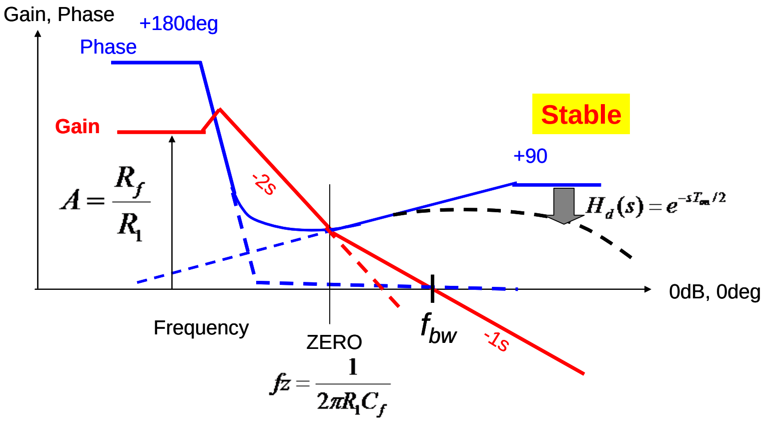


**Figure 2. Frequency response (bode-plot) of “Fixed On-Time with Bottom Detection having ripple injection” [1]**

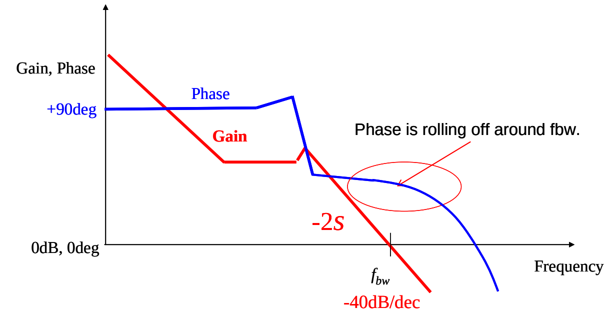


**Figure 3. Bode-plot of Voltage mode control**

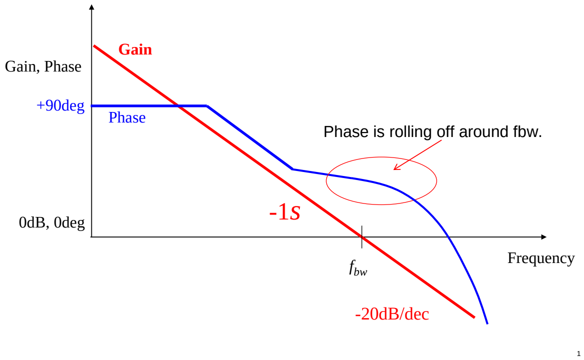


**Figure 4. Bode-plot of Current mode control**

# 1 D-CAP2$^{TM}$ open loop transfer function

## 1.1 Block diagram

Figure 5 shows the block diagram of D-CAP2$^{TM}$ include a comparator having a ripple injection circuit. An open loop transfer function should be expressed in equation (2).

$$G_{open}(s) = G_{dv}(s)H_{FB}(s)H_{COMP}(s)H_d(s) \qquad (2)$$

*Where, Gdv(s)* is the transfer function from Duty to Vo using well known “state-space averaging model”.

*$H_{FB}(s)$* is the transfer function of the feedback divider network from Vo to $V_{FB}$.

*$H_{COMP}(s)$* is the transfer function of the comparator having ripple injection circuit from $V_{FB}$ to Duty.

$H_d(s) = e^{-sT_{on}/2}$ is the delay due to fixed on time.

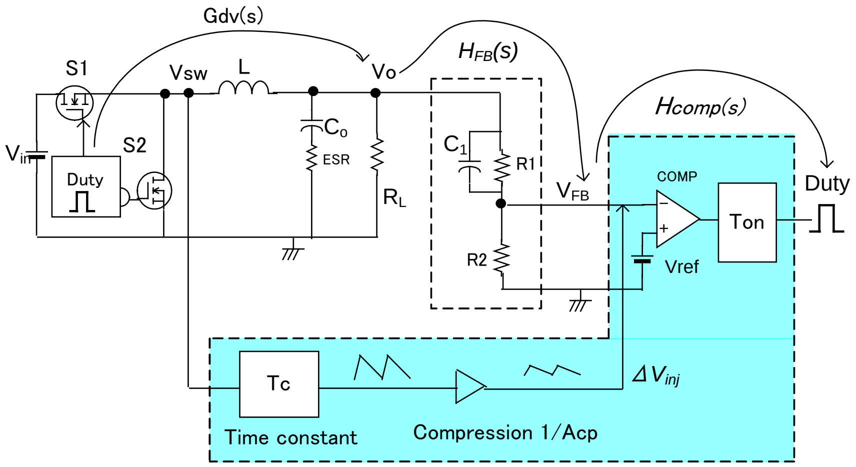


**Figure 5. Block diagram of D-CAP2**

## 1.2 $H_{comp}(s)$: The transfer function of comparator with ripple injection

Per the paper of [1], we know that the comparator with the ripple injection circuit has 1-zero (1st order lead system) which the time constant is defined by capacitor and resister network.

In Figure 5, $H_{comp}(s)$ consists of comparator and the ripple injection circuit. And the ripple injection circuit consists of the time constant block ($T_C$) and a voltage compression block ($1/A_{cp}$). So, the transfer function $H_{comp}(s)$ is expressed as follows.

$$H_{COMP}(s) = \frac{\Delta D(s)}{\Delta V_{FB}(s)} = \frac{A_{cp}}{V_{in}}\left(1 + sT_c\right) \tag{3}$$

## 1.3 $H_{FB}(s)$: Feedback divider network

The transfer function from $V_O$ to $V_{FB}$ is given as follows.

$$H_{FB}(s) = \frac{R_2}{Z_1(s) + R_2} \tag{4}$$

Where, $Z_1(s) = \dfrac{R_1}{1 + sC_1R_1}$ (5)

DC gain of $H_{FB}(s)$ is

$$H_{FB}(0) = \frac{R_2}{R_1 + R_2} = \frac{V_{ref}}{V_o} \tag{6}$$

## 1.4 Gdv(s): Plant (Power stage transfer function from Duty to $V_O$)

$G_{dv}(s)$ is given as follows using well known “state-space averaging model”.

$$G_{dv}(s)=\frac{V_{in}\left(1+\frac{s}{\omega_{esr}}\right)}{1+2\delta\frac{s}{\omega_0}+\left(\frac{s}{\omega_0}\right)^2} \tag{7}$$

Where,

$$\delta=\frac{\sqrt{L/C_O}+R_L(r_L+r_C)\sqrt{C_O/L}}{2R_L\sqrt{1+r_L/R_L}}$$

$$\omega_O=\sqrt{\frac{1+r_L/R_L}{LC_O}} \tag{8}$$

## 1.5 Delay factor of fixed on-time

The duty ratio cannot change while fixed on-time, so it should be considered as delay expressed as follows.

$$H_d(s)=e^{-sTon/2} \tag{9}$$

## 1.6 Bode-plot shape of D-CAP2$^{TM}$

Now, we derived the open loop transfer function of eq. (2) which the image of the curve is shown in Figure 6. DC gain of open loop transfer function $G_{open}(0)$ is obtained as follows.

$$G_{open}(0)=A_{cp}xH_{FB}(0)=A_{cp}\ x\ \frac{V_{ref}}{V_O} \tag{10}$$

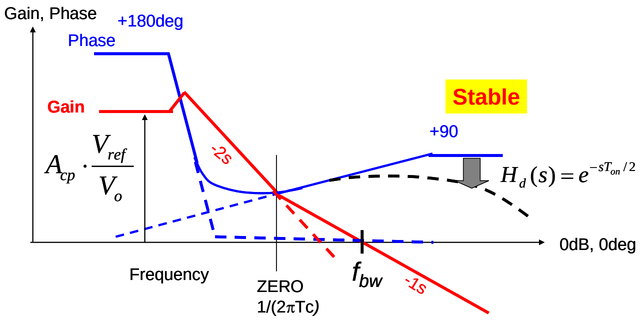


**Figure 6. Frequency response (bode-plot) of D-CAP2$^{TM}$**

## 1.7 Measurement block diagram for bode-plot

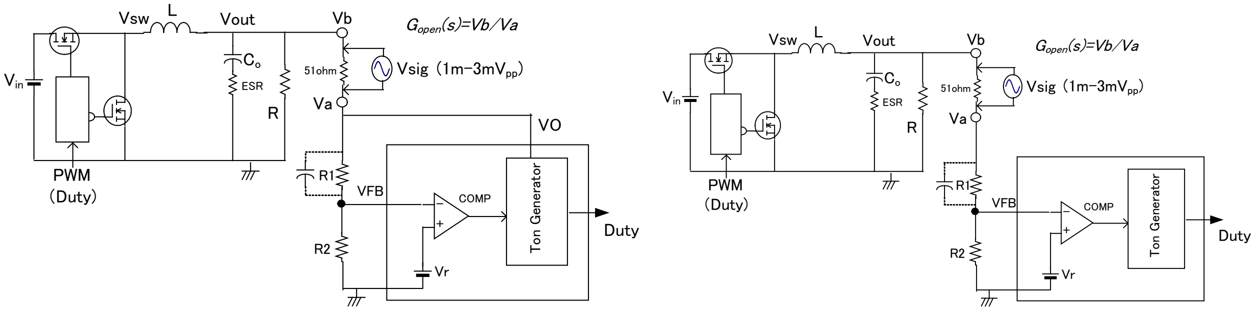
Figure 7 shows the measurement method using the popular signal injection resistor method in series with feedback network. The injection signal, Vsig, from FRA (Frequency Response Analyzer) should be small enough against the amplitude of injected ripple. Usually, Vsig is around 1mVpp to 3mVpp. Then, measure the transfer function from Va to Vb shown in Figure 9.

NOTE: If $V_O$ pin exist, the signal injection resistor (51 ohm) should be connected to R1 and $V_O$ pin as shown in Fig. 7-(a). DO NOT put 51 ohm connect with R1 only as shown in Figure 8 if $V_O$ pin exist. If $V_O$ pin does not exist, put the 51 ohm between R1 and Vo as shown in Figure 7-(b).

**Table 1. Applicable Devices as of December 2012**

| | | PKG | Mesurement set up Fig.7 | Devices ( "/" denotes devices without or with ECO mode) |
|---|---|---|---|---|
| Converter | Single | | (a) | TPS54225/226, TPS54325/326, TPS54425/426, TPS54429/429E, TPS54525/526, TPS54625/626 (1) |
| | | 8SOP | (b) | TPS54227/228, TPS54327/328, TPS54427/428, TPS54527/528, TPS54627/628 (1) , TPS54229/229E, TPS54329/329E, TPS54339/339E (1), TPS54239/239E (1), TPS56528/428 (1), TPS56228/328 (1) |
| | Dual | HTSSOP16 | (b) | TPS54294/295, TPS54394/395, TPS54494/495, TPS542941/2951 |
| Controller | Single | HTSSOP16 | (a) | TPS53114 |
| | | VSSOP10 | (b) | TPS53014/015 |
| | Dual | TSSOP24 | (a) | TPS53125, TPS53126, TPS53127, TPS53128, TPS53129 |

(1) In development



(a) $V_O$ pin exist type

(b) $V_O$ pin does not exist

**Figure 7. Measurement block diagram for bode-plot**

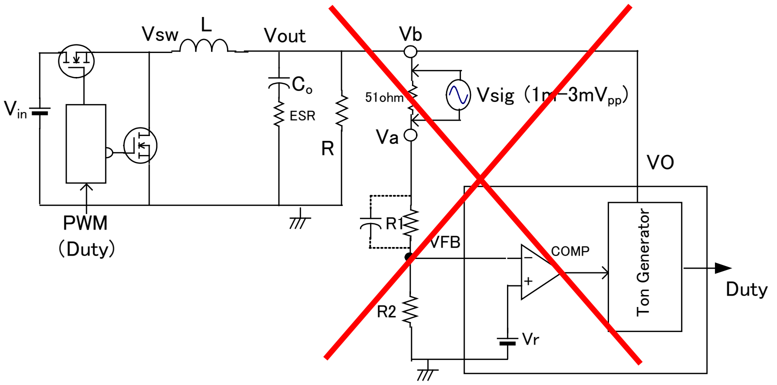


**Figure 8. Wrong measurement block diagram of bode-plot for D-CAP2 (if $V_O$ pin exist)**

## 2 Experimental data of bode-plot (Frequency response)

Here are examples of the TPS54325 (converter) and the TPS53114 (controller). Table 2 and 3 show the value of Acp and Tc of each device with the condition specified in the table.

**Table 2.**

| Device | Condition | | | Acp | Tc (us) |
|---|---|---|---|---|---|
| | Vin(V) | Vo(V) | L(uH) | | |
| TPS54325<br>(fsw=700kHz) | 12.0 | 1.05 | 1.5 | 65 | 1.06 |
| | | 1.2 | 1.5 | 70 | |
| | | 1.5 | 1.5 | 78 | |
| | | 1.8 | 2.2 | 84 | |
| | | 2.5 | 2.2 | 96 | |
| | | 3.3 | 2.2 | 104 | |
| | | 5.0 | 3.3 | 114 | |

TPS53114 (Controller):

**Table 3.**

| Device | Condition | | | Acp | Tc (us) |
|---|---|---|---|---|---|
| | Vin(V) | Vo(V) | L(uH) | | |
| TPS53114<br>(fsw=700kHz) | 12.0 | 1.05 | 1.5 | 35 | **0.95** |
| | | 1.2 | 1.5 | 36 | |
| | | 1.5 | 1.5 | 38 | |
| | | 1.8 | 2.2 | 39 | |
| | | 2.5 | 2.2 | 41 | |
| | | 3.3 | 2.2 | 42 | |
| | | 5.0 | 3.3 | 44 | |

## 2.1 TPS54325 (Converter type)

Vin = 12V, $V_O$ = 1.05V, $I_O$ = 1A: L = 1.5uH, $C_{OUT}$ = 22uFx2 (ceramic), 700kHz

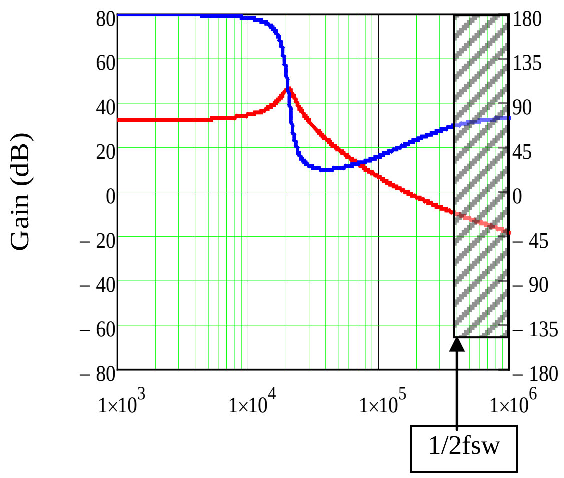


**Figure 9. Calculated**

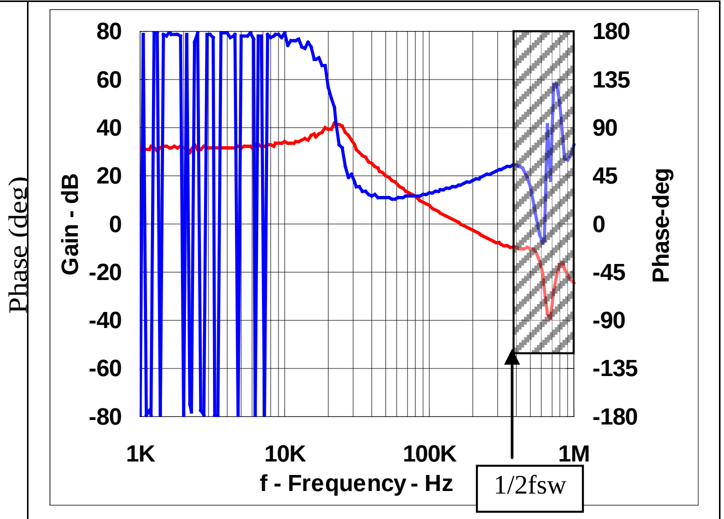


**Figure 10. Measured**

Vin = 12V, $V_O$ = 3.3V, $I_O$ = 1A: L = 2.2uH, $C_{OUT}$ = 22uFx2 (ceramic), fsw = 700kHz

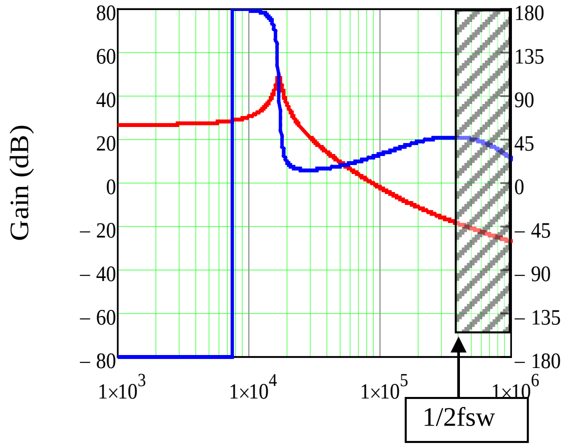


**Figure 11. Calculated**

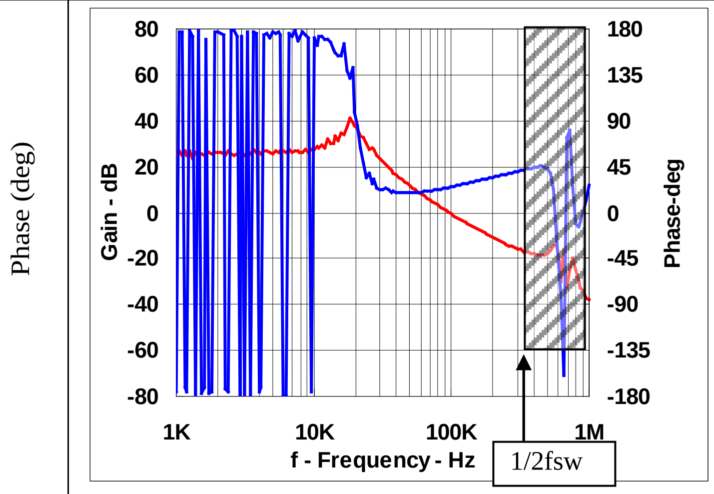


**Figure 12. Measured**

Vin = 12V, $V_O$ = 5V, $I_O$ = 1A: L = 3.3uH, $C_{OUT}$ = 22uFx2 (ceramic), fsw = 700kHz

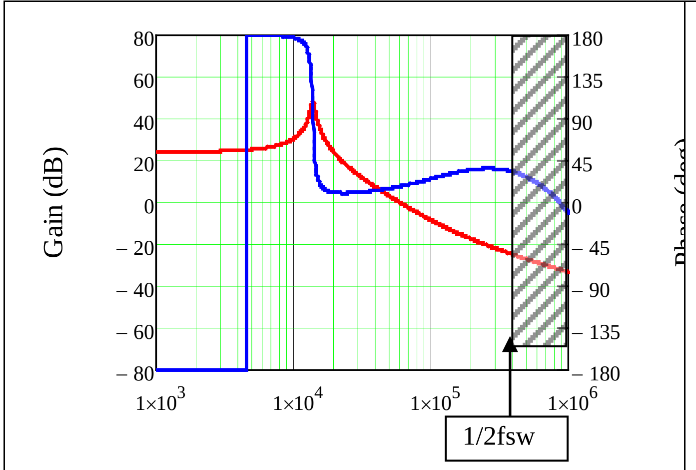


**Figure 13. Calculated**

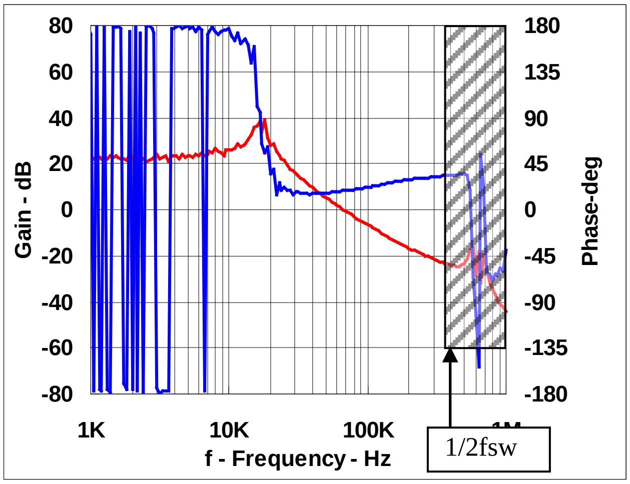


**Figure 14. Measured**

## 2.2 TPS53114 (Controller):

Vin = 12V, $\mathbf{V_O}$ **= 1.2V**, Io=2A, L = 1.5uH, $C_{OUT}$ = 22uFx2 (ceramic), fsw = 700kHz

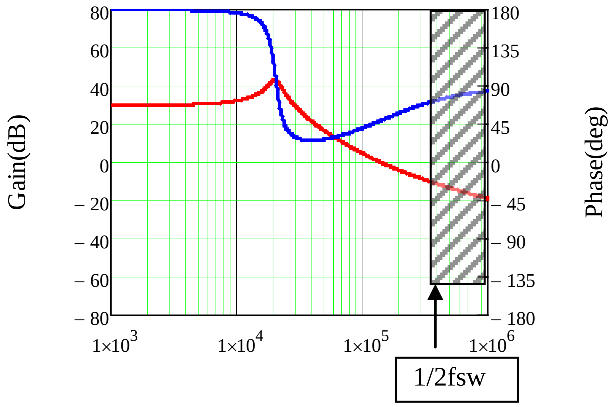


**Figure 15. Calculated**

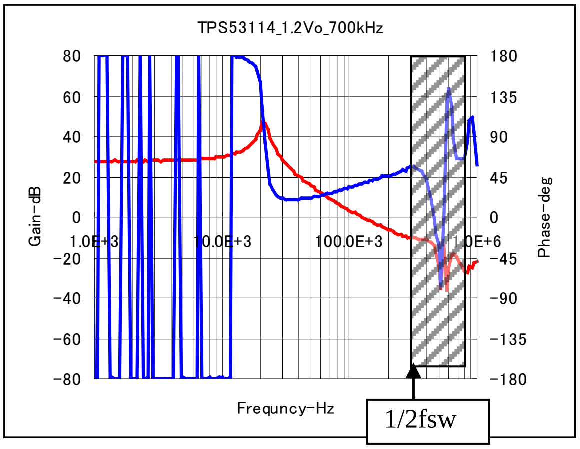


**Figure 16. Measured**

Vin = 12V, Vo=5V, Io=2A, L = 3.3uH, $C_{OUT}$ = 22uFx2 (ceramic), fsw=700kHz

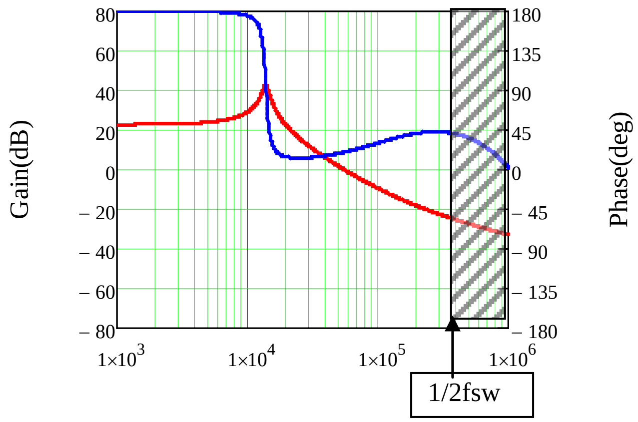


**Figure 17. Calculated**

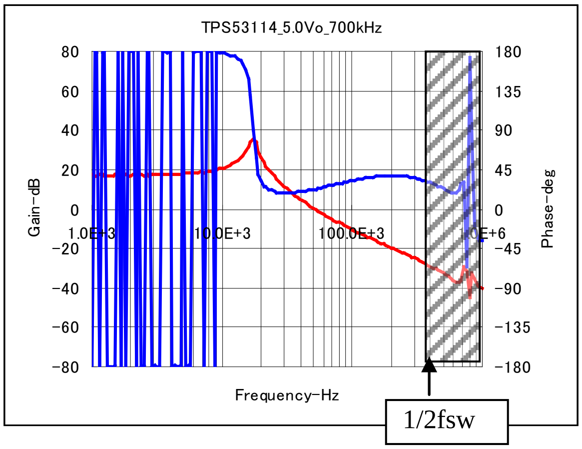


**Figure 18. Measured**

## 2.3 Phase compensation technique with Feed Forward capacitor (1pole-1zero of $H_{FB}$(s))

As shown in equation (2), there exist delay factor $e^{-sTon/2}$ due to fixed on-time. So, for a high duty ratio (such as 12 Vin, 5 Vo, or 5 Vin, 3.3 Vo), the phase curve rolling off by delay factor $e^{-sTon/2}$ becomes obvious.

In this case, feed forward capacitor (C1 in Figure 5) on $H_{FB}$(s) circuit can help to get enough phase margin by making 1pole - 1zero in equation below.

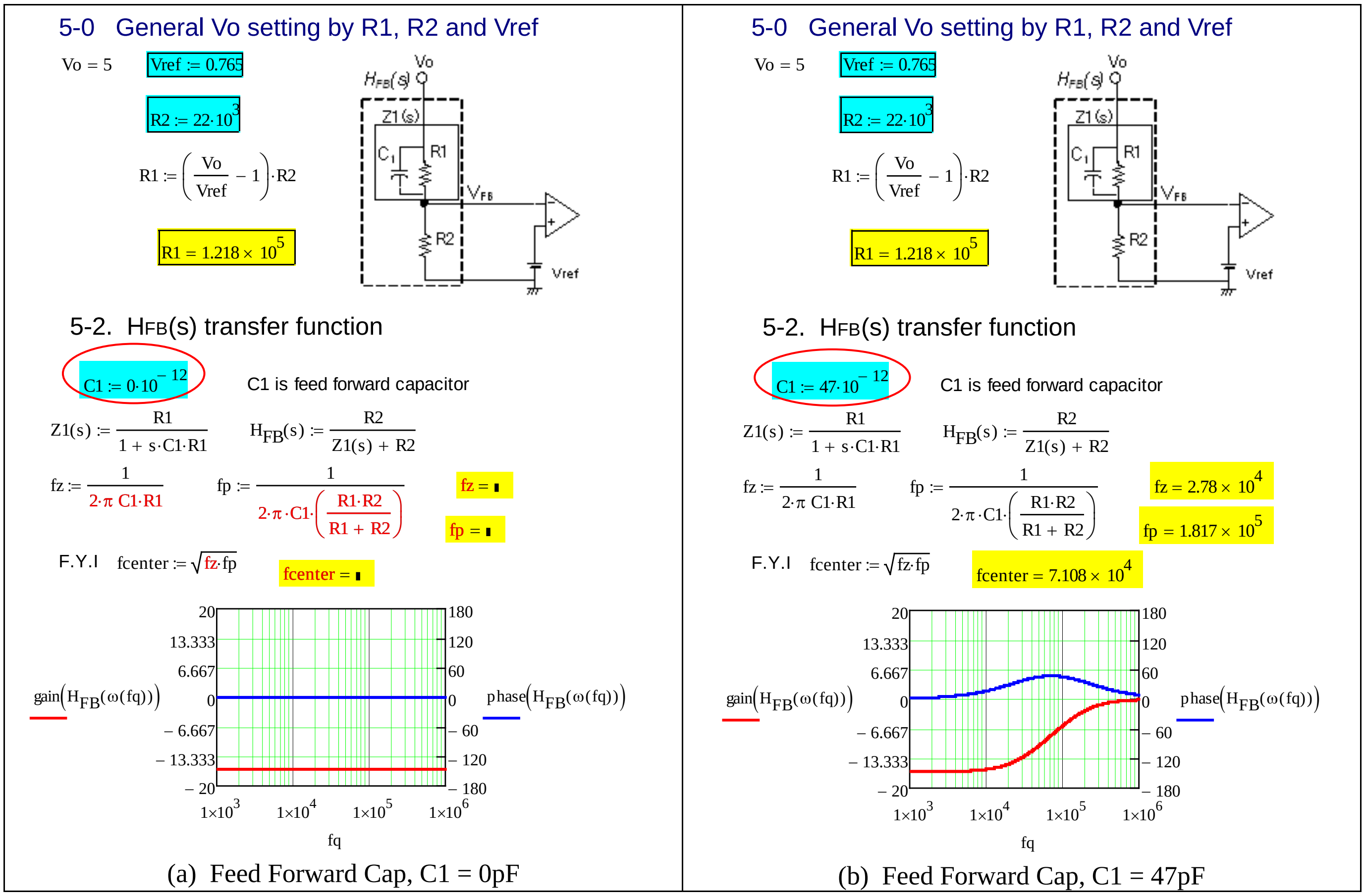
$$H_{FB}(s) = \frac{R_2}{Z_1(s)+R_2} = \frac{R_2}{R_1+R_2} \times \frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_p}} \qquad (23)$$

Where, Zero ($\omega_Z$), pole ($\omega_P$), and center frequency ($\omega_{center}$) of $H_{FB}(s)$ are expressed as follows.

$$\omega_z = \frac{1}{C_1R_1},\ \omega_p = \frac{1}{C_1(R_1//R_2)},\ \omega_{center} = \sqrt{\omega_z\omega_p} \qquad (24)$$

$f_{center}$ (=$\omega_{center}/2\pi$) is the most phase boosting frequency. Usually, when design $H_{FB}(s)$ with feed forward capacitor, place $f_{center}$ to $f_{bw}$ or fz(=$\omega_Z/2\pi$) to $f_{bw}$, or between. It depends on the case.

Figure 19 shows the example of *$H_{FB}(s)$* when Vin = 12V, and $V_{OUT}$ = 5V. Figure 19 (a) shows the case of no feed forward capacitor (C1 = 0pF). Figure 19 (b) shows the case of C1 = 47pF to make 1pole-1zero of *$H_{FB}(s)$*. Zero (*$f_Z$*) is 27.8kHz, and Pole (*$f_P$*) is 182kHz. So maximum phase boost is obtained around 71kHz (=*$f_{center}$*).



5-0 General Vo setting by R1, R2 and Vref

$Vo = 5$

$Vref := 0.765$

$R2 := 22 \cdot 10^{3}$

$R1 := \left(\frac{Vo}{Vref} - 1\right) \cdot R2$

$R1 = 1.218 \times 10^{5}$

5-2. HFB(s) transfer function

$C1 := 0 \cdot 10^{-12}$

C1 is feed forward capacitor

$Z1(s) := \frac{R1}{1 + s \cdot C1 \cdot R1}$

$H_{FB}(s) := \frac{R2}{Z1(s) + R2}$

$fz := \frac{1}{2 \cdot \pi \ C1 \cdot R1}$

$fp := \frac{1}{2 \cdot \pi \cdot C1 \cdot \left(\frac{R1 \cdot R2}{R1 + R2}\right)}$

fz = ▮

fp = ▮

F.Y.I $fcenter := \sqrt{fz \cdot fp}$

fcenter = ▮

(a) Feed Forward Cap, C1 = 0pF

5-0 General Vo setting by R1, R2 and Vref

$Vo = 5$

$Vref := 0.765$

$R2 := 22 \cdot 10^{3}$

$R1 := \left(\frac{Vo}{Vref} - 1\right) \cdot R2$

$R1 = 1.218 \times 10^{5}$

5-2. HFB(s) transfer function

$C1 := 47 \cdot 10^{-12}$

C1 is feed forward capacitor

$Z1(s) := \frac{R1}{1 + s \cdot C1 \cdot R1}$

$H_{FB}(s) := \frac{R2}{Z1(s) + R2}$

$fz := \frac{1}{2 \cdot \pi \ C1 \cdot R1}$

$fp := \frac{1}{2 \cdot \pi \cdot C1 \cdot \left(\frac{R1 \cdot R2}{R1 + R2}\right)}$

$fz = 2.78 \times 10^{4}$

$fp = 1.817 \times 10^{5}$

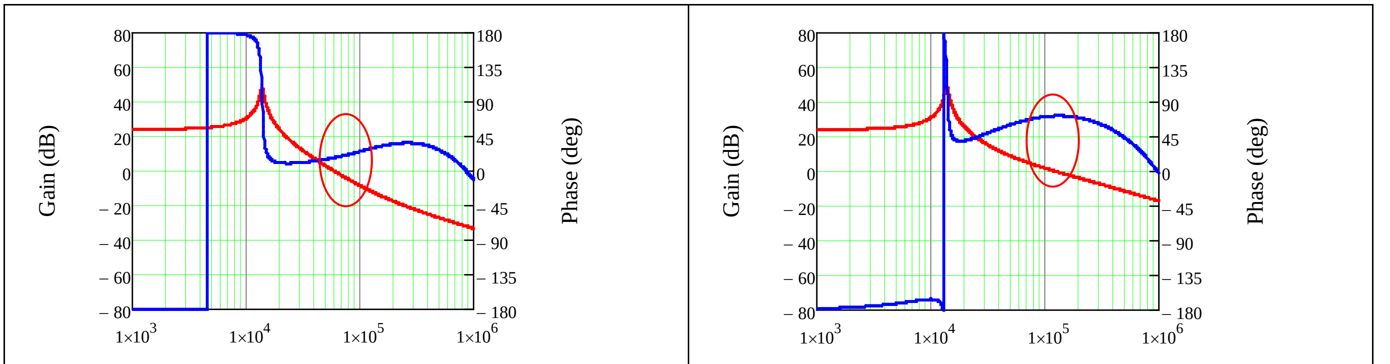
F.Y.I $fcenter := \sqrt{fz \cdot fp}$

$fcenter = 7.108 \times 10^{4}$

(b) Feed Forward Cap, C1 = 47pF

**Figure 19. Design of 1pole-1zero using feed forward capacitor (12 Vin, 5 $V_O$)**

Figure 20 shows the example of calculated bode-plot (open loop transfer function) of TPS54325 without and with feed forward capacitor, respectively. It is found that the phase margin around loop bandwidth (70kHz) was improved. Here, L=3.3uH, Co=22uFx2, fsw=700kHz.



(a) With out 1p-1z compensation (C1=0pF)

(b) With 1p-1z compensation (C1=47pF)

**Figure 20. Calculated bode-plot (open loop transfer function) of TPS54325 at 12 Vin, 5 $V_O$.**

Figure 21 shows the measured bode-plot with various feed-forward capacitor (Cf means feed-forward capacitor here) to validate the result of Figure 20. It is found that the feed forward capacitor can get enough phase margin as predicted by 1pole-1zero of HFB(s).

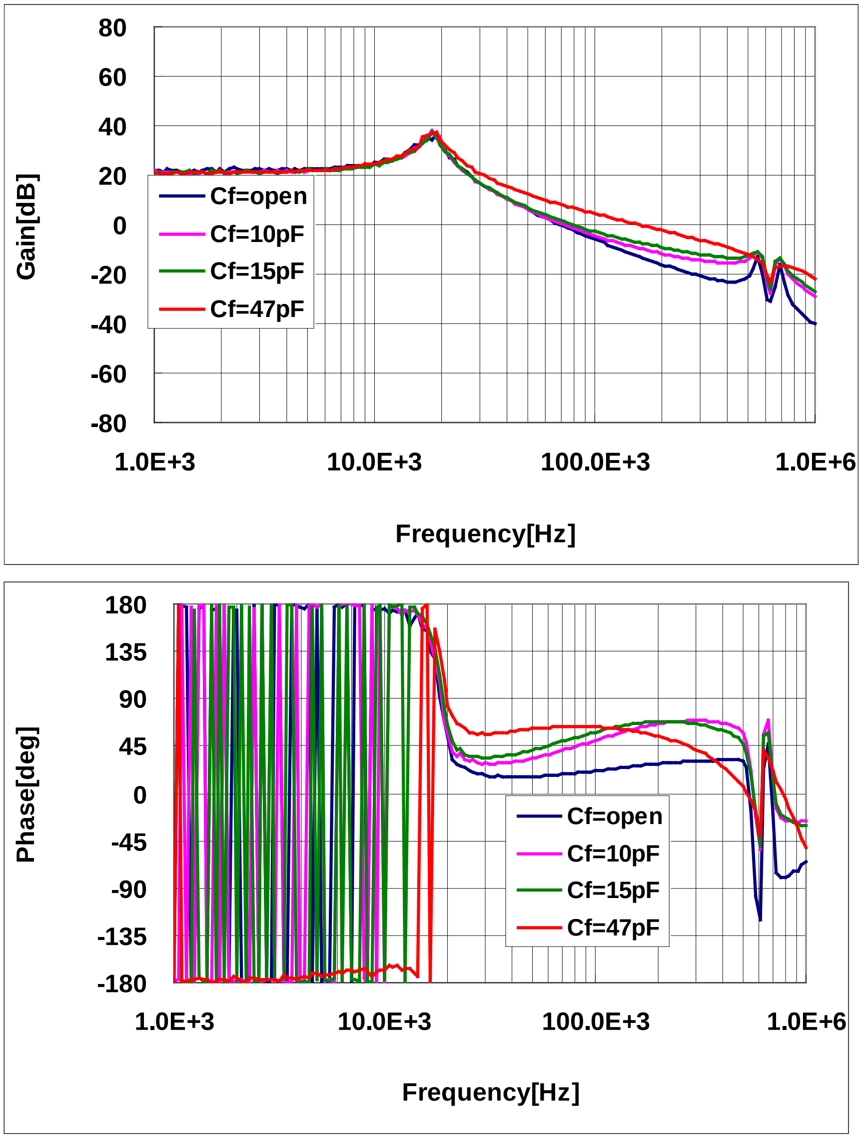


**Figure 21. Measued bode-plot (open loop transfer function) of TPS54325 at 12 Vin, 5 $V_O$.**

## References:

[1]M. Lin, T. Zaitsu, T. Sato, and T. Nabeshima,“ Frequency Domain Analysis of Fixed On-Time with Bottom Detection Control for Buck Converter,” IEEE IECON2010, pp.475-479

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# Appendix A.

## A.1 How to derive the transfer function of hysteretic comparator having ripple injection in the hysteretic control

This is the appendix for the paper [1].

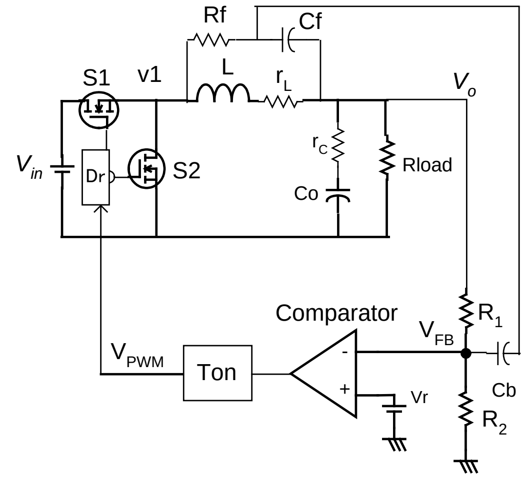

Figure A-1. Block diagram of hysteretic control (Fixed on-time with Bottom detection) having ripple injection

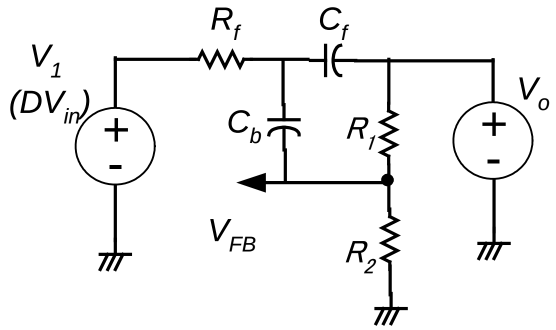

Figure A-2. Equivalent circuit of Figure A-1

There are two voltages of $V_1$ (=DVin) and $V_O$ in Figure A-2. Principle of superposition is used to get the transfer function.

## A.2 When$V_O$ = 0 ($V_O$ short)

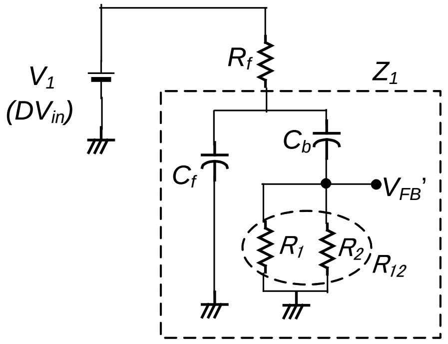

Figure A-3 Equivalent Circuit of Fig. A-2 when $V_O$ = 0

The impedance of Z1 is expressed as follows.

$$Z_1 = \frac{1}{sC_f} // \left( \frac{1}{sC_b} + R_{12} \right) = \frac{1 + sR_{12}C_b}{s(C_f + C_b) + s^2C_fC_bR_{12}} \qquad \text{(A-1)}$$

Where, $R_{12} = \dfrac{R_1R_2}{R_1 + R_2}$

Using equation (A-1), $V_{FB}'$ is expressed as follows with D x Vin.

$$V_{FB}' = DV_{in} \times \frac{Z_1}{R_f + Z_1} \times \frac{R_{12}}{\frac{1}{sC_b} + R_{12}} = \frac{sC_bR_{12}}{s^2T_cC_bR_{12} + sC_bR_{12} + sR_f(C_f + C_b) + 1} \times DV_{in} \qquad \text{(A-2)}$$

Where, $T_C = C_fR_f$

## A.3 When $V_1$ = 0 ($V_1$ short)

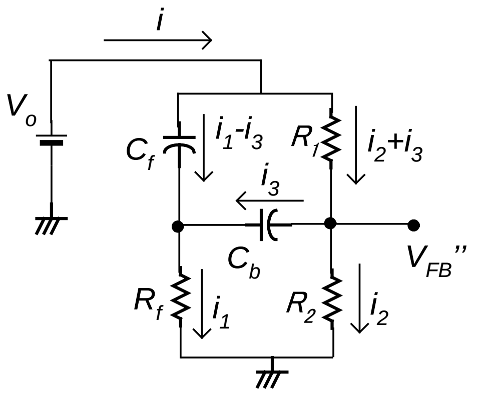

*Figure A-4 Equivalent Circuit of Fig. A-2 when $V_1$ = 0*

By Kirchhoff's laws, equations were obtained as follows.

$$V_O = \frac{1}{sC_f}(i_1 - i_3) + R_f i_1 \qquad \text{(A-3)}$$

$$V_O = R_1(i_2 + i_3) + R_2 i_2 \qquad \text{(A-4)}$$

$$R_f i_1 = R_2 i_2 - \frac{1}{sC_b} i_3 \qquad \text{(A-5)}$$

$i_3$ is obtained by eliminating $i_1$ from equations (A-3) and (A-5).

$$i_3 = \frac{1}{\dfrac{R_f}{1 + sC_fR_f} + \dfrac{1}{sC_b}} \times \left( R_2 i_2 - \frac{R_f}{R_f + \dfrac{1}{sC_f}} \times V_O \right) \tag{A-6}$$

$i_2$ is obtained by eliminating $i_3$ from equations (A-4) and (A-6).

$$i_2 = \frac{\left( \dfrac{R_f}{1 + sC_fR_f} + \dfrac{1}{sC_b} \right) \times \dfrac{1}{R_1} + \dfrac{sC_fR_f}{1 + sC_fR_f}}{R_2 + \dfrac{R_1 + R_2}{R_1} \times \left( \dfrac{R_f}{1 + sC_fR_f} + \dfrac{1}{sC_b} \right)} V_O \tag{A-7}$$

So, we can get $V_{FB}$” as follows.

$$V''_{FB} = R_2 i_2 = \frac{\left( \dfrac{R_f}{1+sC_fR_f} + \dfrac{1}{sC_b} \right) \cdot \dfrac{1}{R_1} + \dfrac{sC_fR_f}{1+sC_fR_f}}{1 + \dfrac{R_1 + R_2}{R_1R_2} \cdot \left( \dfrac{R_f}{1+sC_fR_f} + \dfrac{1}{sC_b} \right)} V_o = \frac{s^2 \cdot T_C C_b R_1 R_2 + s \cdot R_2 (T_C + R_f C_b) + R_2}{s^2 \cdot T_C C_b R_1 R_2 + s\left\{ C_b R_1 R_2 + (R_1 + R_2)(T_C + R_f C_b) \right\} + (R_1 + R_2)} \cdot V_o \tag{A-8}$$

From the principle of superposition,

$$\begin{aligned} V_{FB} &= V'_{FB} + V''_{FB} = \frac{sC_bR_{12}}{s^2 T_C C_b R_{12} + sC_b R_{12} + sR_f(C_f + C_b) + 1} \times DV_{in} \\ &+ \frac{s^2 \times T_C C_b R_1 R_2 + s \times R_2 (T_C + R_f C_b) + R_2}{s^2 \times T_C C_b R_1 R_2 + s\left\{ C_b R_1 R_2 + (R_1 + R_2)(T_C + R_f C_b) \right\} + (R_1 + R_2)} \times V_O \end{aligned} \tag{A-9}$$

Here we can assume below because the ripple voltage $\Delta V_{FB}$ is small enough compared to $V_{FB}$.

$$V_{FB} = V_r \tag{A-10}$$

Equation (A-9) is simply expressed as follows. This is a steady-state solution.

$$V_{FB} = V_r = G_1(s)DV_{in} + G_2(s)V_O \tag{A-11}$$

Where, $G_1(s) = \dfrac{sC_bR_{12}}{s^2T_CC_bR_{12} + sC_bR_{12} + sR_f(C_f + C_b) + 1}$

$$G_2(s) = \frac{s^2 \times T_CC_bR_1R_2 + s \times R_2(T_C + R_fC_b) + R_2}{s^2 \times T_CC_bR_1R_2 + s\left\{C_bR_1R_2 + \left(R_1 + R_2\right)\left(T_C + R_fC_b\right)\right\} + \left(R_1+R_2\right)}$$

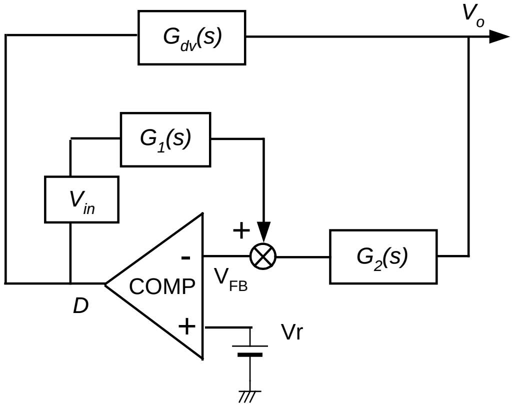

*Figure. A-5. Control Block Diagram of equation (A-11)*
*(Gdv(s) is the known plant transfer function from D to Vo)*

## A.4 Transfer function from ΔVo to ΔD (Small-signal dynamic characteristic analysis)

Through a well-known “small-signal dynamic characteristic analysis”, assuming $D \rightarrow D + \Delta D$, $V_O \rightarrow V_O + \Delta V_O$ to see the transfer function from $\Delta V_O$ to $\Delta D$. Equation (A-11) is expressed as follows.

$$V_r = G_1(s)(D + \Delta D)V_{in} + G_2(s)(V_O + \Delta V_O) \tag{A-12}$$

Substituting equation (A-11) as steady-state solution to equation (A-12), equation (A-13) was obtained.

$$\frac{\Delta D}{\Delta V_O} = -\frac{G_2(s)}{G_1(s)} \times \frac{1}{V_{in}} = -\frac{\dfrac{s^2 \times T_C C_b R_1 R_2 + s \times R_2 (T_C + R_f C_b) + R_2}{s^2 \times T_C C_b R_1 R_2 + s\left\{C_b R_1 R_2 + \left(R_1 + R_2\right)\left(T_C + R_f C_b\right)\right\} + \left(R_1 + R_2\right)}}{\dfrac{sC_b R_{12}}{s^2 T_c C_b R_{12} + sC_b R_{12} + sR_f (C_f + C_b) + 1}} \times \frac{1}{V_{in}}$$

$$= -\frac{s^2 T_C C_b R_1 + s(T_C + R_f C_b) + 1}{sR_1 C_b} \times \frac{1}{V_{in}} \tag{A-13}$$

Finally, putting $C_b = \infty$, the simplified equation of the comparator transfer function was obtained as follows.

$$\frac{\Delta D}{\Delta V_O} = -\frac{R_f}{R_1 V_{in}}\left(1 + sR_1 C_f\right) \tag{A-14}$$

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