Application Report
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A Practical Approach to Higher Output Voltage Applications for I²C Based DC/DC Converters

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ABSTRACT

DC/DC converters with I²C interfaces usually have the output voltage range from 0.6 V to 1.87 V to power up micro-processors (MCUs) requiring core voltage tune-ups. After the initial power-up, the output voltage can be programmed or scaled by VID codes sent over an I²C-compatible bus. This application report describes how to achieve a higher output voltage range with an I²C interface than the predetermined output voltage range. The I²C interface has been implemented in many TI DC/DC products such as TPS56C20, TPS56920, TPS56720, TPS56520, and this paper introduces a practical method with test results using the TPS56C20 for wide voltage range applications on the output.

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Trademarks

1 Introduction

The TPS56C20 is a synchronous step-down (Buck) converter, and the output voltage can be adjusted using the feedback resister divider network (*Adjusting the Output Voltage by External Regulation Mode*) or using a VID command from an I²C interface bus (*Programming the Output Voltage by Internal Regulation Mode*). It is a single, adaptive on-time, D-CAP2™ mode converter requiring a very low external component count. D-CAP2 control combines constant on-time control with an internal compensation circuit for a pseudo-fixed frequency of 500 kHz.

Figure 1 shows the typical application circuit of the TPS56C20 for the output voltage range from 0.6 V to 1.87 V in 10-mV steps using the I²C interface to power up micro-processors (MCUs). The device allows for a variety of applications by using the VIN and PVIN terminals together, or separately. The VIN terminal voltage supplies the internal control circuits of the device, and the PVIN terminal voltage provides the input voltage to the power converter system. The input voltage for VIN and PVIN can range from 4.5 V to 17 V.

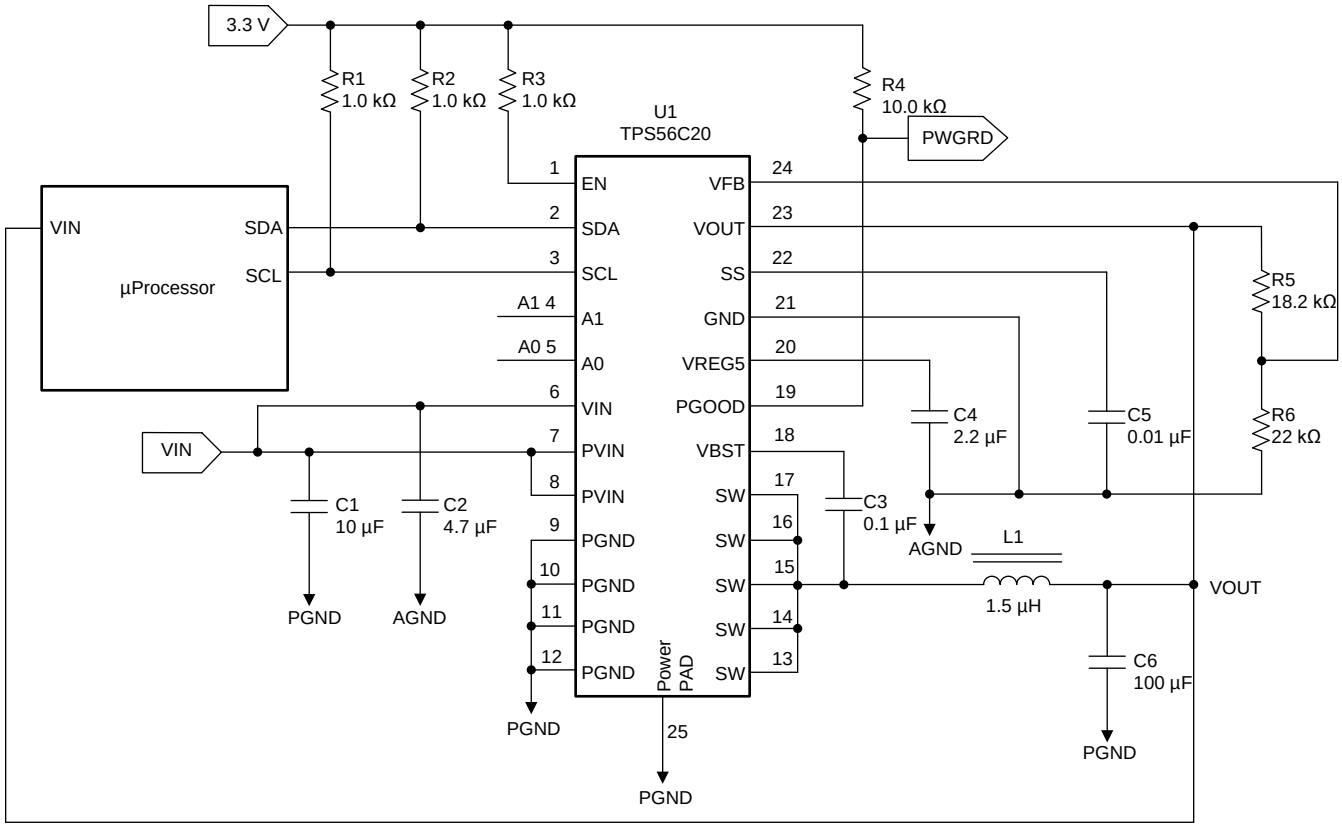

Figure 1. Typical TPS56C20 Application Circuit

Until a VOUT command has been accepted, the output voltage of the TPS56C20 will be determined by the external resistor feedback to the VFB terminals, the condition of the EN terminals, and the capacitance on the SS terminals. After recognizing its chip address, it will send an ACK and prepare to receive a data byte to be sent to that register if the TPS56C20 receives a valid register address.

2 Proposed Circuit for Higher Output Voltages with I²C

Figure 2 shows the schematic with the design parameters (V_{IN} = 12 V, V_{OUT} = 1.80 V to approximately 5.61 V, L = 1.5 µH). Note that the VFB and the EN terminals are tied to AGND for the operation of internal regulation mode only, and the actual output voltage (Vout) is determined by the external resistor feedback to the VOUT terminals.

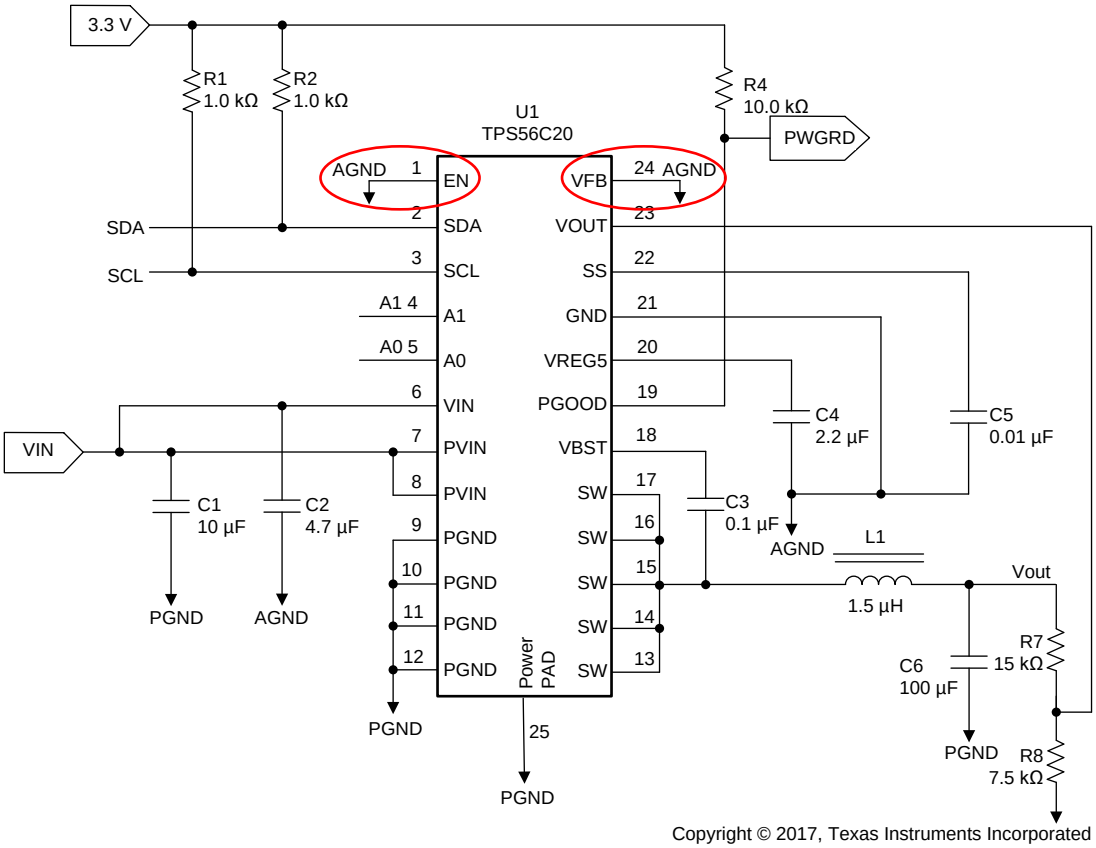

Figure 2. Proposed Circuit for Higher Output Voltage

The I²C interface terminals are composed of the SDA (Data) and SCL (Clock) terminals, and the A0 and A1 terminals to set up the address of the chip. The A0 and A1 terminals are connected to AGND for the selection of the device address (01101000, 68h).

The user can program Vout by writing any VOUT code. Since the EN terminal is low, soft start and Vout can be enabled by writing the desired VOUT code and programming the Enable bit to a one. The register map is shown in Table 1.

Table 1. I²C Register Address Byte

Register Name	Address (Decimal)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VOUT	0	Odd Parity	VOUT [:0]						
Control A	8	Internal Mode	PGOOD Delay [1:0]		Hiccup Mode On	—	ECO Mode On	DAC Settle [1:0]	
Control B	9	Enable	—	OVP Latchoff Mode Off	UVP Latchoff Mode Off	—	Current Limit [2:0]		
Status (Read Only)	24	—	TI only	TI only	TI only	TI only	OT Shutdown	Early OT Warn	PGOOD

The output voltage (Vout) is set with a resistor divider from VOUT, and it is recommended to use 1% tolerance or better divider resistors.

$$R_7 = R_8 \times \frac{Vout - VOUT}{VOUT} \quad (1)$$

Start with 7.5 kΩ for R_8 and use Equation 1 to calculate R_7 with the maximum target output voltage (Vout = 5.61 V) at VOUT = 1.81 V. To improve efficiency at light loads, consider using larger value resistors. However, if the values are too high, the converter is more susceptible to noise and voltage errors from the VOUT input current are noticeable. Also, absolute maximum voltage ratings on VFB and VOUT should be considered when the actual output voltage (Vout) is set. The maximum absolute voltage rating for VFB and VOUT is 3.6 V, and a Zener diode might be added on these pins for higher reliability. Target Vout vs VOUT[6:0] code for the Vout range from 1.80 V to 5.61 V is shown in Table 2 as an example.

Table 2. Target Vout vs VOUT[6:0] Code (Vout: 1.80 V to Approximately 5.61 V)

Code	Binary	Hex	Vout	Code	Binary	Hex	Vout	Code	Binary	Hex	Vout	Code	Binary	Hex	Vout
0	10000000	80	1.80	32	10100000	A0	2.76	64	11000000	C0	3.72	96	11100000	E0	4.68
1	10000001	81	1.83	33	10100001	A1	2.79	65	11000001	C1	3.75	97	11100001	E1	4.71
2	10000010	82	1.86	34	10100010	A2	2.82	66	11000010	C2	3.78	98	11100010	E2	4.74
3	10000011	83	1.89	35	10100011	A3	2.85	67	11000011	C3	3.81	99	11100011	E3	4.77
4	10000100	84	1.92	36	10100100	A4	2.88	68	11000100	C4	3.84	100	11100100	E4	4.80
5	10000101	85	1.95	37	10100101	A5	2.91	69	11000101	C5	3.87	101	11100101	E5	4.83
6	10000110	86	1.98	38	10100110	A6	2.94	70	11000110	C6	3.90	102	11100110	E6	4.86
7	10000111	87	2.01	39	10100111	A7	2.97	71	11000111	C7	3.93	103	11100111	E7	4.89
8	10001000	88	2.04	40	10101000	A8	3.00	72	11001000	C8	3.96	104	11101000	E8	4.92
9	10001001	89	2.07	41	10101001	A9	3.03	3.73	11001001	C9	3.99	105	11101001	E9	4.95
10	10001010	8A	2.10	42	10101010	AA	3.06	74	11001010	CA	4.02	106	11101010	EA	4.98
11	10001011	8B	2.13	43	10101011	AB	3.09	75	11001011	CB	4.05	107	11101011	EB	5.01
12	10001100	8C	2.16	44	10101100	AC	3.12	76	11001100	CC	4.08	108	11101100	EC	5.04
13	10001101	8D	2.19	45	10101101	AD	3.15	77	11001101	CD	4.11	109	11101101	ED	5.07
14	10001110	8E	2.22	46	10101110	AE	3.18	78	11001110	CE	4.14	110	11101110	EE	5.10
15	10001111	8F	2.25	47	10101111	AF	3.21	79	11001111	CF	4.17	111	11101111	EF	5.13
16	10010000	90	2.28	48	10100000	B0	3.24	80	11010000	D0	4.20	112	11110000	F0	5.16
17	10010001	91	2.31	49	10100001	B1	3.27	81	11010001	D1	4.23	113	11110001	F1	5.19
18	10010010	92	2.34	50	10100010	B2	3.30	82	11010010	D2	4.26	114	11110010	F2	5.22
19	10010011	93	2.37	51	10100011	B3	3.33	83	11010011	D3	4.29	115	11110011	F3	5.25
20	10010100	94	2.40	52	10100100	B4	3.36	84	11010100	D4	4.32	116	11110100	F4	5.28
21	10010101	95	2.43	53	10100101	B5	3.39	85	11010101	D5	4.35	117	11110101	F5	5.31
22	10010110	96	2.46	54	10100110	B6	3.42	86	11010110	D6	4.38	118	11110110	F6	5.34
23	10010111	97	2.49	55	10100111	B7	3.45	87	11010111	D7	4.41	119	11110111	F7	5.37
24	10011000	98	2.52	56	10101000	B8	3.48	88	11011000	D8	4.44	120	11111000	F8	5.40
25	10011001	99	2.55	57	10101001	B9	3.51	89	11011001	D9	4.47	121	11111001	F9	5.43
26	10011010	9A	2.58	58	10101010	BA	3.54	90	11011010	DA	4.50	122	11111010	FA	5.46
27	10011011	9B	2.61	59	10101011	BB	3.57	91	11011011	DB	4.53	123	11111011	FB	5.49
28	10011100	9C	2.64	60	10101100	BC	3.60	92	11011100	DC	4.56	124	11111100	FC	5.52
29	10011101	9D	2.67	61	10101101	BD	3.63	93	11011101	DD	4.59	125	11111101	FD	5.55
30	10011110	9E	2.70	62	10101110	BE	3.66	94	11011110	DE	4.62	126	11111110	FE	5.58
31	10011111	9F	2.73	63	10101111	BF	3.69	95	11011111	DF	4.65	127	11111111	FF	5.61

3 Experimental Results

To verify the operation and performance of the proposed application method, the output voltages are measured based on I²C signals as shown in the figures from Figure 3 to Figure 6. The results shown in Figure 3 to Figure 6 have been obtained without a feedforward capacitor (C7), and it can be seen that the TPS56C20 operates properly for higher output voltage applications.

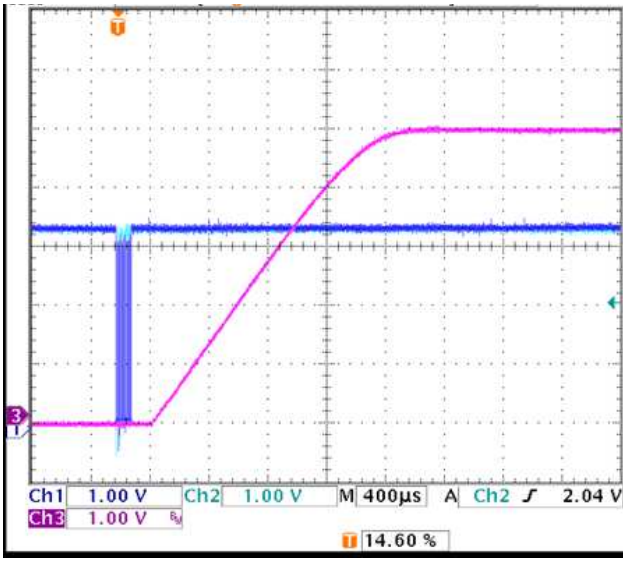

Figure 3. TPS56C20 Start Up (Vout = 5 V) With I²C

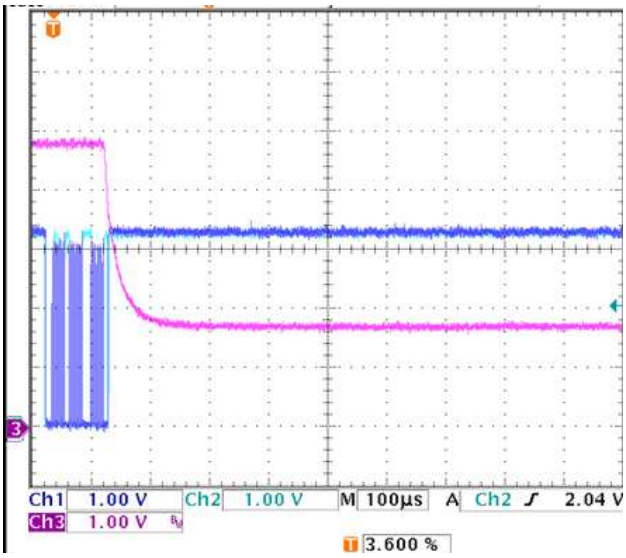

Figure 4. Output Voltage Change From 4.8 V to 1.8 V With I²C

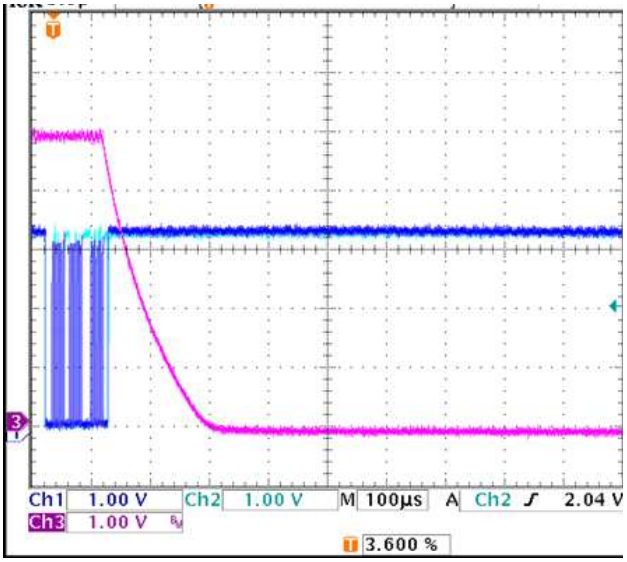

Figure 5. Shutdown With I²C

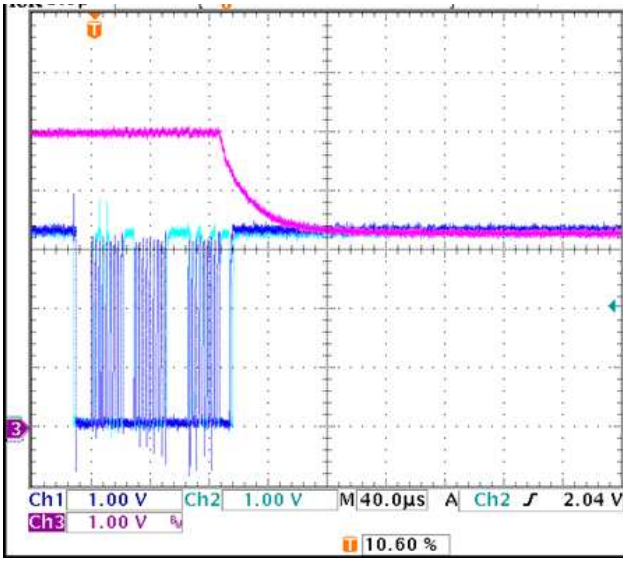

Figure 6. Output Voltage Change From 5 V to 3.3 V With I²C

For higher output voltage, a feed forward capacitor (C7) in parallel with R_7 may be required to improve phase margin with additional phase boost as shown in Figure 7.

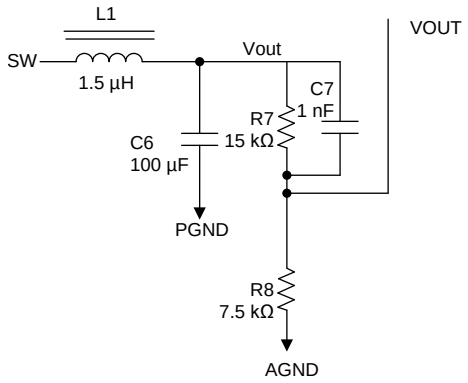

Figure 7. Feed Forward Capacitor for Higher Output Voltages

Also, in order to verify the performance of frequency stability, the AC sweep has been performed as shown in Figure 8. As for 1.87 VOUT, a feed forward capacitor is not necessary due to relatively lower output voltage, and it shows that a phase margin of 45 degrees will guarantee a stable operation without a feed forward capacitor. As for the higher output voltage (5 Vout), the phase margin (in red) without a feedforward capacitor measured to be about 30 degrees at the crossover frequency, and Figure 8 also shows the improved loop gain (in blue) with a feedforward capacitor.

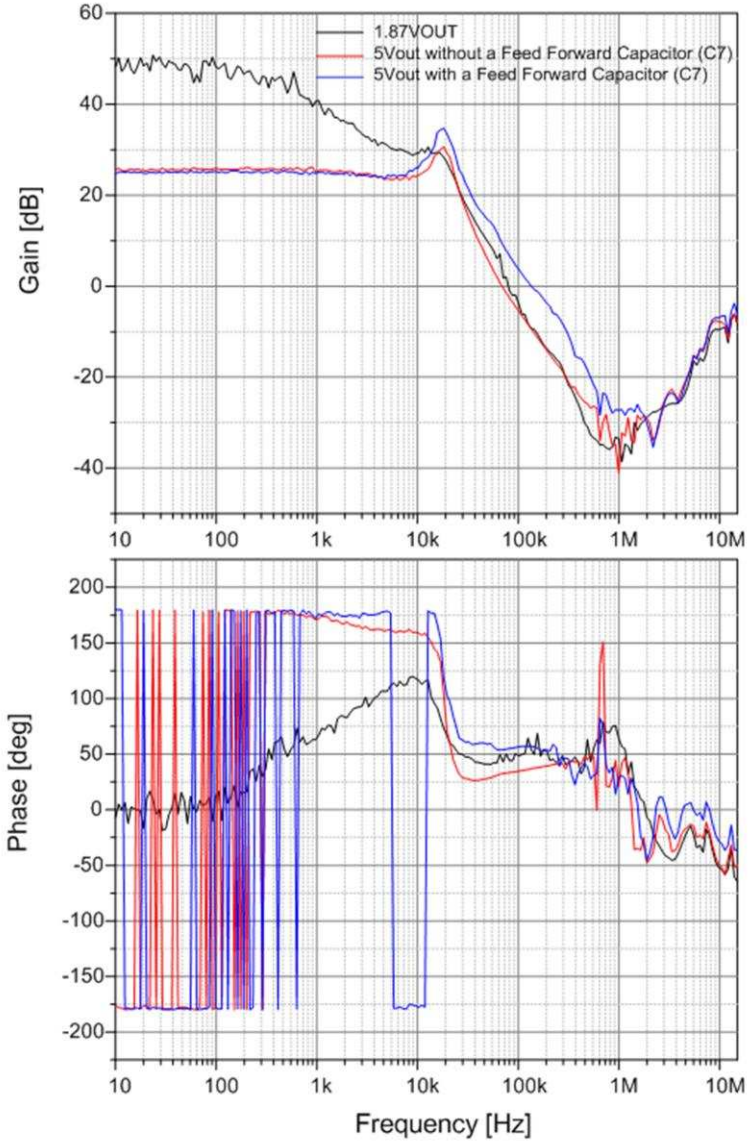

Figure 8. AC Sweep Results for Loop Gain and Phase Margin

Figure 9 shows the loop gain and the phase margin with a 1-µF feedforward capacitor for 5-V output. The converter switches at 500 kHz. The crossover frequency is limited to about 130 kHz, and the phase margin measured to be 55 degrees at this crossover frequency.

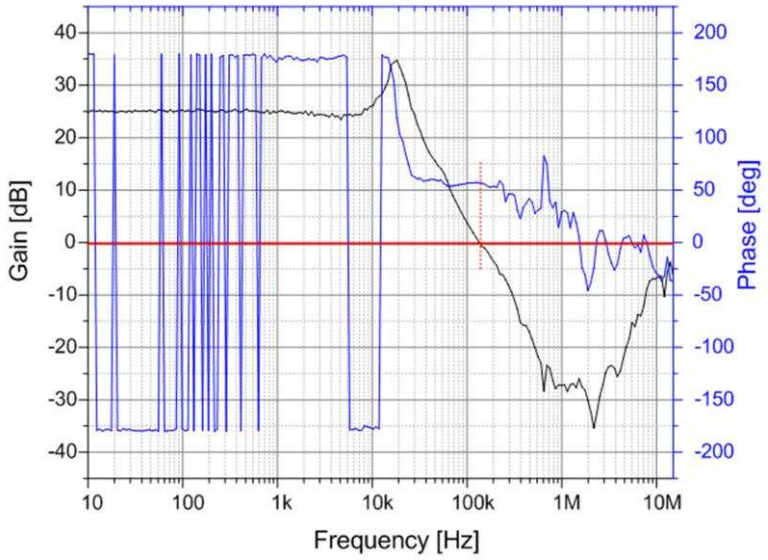

Figure 9. Loop Gain and Phase Margin for 5 Vout With a Feedforward Capacitor

4 Conclusion

A practical approach to higher output voltages with I^2C is proposed in this application report. As it has been confirmed with the actual application case (VIN = 12 V, Vout = 1.80 V to approximately 5.61 V, L = 1.5 µH), the solution operates properly, and the actual output voltage (Vout) is determined by the external resistor feedback to the VOUT terminals. The VFB and the EN terminals are tied to AGND for the operation of internal regulation mode only, and Vout can be enabled by writing the desired VOUT code and programming the Enable bit to a one. Also, the absolute maximum voltage rating on VOUT should be considered when the actual output voltage (Vout) is set, and an external Zener diode might be added to VOUT in order to increase the system reliability.

5 References

1. TPS56x20 data sheet (SLVSCB6)
2. *TPS56C20-614, 12A, SWIFT Regulator Evaluation Module* (SBAU227)
3. *Demystifying Type II and Type III Compensators Using Op-Amp and OTA for DC/DC Converters* (SLVA662)

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