Application Report
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Expand Buck Converter Minimum Input Voltage with External VCC Bias

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ABSTRACT

A typical step down (buck) converter has an internal linear low-drop-out (LDO) power supply for internal logic control and circuit drive capability. Integrating the output pin and capacitor of the LDO can help save IC pin count as well as reduce solution size; however, taking the approach of utilizing an external bias cap can provide stronger capability to drive the circuit. Additionally, using an external VCC bias allows the use of a device in lower input voltage applications while also increasing efficiency.

TPS56C215 is a monolithic 12-A synchronous buck converter with an adaptive on-time D-CAP3™ control mode. Using TPS56C215 as an example, this application note introduces a method of using an external VCC bias to support lower input voltage (VIN) applications. First, this report will describe the features of the TPS56C215 device before an example of a low input voltage application is introduced. Then, a detailed schematic with the external VCC bias configuration is presented, followed by the confirmation of this theory via bench testing and an efficiency comparison.

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1 TPS56C215 Introduction

TPS56C215 is a monolithic 12-A synchronous buck converter with an adaptive on-time D-CAP3™ control mode. The device integrates low RDS(on) power MOSFETs that enable high efficiency and offer ease-of-use with minimum external component count, handy for space-conscious power systems.

The TPS56C215 has a 4.7 V internal LDO that generates a bias for all internal circuitry. There is a feature to overdrive this internal LDO with an external voltage on the VREG5 pin which improves the converter's efficiency. Figure 1 is the Typical Application Diagram of TPS56C215.

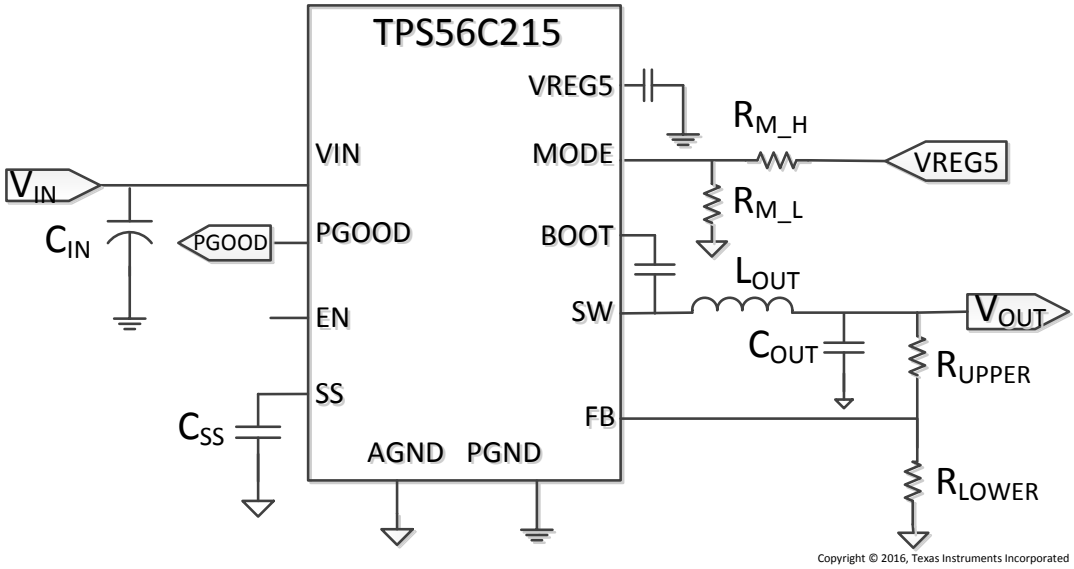

Figure 1. TPS56C215 Typical Application Diagram

2 12 V / 5 V O-ring supply for DDR application

In workstation DDR applications, customers can use 12 V to convert 2.5 V for Vpp supply. When 12 V fails, customers can have another 5 V rail as backup source to supply the Vpp rail. So customers typically want to use their ORing topology summing together 5 V and 12 V inputs to Vin through diodes. Considering the margin, usually a 4 V–13.2 V input range voltage buck converter is employed here. A simplified schematic is shown in Figure 2

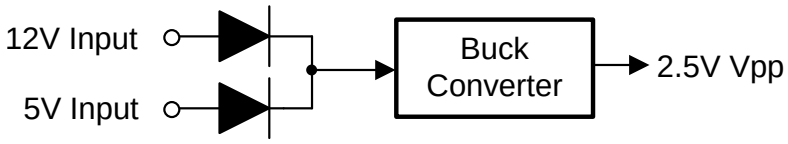

Figure 2. Simplified Schematic of DDR Vpp Supply

In the current market, devices with 17 V max-VIN ratings typically have a minimum input voltage in the range of 4.5 V. If the VIN_min goes lower, the internal logic circuit power supply would be difficult to realize or the cost of device will increase significantly, especially for a high-current device. For this DDR application, there is already 5 V rail in the system. When connecting this 5 V to VREG5 for internal circuit supply, the buck converter could support input voltages lower than 4.5 V, meaning the customer could use the current solution to realize 5 V / 12 V ORing topology. The configuration schematic based on TPS56C215 is shown in Figure 3.

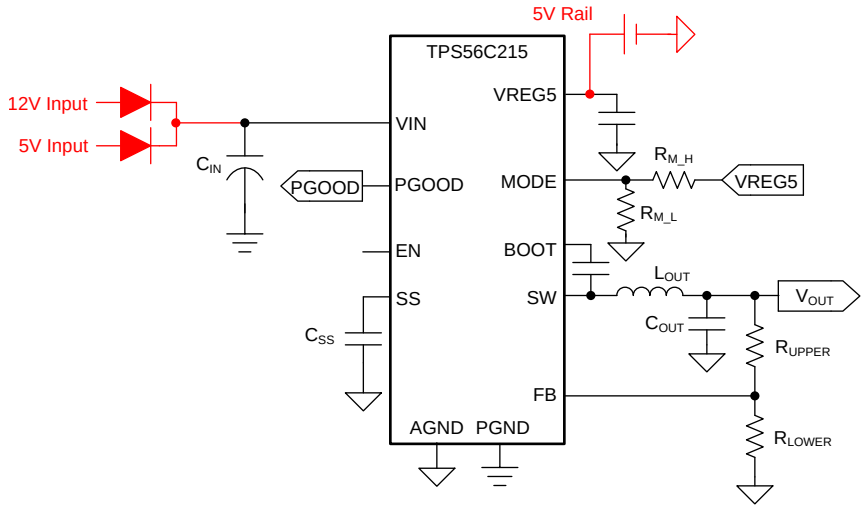

Figure 3. Configuration Schematic Based on TPS56C215

3 Schematic and Bench Results

The detail schematic of external VREG5 Biased TPS56C215 schematic is shown in Figure 4.

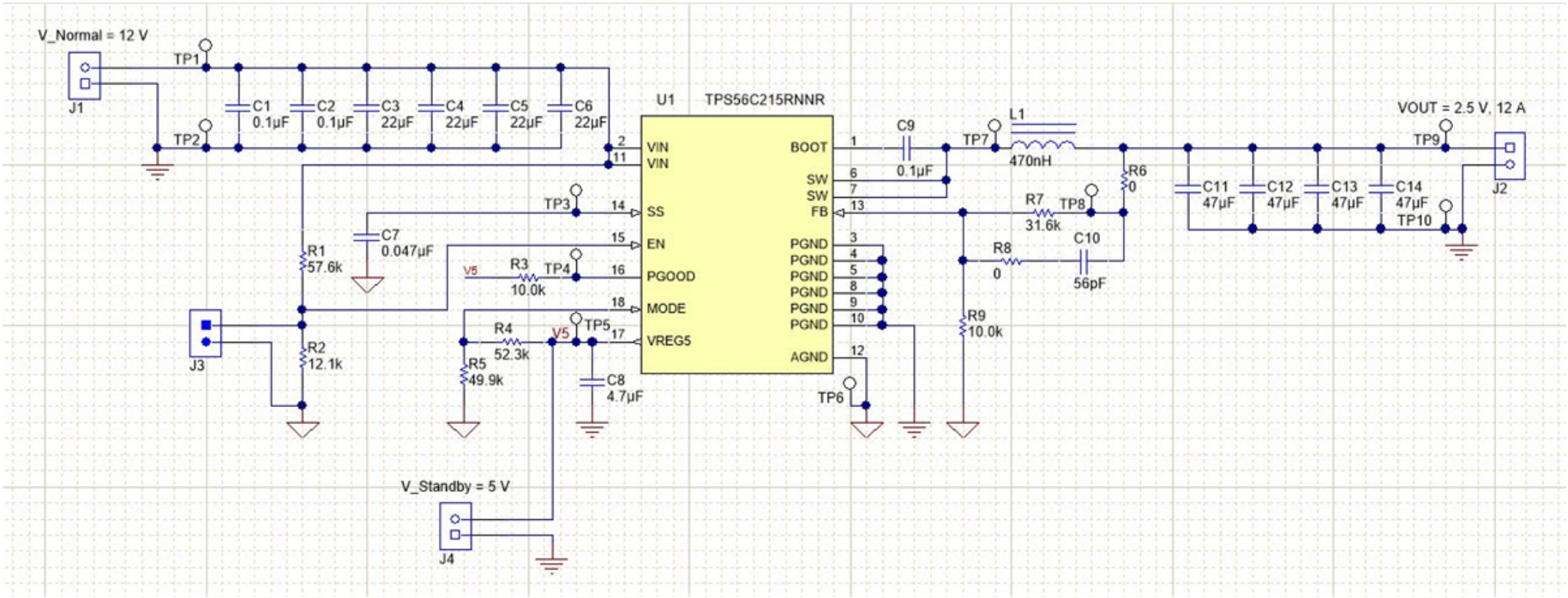

Figure 4. External VREG5 Biased TPS56C215 Schematic

The system level parameters are shown in Table 1.

Table 1. System Parameters

Parameter	Example Value
12 V Input Voltage Rail, V 12	12 VDC
5 V Input Voltage Rail, V 5	5 VDC
VREG5 Supply, V_{DD}	5 VDC
Output V_{PP} Voltage, V_{OUT}	2.5 VDC
Maximum Output Current, I_{O_MAX}	12 A
Switching Frequency, F_{SW}	800 kHz
Output Inductor, L_f	470 nH
Output Capacitor, C_{OUT}	47uFx4

3.1 Efficiency Comparison

With external VREG5 supplied, the internal LDO is disabled. The analog circuitry and driver power supply will come from the external VREG5 supply. While monitoring 12 V normal input rail efficiency, it could be observed that the external VREG5 supply efficiency is slightly higher than internal VREG5 supply. The comparison curve is shown in Figure 5.

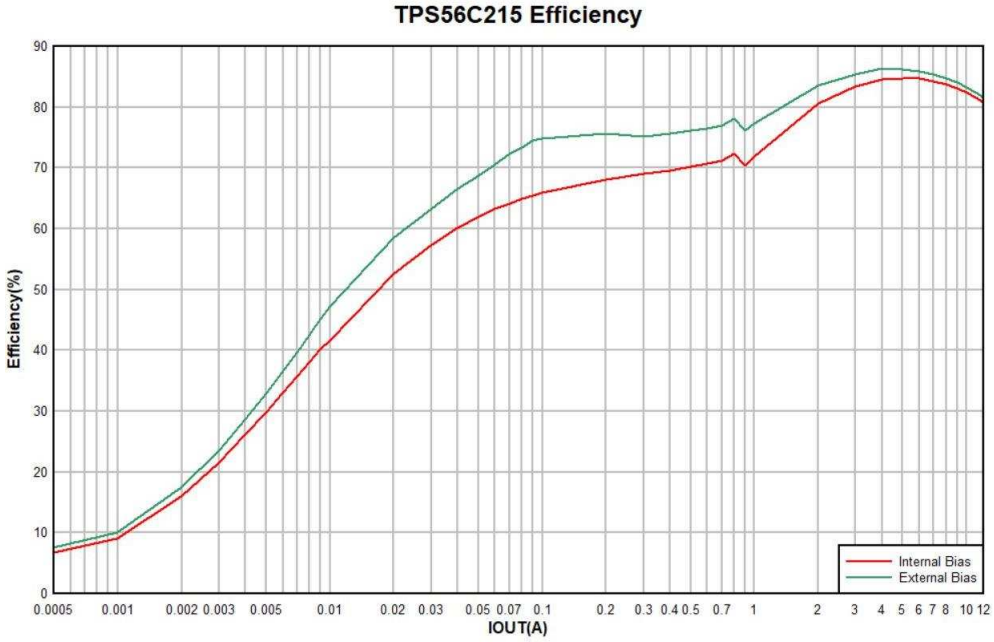

Figure 5. Efficiency Comparison Between Internal and External VREG5 Power Supply

3.2 Bench Waveforms

Figure 6 through Figure 13 show TPS56C215 steady state, start up, shut down and ORing switch waveforms. It indicates that with external VREG5 power supply, TPS56C215 could support applications with input voltages as low as 4 V. 5 V and 12 V rails switches can be realized smoothly

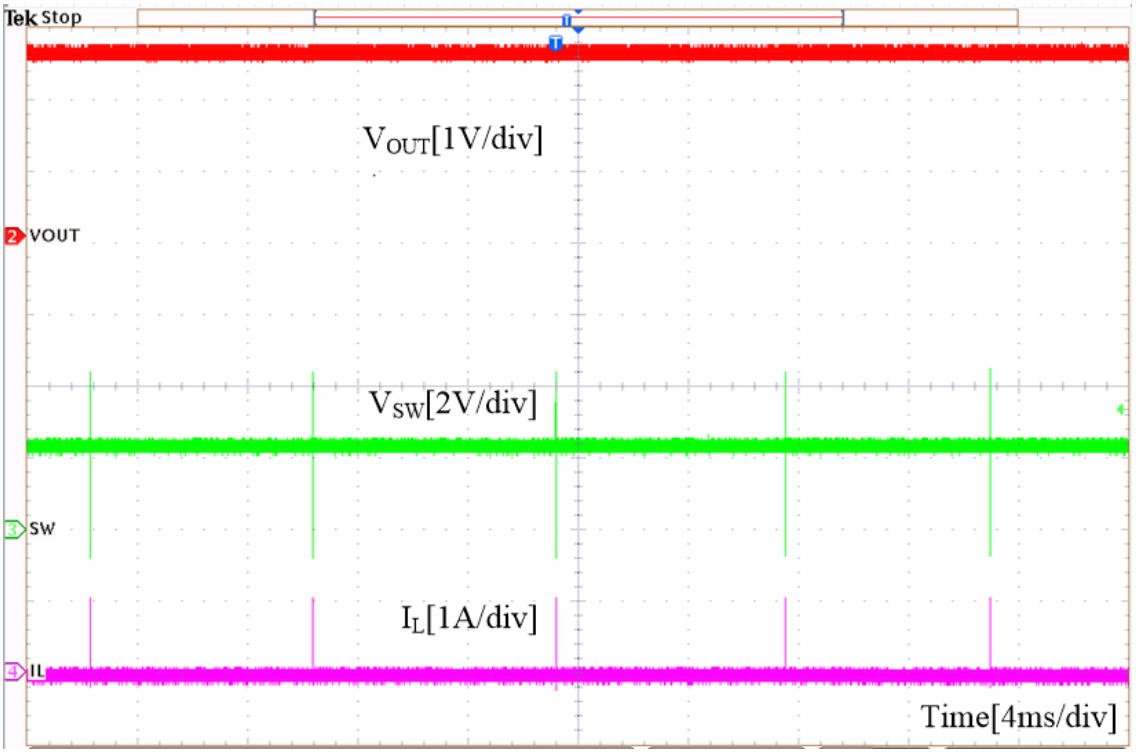

Figure 6. Steady State, V_{IN}= 4 V, I_{OUT}= 0 A

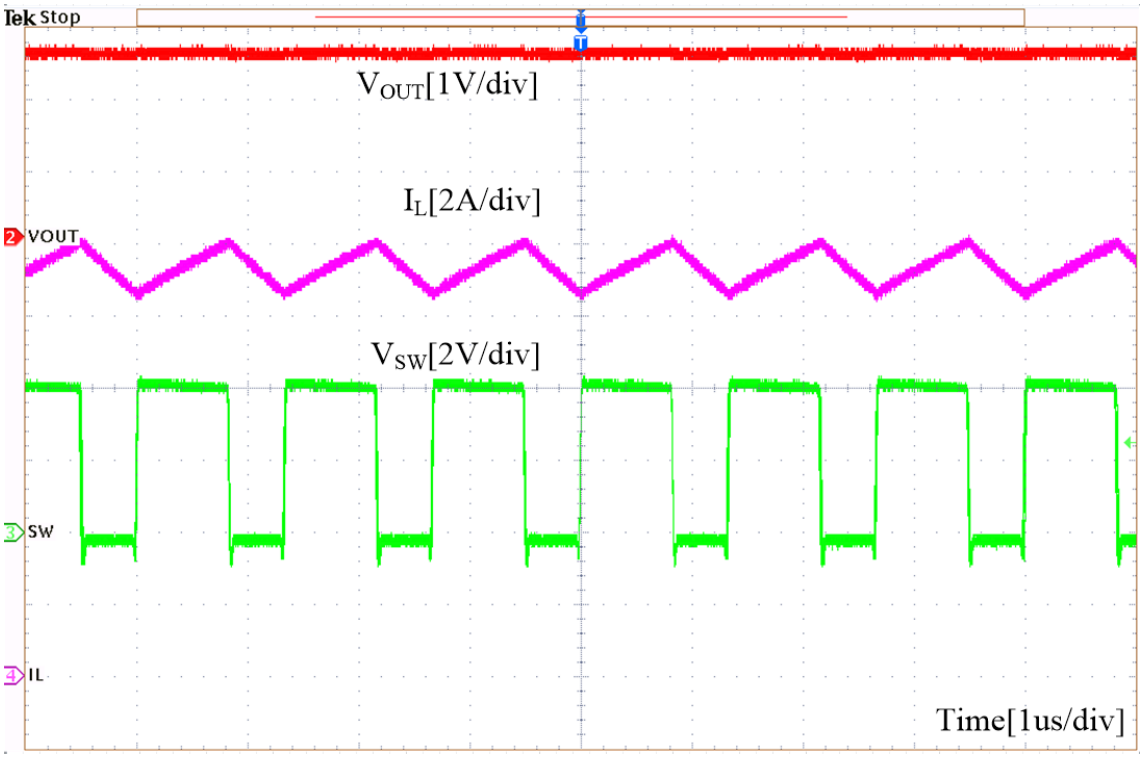

Figure 7. Steady State, V_{IN}= 4 V, I_{OUT}= 12 A

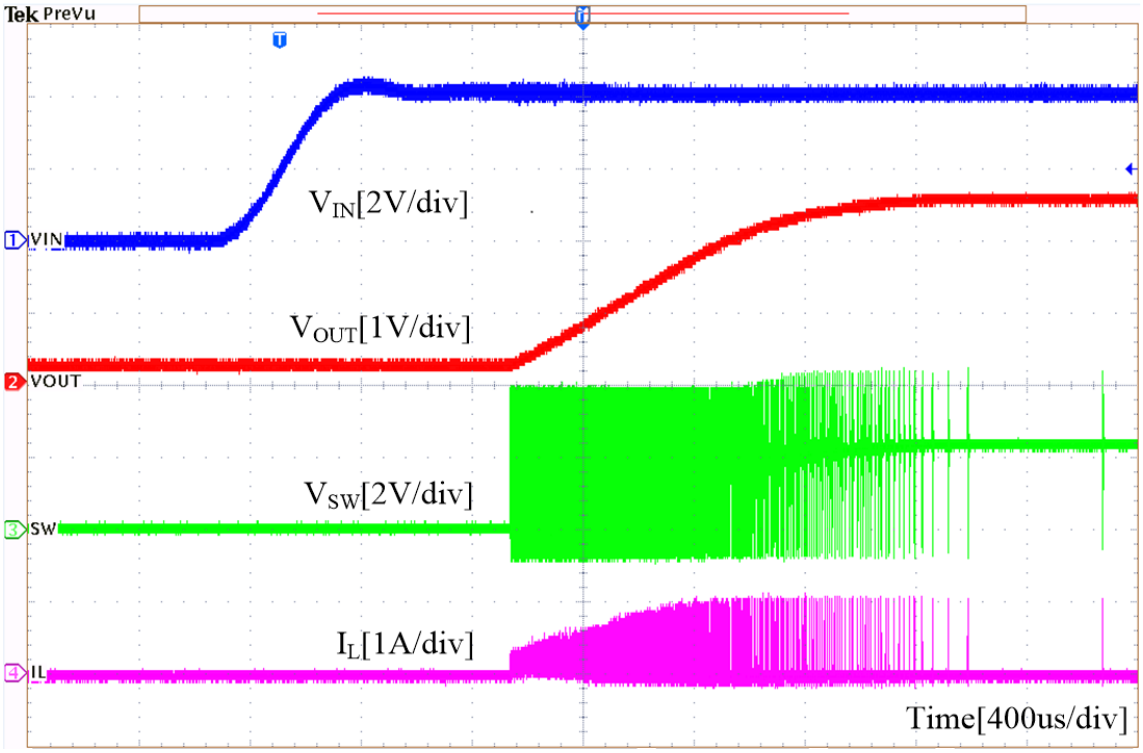

Figure 8. Start Up, V_{IN}= 4 V, I_{OUT}= 0 A

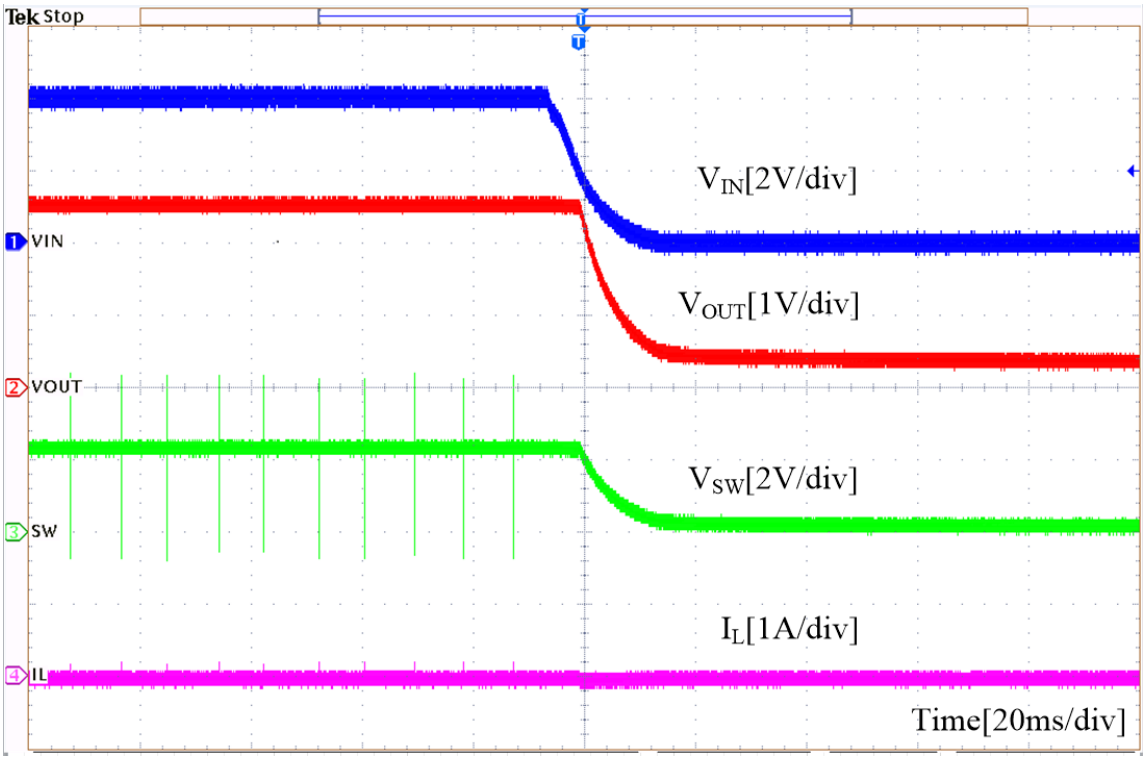

Figure 9. Shut Down, V_{IN}= 4 V, I_{OUT}= 0 A

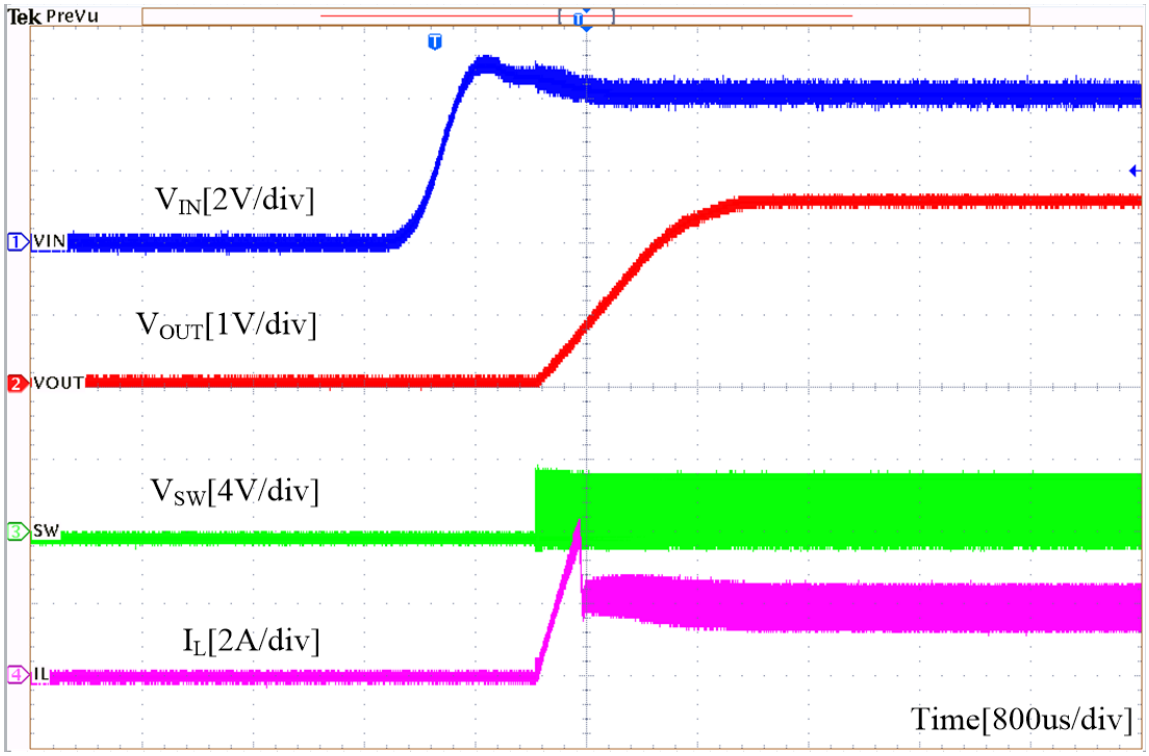

Figure 10. Start Up, V_{IN}= 4 V, I_{OUT}= 2 A

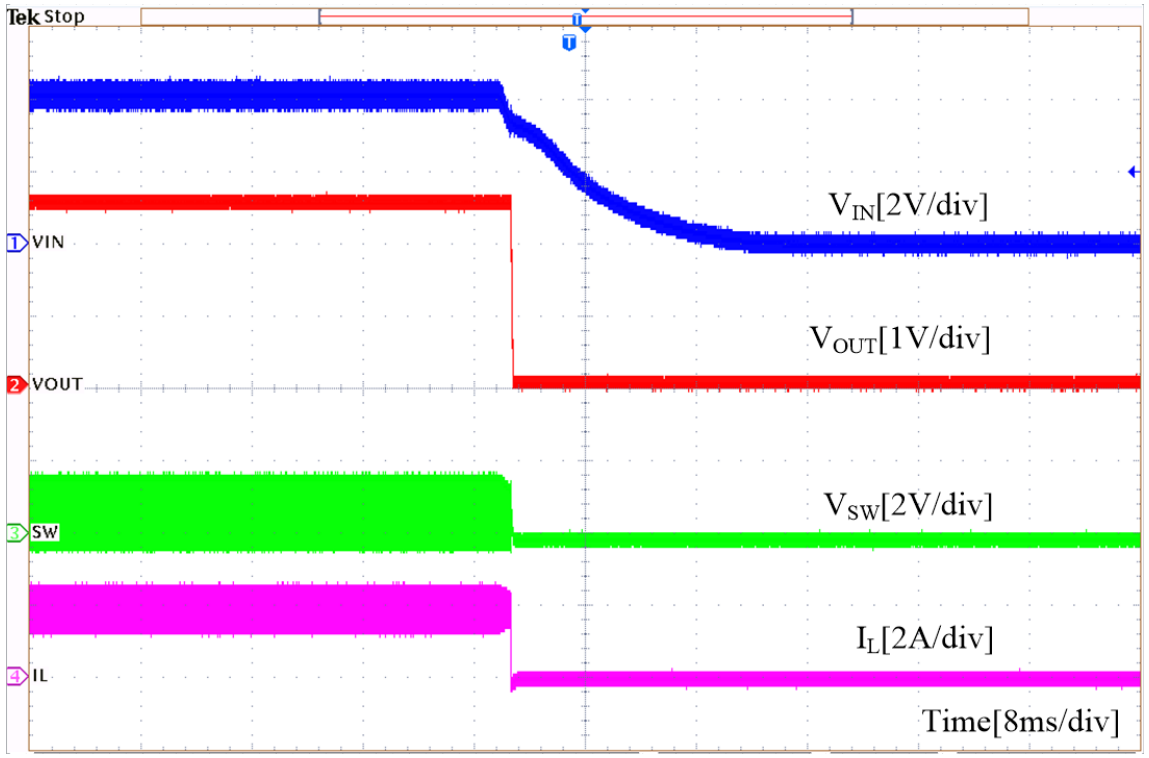

Figure 11. Shut Down, V_{IN}= 4 V, I_{OUT}= 2 A

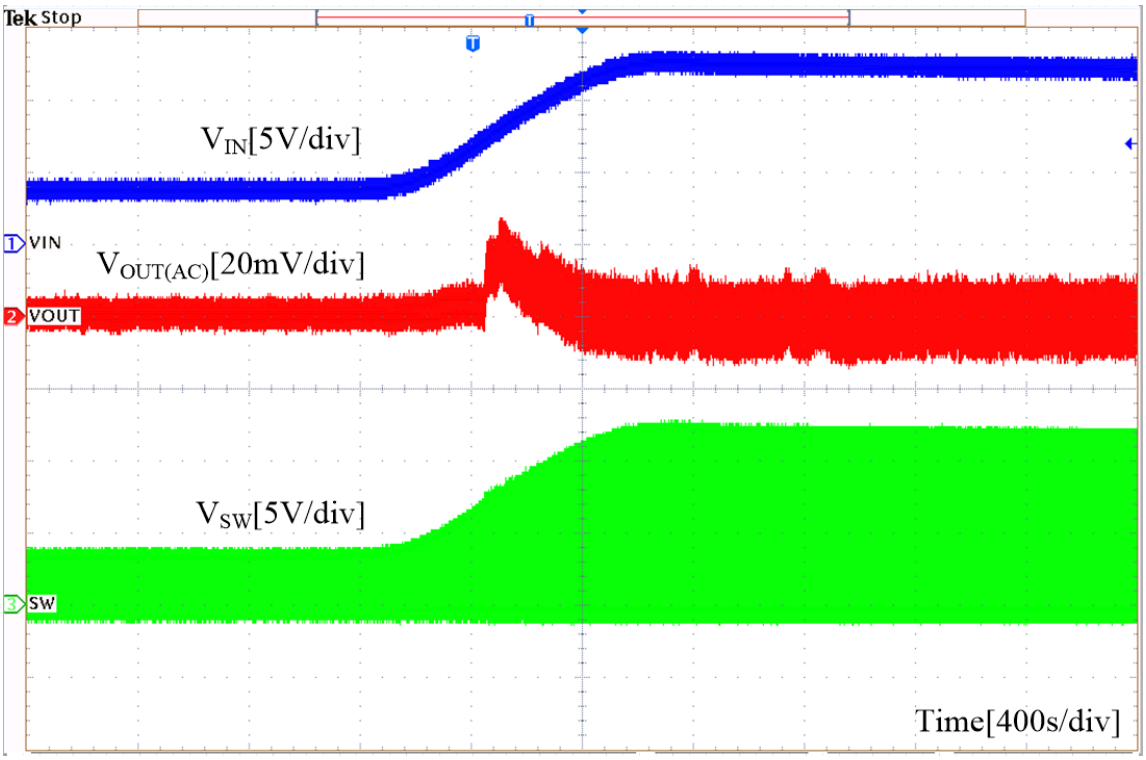

Figure 12. O-ring Switch, V_{IN} 5 V to 12 V, I_{OUT}= 2 A

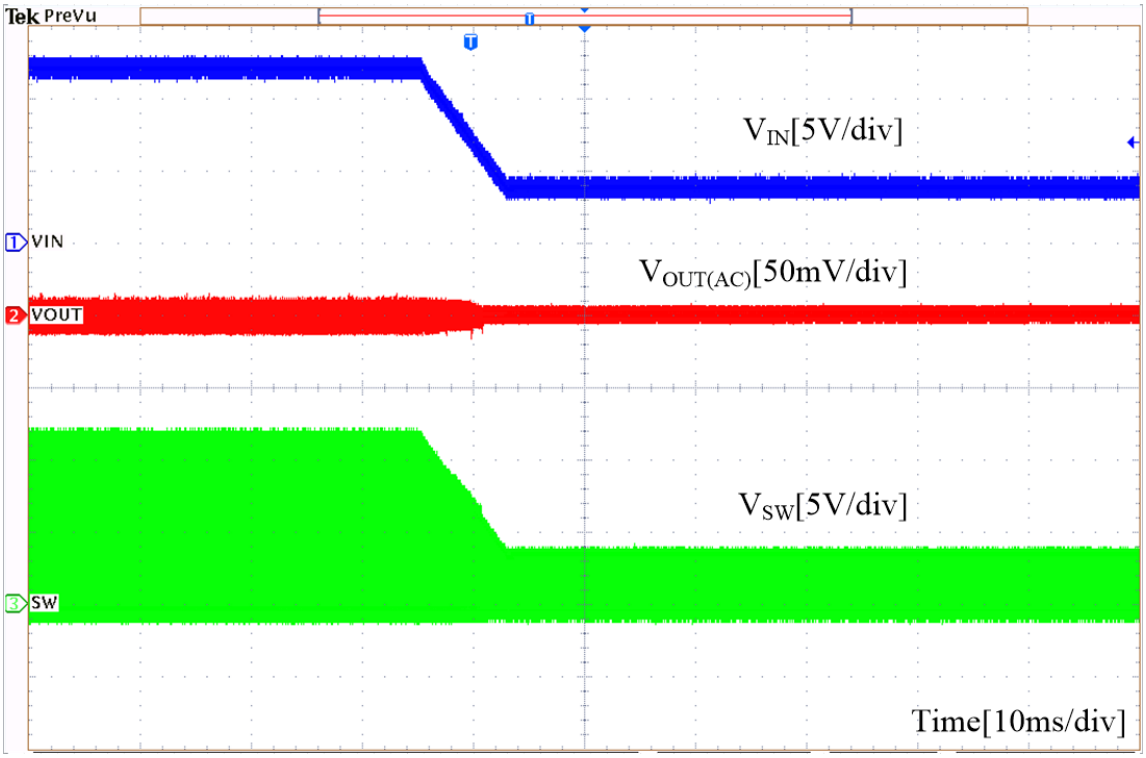

Figure 13. O-ring Switch, V_{IN} 12 V to 5 V, I_{OUT}= 2 A

4 Conclusion

5 V and 12 V ORing supply rails are common in server applications. Using the system 5 V rail as an external VCC bias supply could extend the minimum input voltage while also improving 12 V rail efficiency. The detailed schematic based on TPS56C215, along with bench testing, both verify the theory.

5 References

1. Texas Instruments, *TPS56C215 3.8-V to 17-V Input , 12-A Synchronous Step-Down SWIFT™ Converter*
2. Texas Instruments, *TPS56C215 EVM User Guide*

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