Application Report
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Adjustable Undervoltage Lockout Circuit Used in TPS61022 and TPS61023

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ABSTRACT

TI's TPS61022 and TPS61023 boost converters can operate down to a 0.4-V input voltage after the devices start up. However, a higher undervoltage lockout value is required in some applications. This application report proposes an external circuit that can adjust the undervoltage lockout voltage between 0.4 V and 1.7 V.

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Trademarks

1 Introduction

Table 1 is a portion of the electric specification from the TPS61022 and TPS61023 data sheet. The undervoltage lockout (UVLO) threshold is 1.7 V at the rising edge and 0.4 V at the falling edge. This means if the EN pin is logic high:

- The device starts up when the VIN pin is higher than 1.7 V.
- After the output voltage (VOUT) rises higher than 2.2 V, the device only shuts down again after the input voltage becomes lower than 0.4 V.

Table 1. TPS61022 and TPS61023 VIN pin UVLO Specification

Parameter		Test Condition	TYPICAL	MAX	Unit
V_{IN_UVLO}	Undervoltage lockout threshold	V_{IN} rising	1.7	1.8	V
		V_{IN} falling	0.4	0.5	V

This ultra-low UVLO feature is useful in applications such as a super-capacitor power system. It helps to utilize all the energy from the super capacitor. However, the feature is not always desired. If the converters are powered with two alkaline batteries in series, of which the operation voltage is between 3.2 V to 1.4 V, the minimum operating voltage is unnecessary to below 1.2 V. Shutting down the boost converter at a higher voltage can help to select the external components easily, such as an inductor and capacitor, and it also helps to protect the battery from being overly discharged.

This application report introduces a circuit to shut down the TPS61022 and TPS61022 devices at a voltage higher than 0.4 V. Using the TPS61022 device as example, theoretical analysis and bench test result are presented to verify the proposed circuit.

2 Proposed Circuit Principle

The proposed solution utilizes a special feature of the EN logic threshold voltage, as shown in Table 2:

- When V_{IN} > 1.8 V or V_{OUT} > 2.2 V, the EN logic high threshold V_{EN_H} is 1.2 V.
- After the device starts to operate, the typical EN logic low threshold V_{EN_L} is typically 0.42 V, with a minimum of 0.35 V and a maximum of 0.42 V

Table 2. TPS61022 EN pin Specification

Parameter		Test Condition	MIN	TYPICAL	MAX	Unit
V_{EN_H}	EN logic high threshold	V_{IN} > 1.8 V or V_{OUT} > 2.2 V			1.2	V
V_{EN_L}	EN logic low threshold	V_{IN} > 1.8 V or V_{OUT} > 2.2 V	0.35	0.42	0.45	V

Figure 1 shows a simplified schematic of the proposed solution. The operating principle details follow:

- At the beginning, the device V_{IN} < 1.7 V and V_{OUT} = 0 V. The device shuts down and disconnects VIN and VOUT. The NMOS Q1 turns off and the voltage at EN pin V_{EN} is equal to V_{IN}.
- When V_{IN} increases to higher than a typical 1.7 V (maximum 1.8 V) and EN voltage is higher than the logic high threshold, the device starts to operate. The EN logic high threshold is typically 0.95 V with a maximum value of 1.2 V. As V_{EN} = V_{IN} > 1.7 V, the device begins the soft-start process. During the soft-start process, the device initially pre-charges the V_{OUT} closed to V_{IN}, then switches to boost the output to the higher voltage.
- After the V_{OUT} becomes higher than 2.2 V, the UVLO value of the VIN pin is changed to typical 0.4 V and the EN logic low threshold is changed to 0.42 V. Because of the R5, R6, and C2, the Q1 gate voltage is still too low to turn on, the V_{EN} is still equal to V_{IN}.
- After the V_{OUT} ramps to the setting value and Q1 turns on, the voltage at the EN pin is defined by Equation 1.

$$V_{EN} = \frac{R_4}{R_3 + R_4} \times V_{IN} \quad (1)$$

- If VIN declines and results in V_{EN} lower than typical 0.42 V, the device shuts down. The V_{OUT} is discharged by the loading. After Q1 turns off, V_{EN} will be equal to VIN again. However, the device would keep off if V_{IN} < 1.7 V.

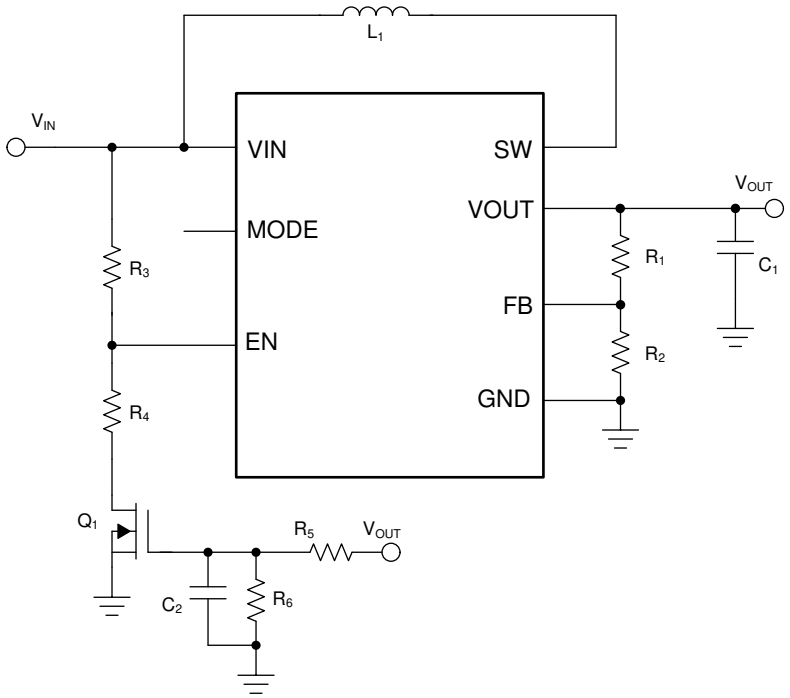

Figure 1. Schematic of the Proposed Circuit

Based on the previous analysis, the UVLO value set by this method must be lower than 1.7 V.

The function of the R5, R6, and C2 is to keep Q1 off before the VOUT is ready. But Q1 must turn on after the output voltage is stable at the setting voltage. The gate-to-source voltage at stable condition is defined by Equation 2, which should be 10% higher than the MOSFET gate to source threshold voltage for design margin.

$$V_{GS} = \frac{R_6}{R_5 + R_6} \times V_{OUT} > 1.1 \times V_{GS(th)} \quad (2)$$

where

- $V_{GS(th)}$ is the gate-to-source threshold voltage of a MOSFET
- V_{OUT} is the setting value of the output voltage

The time constant of the R5, R6, and C2, which is defined by Equation 3, is suggested to be the startup time of the device – 700 µs (typical).

$$T_{RC} = \frac{R_5 \times R_6}{R_5 + R_6} \times C_2 \quad (3)$$

Figure 2 shows the method to shut down the boost converter through an external control logic pin. The device shuts down if CTRL is high, while the device is controlled by the proposed circuit if CTRL is low. If the CTRL signal can support open-drain output, it can connect to the EN pin directly. Then the boost is off at CTRL low logic, and it is controlled by the proposed circuit at CTRL open-drain.

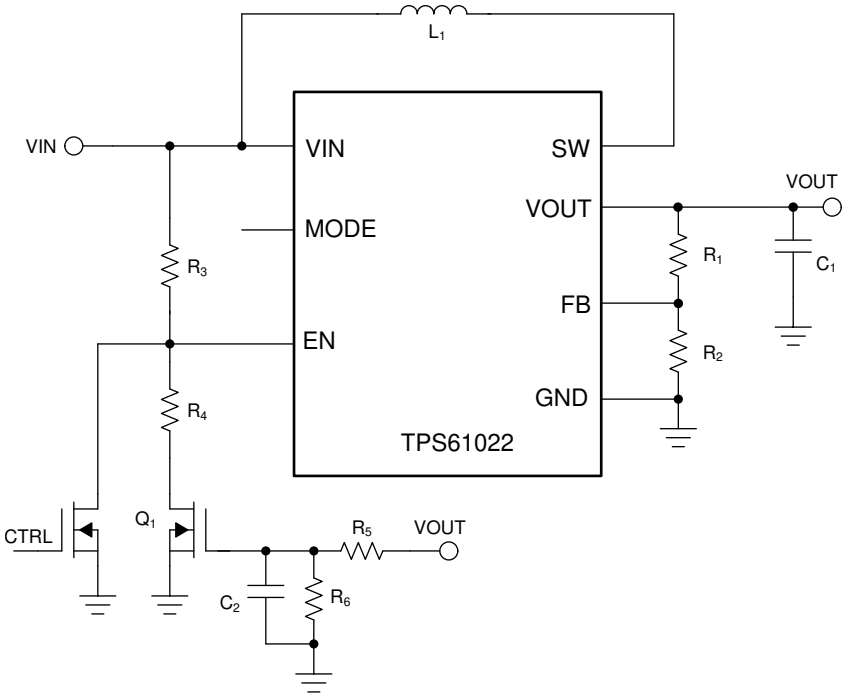

Figure 2. Method to Shutdown Proposed Circuit With I/O

Assuming the output voltage is set to 5 V and the new UVLO voltage is 1.2 V, the following process details the design of the components for the proposed circuit:

- Set R3 to be 1 MΩ, R4 will be 538 kΩ based on Equation 1. Considering the threshold variation in Table 2, the new UVLO value would have a 1-V minimum and 1.29-V maximum.
- Select CSD13381F4 as the Q1, which has a typical 0.85-V gate-to-source threshold voltage $V_{GS(th)}$ with a 0.65-V minimum and 1.1-V maximum at room temperature. Considering the variation of $V_{GS(th)}$ overtemperature, the gate-to-source voltage must be higher than 1.2 V to safely turn on the MOSFET. Select 1-MΩ R5, the R6 would be 359 kΩ according to Equation 2.
- Select the time constant of the R5, R6, and C2 to be 700-µs (TPS61022 start up time), the C2 would be 2.6 nF from Equation 3.

Figure 3 shows the value of the external components.

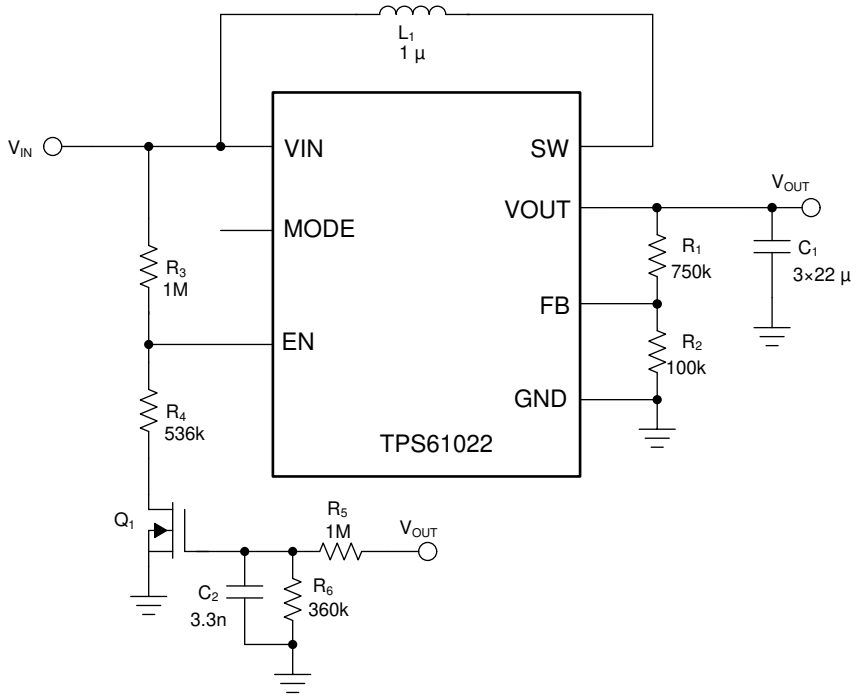

Figure 3. Components Value of the Proposed Circuit

3 Bench Test

After adding the proposed circuit, the startup waveform is shown in Figure 4.

- When the V_{IN} is lower than 1.7 V, the TPS61022 device shuts down. The VOUT is zero and the EN pin voltage is equal to the input voltage.
- After V_{IN} > 1.7 V, the TPS61022 device starts to operate. The VOUT ramps up to 5 V. Then Q1 turns on and the EN pin voltage decreases to 0.6 V. If the V_{EN} is still higher than the EN pin logic low threshold, the device keeps operating.

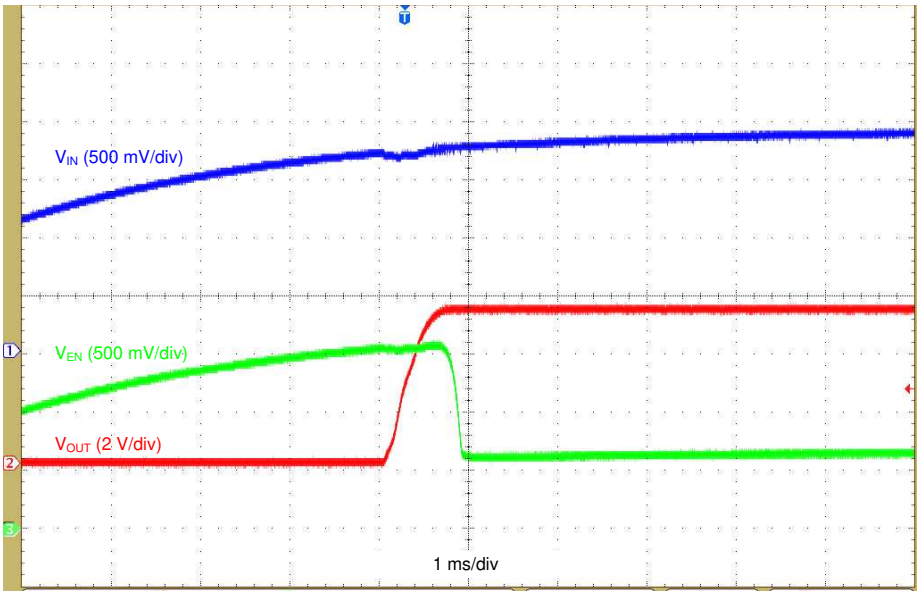

Figure 4. Startup After Adding Proposed Circuit

The Figure 5 shows the shutdown waveform at 1-mA load condition as the V_{IN} deceases. As the V_{IN} decreases toward 1.2 V, the EN also decreases toward 0.42 V. Once the EN pin voltage is lower than 0.42 V, the device stops operating and V_{OUT} decreases. After V_{OUT} decreases below approximately 2.4 V, Q1 turns off and the V_{EN} becomes equal to VIN again. The VIN is lower than 1.7 V, so the device does not restart, although the EN pin becomes logic high again.

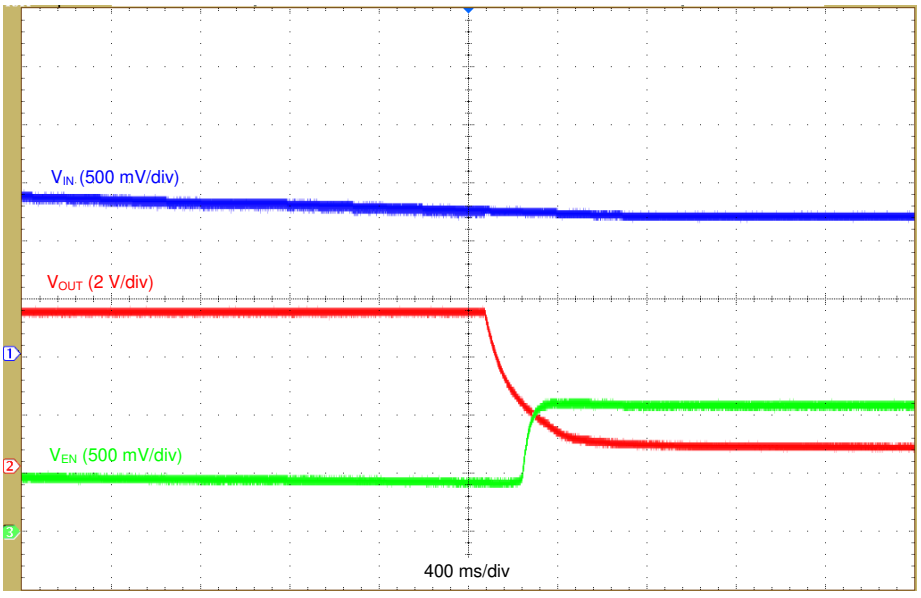

Figure 5. Shutdown at 1-mA Condition

Figure 6 shows the shutdown waveform at the 500-mA load condition. The boost converter shuts down when V_{IN} is lower than 1.2 V as designed. Because of the voltage drop across the input cable, the input voltage increases 100 mV after device shuts down.

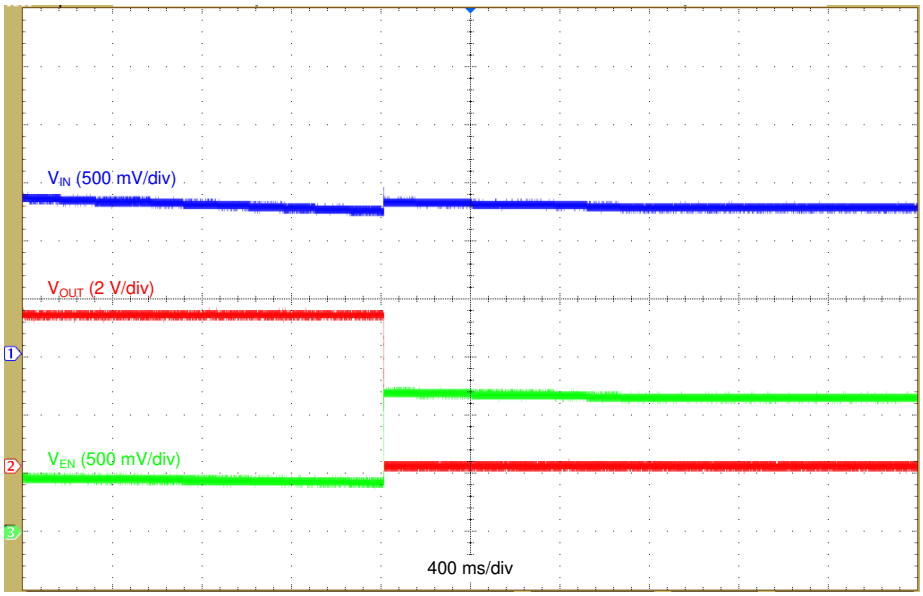

Figure 6. Shutdown at 500-mA Load

4 References

1. Texas Instruments, *TPS61022 8-A Boost Converter With 0.5-V Ultra-low Input Voltage Data Sheet*
2. Texas Instruments, *TPS61023 3.7-A Boost Converter with 0.5-V Ultra-low Input Voltage Data Sheet*

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