Application Report
SLVAES4–May 2020

TPS61022 and TPS61023 Boost Converters Layout Guidelines

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ABSTRACT

For all switching power supplies, especially those running at high switching frequencies and high currents, layout is an important design step. The TPS61022 device is a high-current capability boost converter with valley switch current limit up to 8 A and the valley switch current limit of the TPS61023 is typically 3.7 A. It is critical for engineers to take care of the layout at an early stage. Poor PCB layout introduces larger PCB parasitic inductance and capacitance, which causes unstable switching waveforms, poor output load regulations, electromagnetic interference (EMI) problems, and even IC damage.

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Trademarks

1 Introduction

The TPS61022 device is a synchronous step-up converter which is designed to operate from an input voltage supply range between 0.5 V and 5.5 V with 8 A (typical) valley switch current limit. It typically operates at a quasi-constant frequency pulse width modulation (PWM) at moderate to heavy load currents. The switching frequency is 1 MHz in the V_{IN} range higher than 1.5 V and keeps at 0.6 MHz when the input voltage is below 1 V. The TPS61023 device has the same control method with the TPS61022 device but its typical switch current limit is 3.7 A. The TPS61022 and TPS61023 data sheets and evaluation module (EVM) user's guides provide the layout guideline and example layout for an engineer to copy. This application note presents the design considerations for a proper step-by-step layout design.

2 Placement of Layers

As a general rule, the ground or DC voltage planes in a multilayer PCB is recommended to be placed between the main current component layer and small signal trace layer. The ground or DC voltage planes help shield the sensitive small signal traces, such as feedback trace, EN, Mode traces from noisy switch nodes, and power components. Figure 1 shows the (a) recommended placement of layers and (b) not recommended placement layers. The (b) configuration causes capacitive noise coupling between the high speed, high current voltage power layer and small analog signal layer.

Layer 1: Power Traces and Compoents
Layer 2: Ground Plane
Layer 3: Small Signal
Layer 4: Small Signal

(a) Recommended

Layer 1: Power Traces and Compoents
Layer 2: Small Signal
Layer 3: Small Signal
Layer 4: Ground Plane

(b) Not Recommended

Figure 1. Placement of Layers

Besides implementing the recommended placement of layers, it is also desirable to have thick and wide enough copper for the high-current traces to minimize the PCB conduction loss and optimize the thermal performance.

3 Output Capacitors Placement and Routing

Figure 2 shows the continuous current path and discontinuous current path in a non-synchronous boost converter. The blue solid line represents the continuous current path. The red dashed line represents the discontinuous current path. When the power MOSFET Q is turned on, the current flows through the inductor L, power MOSFET Q and back to input voltage supply V_{IN}. When the power MOSFET Q is turned off, current will flow through the inductor L, Schottky diode D, output capacitor C_{OUT} and back to input voltage supply V_{IN}. Figure 3 shows the PCB parasitic inductors in discontinuous current path. The loop formed by power MOSFET Q, Schottky diode D, output capacitor C_{OUT} must be minimized as short as possible because the PCB parasitic inductors in these high di/dt current paths will generate high voltage spikes at output and across power MOSFETs. The spikes and ringing at switch node SW is the source of EMI and may cause power MOSFET overvoltage damage. To minimize the influences of PCB parasitic inductors Lpara1, Lpara2, and Lpara3, the power MOSFET Q, Schottky diode D should be placed close to each other and a low ESL and ESR X5R or X7R dielectric ceramic capacitor C_{OUT1} is better to be placed across to the Schottky diode cathode and MOSFET source shown in Figure 3.

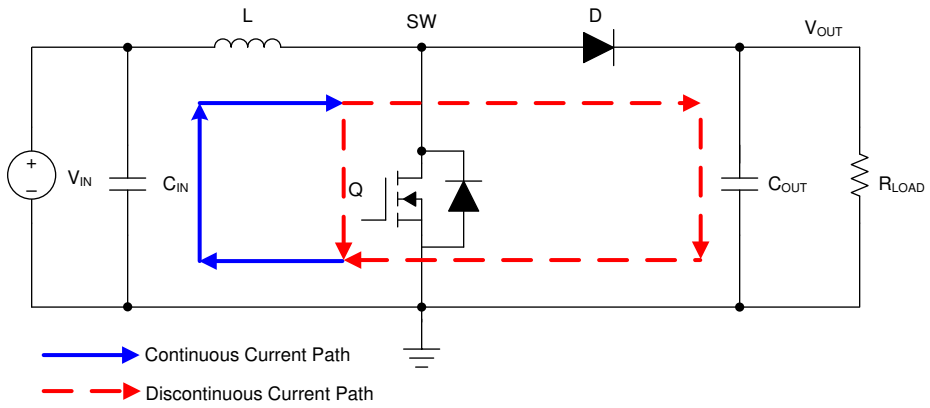


Figure 2. Continuous and Discontinuous Current Paths

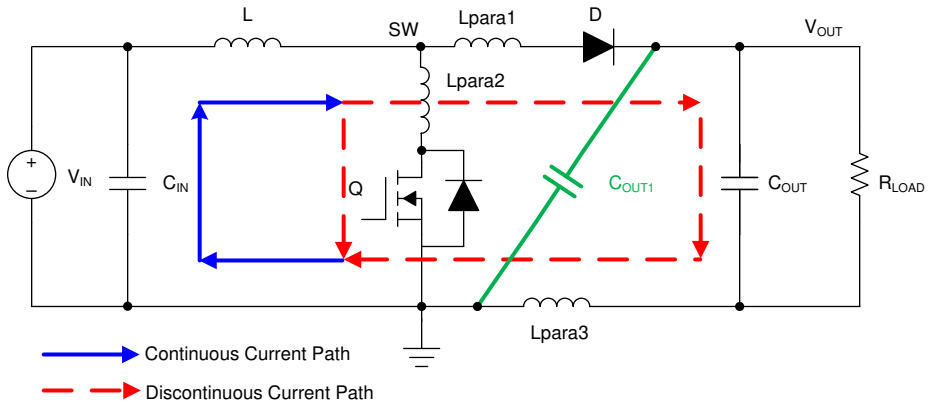


Figure 3. PCB Parasitic Inductors in Discontinuous Current Paths

Figure 4 shows the TPS61022 EVM schematic. This application note presents the layout guidelines based on the TPS61022. The analysis and suggestions also apply to TPS61023 layout.

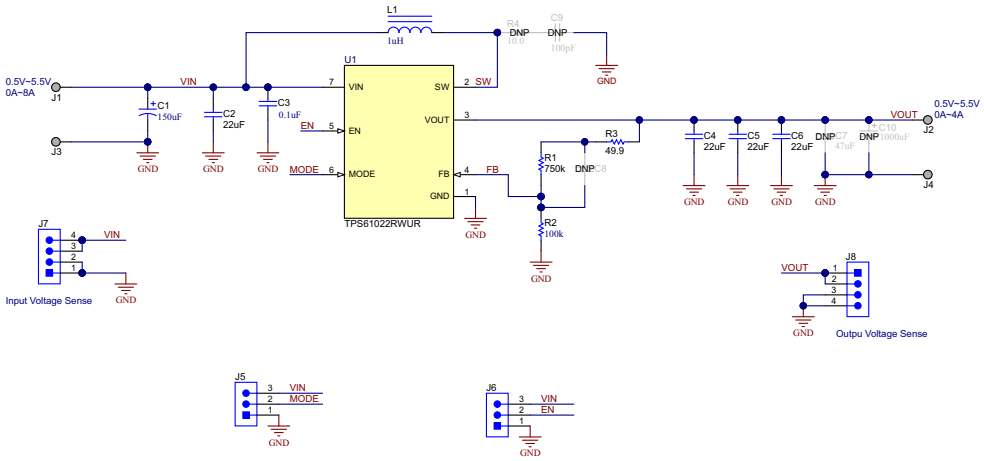


Figure 4. TPS61022 EVM Schematic

Figure 5 shows the recommended output capacitor placements for the TPS61022. Three 0805 package X5R dielectric capacitors are placed in parallel and close to the IC. This is the easy and recommended way since it has minimum parasitic inductance. Figure 6 shows the recommended output capacitors placements for the TPS61023. Two 0603 package X5R dielectric capacitors are placed in parallel and close to the IC with wide copper.

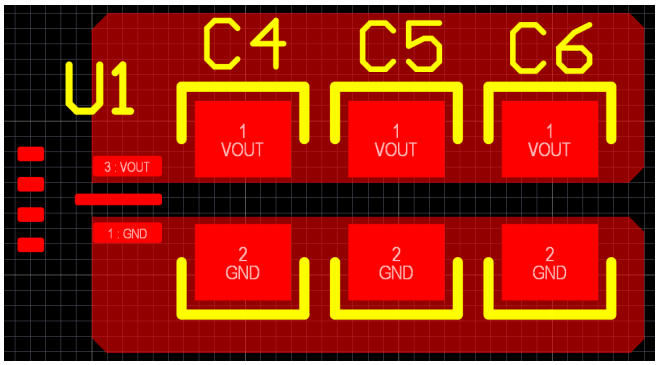


Figure 5. Recommended Output Capacitors Placement for TPS61022

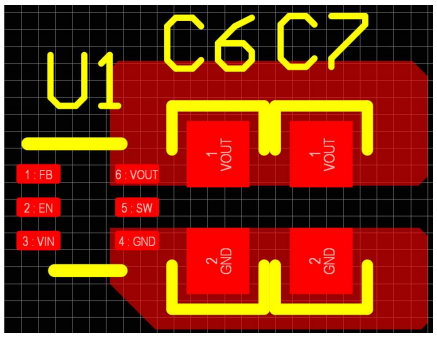
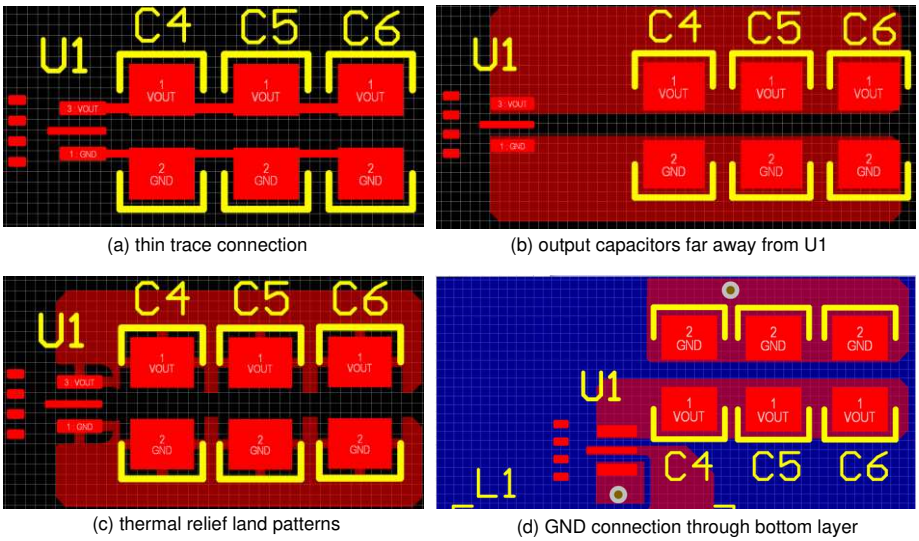


Figure 6. Recommended Output Capacitors Placement for TPS61023

Figure 7 shows four common output capacitor placement mistakes. (a) Use a thin 10-mil trace to connect IC and ceramic capacitors. The PCB parasitic inductance is big and the trace has a big voltage drop, which may affect the normal switching. (b) Ceramic capacitors are put far away from the IC, which introduces big parasitic inductors. (c) Unnecessary use of thermal relief land patterns increases the interconnection impedance of power components. (d) The ceramic capacitors are placed in the opposite direction. IC GND is connected to ceramic capacitor GND pads through the bottom layer and only one via. This results in higher power losses and big parasitic inductance.



(a) thin trace connection (b) output capacitors far away from U1

(c) thermal relief land patterns (d) GND connection through bottom layer

Figure 7. Four Common Output Capacitor Placement Mistakes

In some applications an aluminum electrolytic capacitor is needed to buff the energy to achieve low voltage drop during load transient from 0 A to a heavy load. Another common mistake is using one 1-nF to 100-nF 0402 package ceramic capacitor and one bulk aluminum electrolytic capacitor combination as Figure 8 shows. The small value 1-nF to 100-nF 0402 package ceramic capacitor does not help to eliminate the PCB parasitic inductance influence because the main power current will flow through the aluminum electrolytic capacitor.

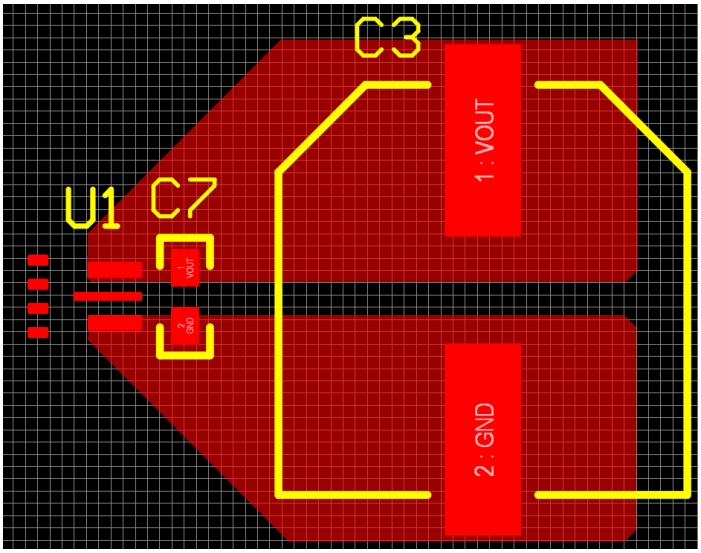


Figure 8. One Ceramic Capacitor and One Aluminum Electrolytic Capacitor Combination

4 Inductor and Snubber Circuit Placement and Routing

For the TPS61022 and TPS61023 devices, the SW pin is in the middle of the VOUT pin and GND pin, place the SW trace underneath the device so that output ceramic capacitors are still placed close to the IC. Figure 9 shows the inductor and snubber circuit placement example. To reduce the radiated EMI, place the inductor close to the IC. Make the copper wide enough to handle the larger power current and provide a heat sink. However, to minimize the coupling capacitance between SW node and other noise-sensitive traces, minimize the SW copper area.

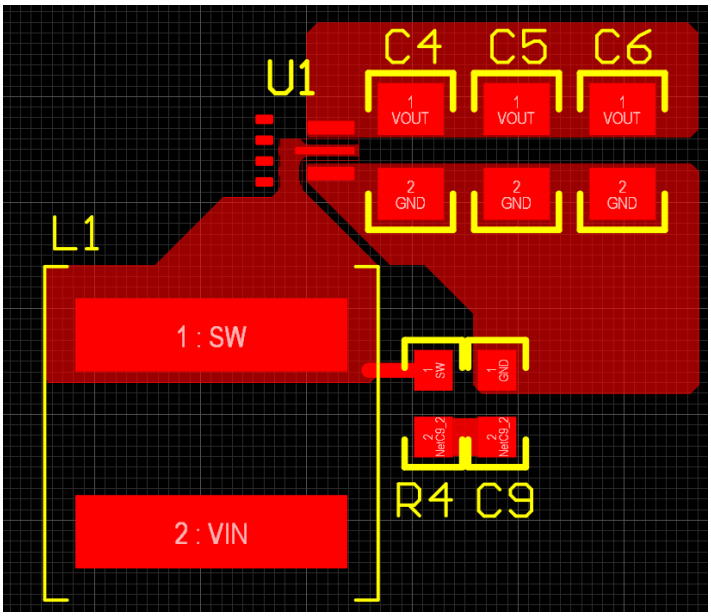


Figure 9. Inductor and Snubber Circuit placement

Figure 7 (d) shows a bad SW trace example. The SW trace is placed right of the IC so there is no room to connect IC GND pin to output ceramic capacitors GND pads directly on top layer.

The Snubber circuit helps reduce the SW node spikes at heavy load and optimize EMI. It is usually preferred to be placed close to SW node so that the loop area and parasitic inductance is small. A ground copper area placed underneath the inductor and snubber circuit on inner layer 1 would help provide additional shielding.

5 Feedback Network Placement and Routing

The feedback loop is sensitive to noise so place the feedback networks close to the FB pin. The FB trace between components and IC should be as short as possible to avoid noise coupling from SW node. Never route the FB trace in parallel with SW node closely. Figure 10 shows the example of feedback network placement and routing with the TPS61022 device. The suggestions also apply to TPS61023 layout.

A small ceramic capacitor of 1-µF or 0.1 µF is suggested to be put close to the VIN pin of the IC.

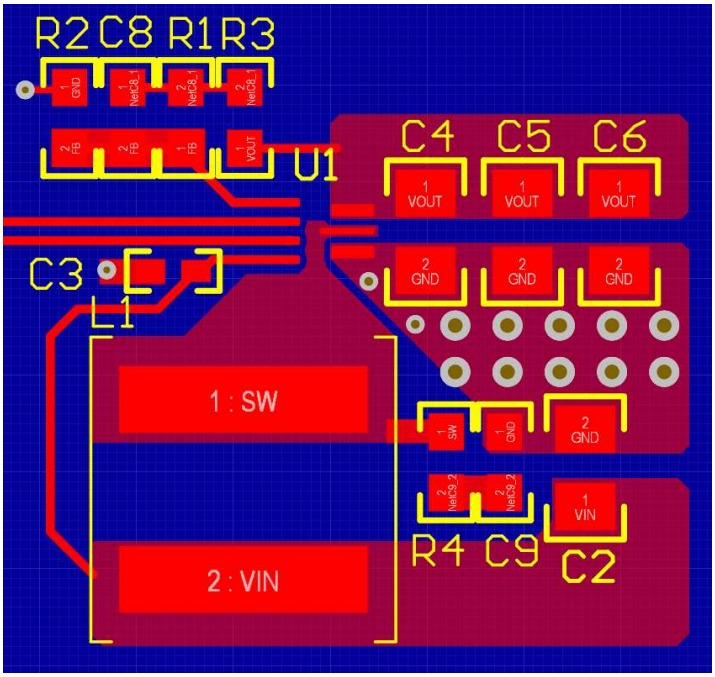


Figure 10. Place and Route the Feedback Network and Other Components

6 Thermal Performance Optimization

The TPS61022 switch valley current limit is 8 A typically and is able to output 20 W from 3.6-V input voltage. It offers a very small solution size with its 2-mm × 2-mm VQFN package. To optimize the thermal performance, use larger and thicker PCB copper for the power pads (GND, SW, and VOUT) to enhance the thermal performance. Using more vias connects the ground plane and VOUT plane on the top layer and bottom layer around the IC improves the thermal capability.

The TPS61023 switch valley current limit typical value is 3.7 A. It has a 1.2 mm × 1.6-mm SOT563 package. For better thermal performance, enlarge the copper area connected to FB, EN and VIN pins like Figure 11.

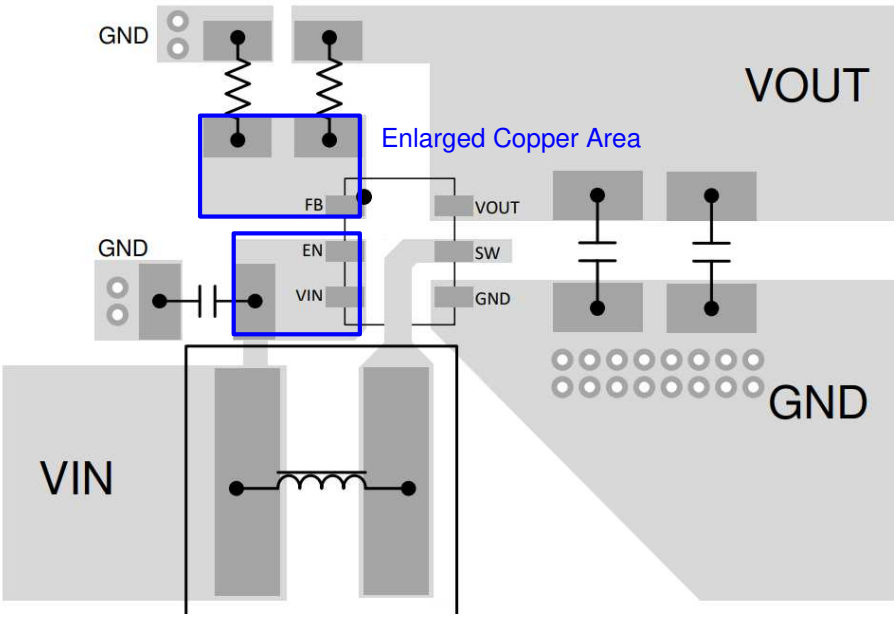


Figure 11. TPS61023 Layout

7 Reference

- Texas Instruments, *TPS61022 8-A Boost converter with 0.5-V ultra-low input voltage Data Sheet*
- Texas Instruments, *TPS61022EVM-034 Evaluation Module User's Guide*
- Texas Instruments, *TPS61023 3.7-A Boost Converter with 0.5-V Ultra-low Input Voltage Data Sheet*
- Texas Instruments, *TPS61023EVM-052 Evaluation Module User's Guide*

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