Application Report
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Improving Boost Converter Reliability Using the TPS61178x Hiccup Mode Short Protection

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ABSTRACT

This application note is provides guidance on handling the output short protection using TPS61178x devices. With a brief introduction to the output short protection functionality of the TPS61178x, a user guide of how to select the external components is presented to show a desired methods to safeguard a boost converter from short circuits.

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Trademarks

1 Introduction

The traditional boost converter is particularly susceptible to output short protection due to the DC path from the input to output. Usually an additional load switch is required to achieve the output short protection but it will make the circuitry more complicated and also consume more overall size and cost.

2 TPS61178x Hiccup Mode Protection

The TPS61178x integrates the hiccup mode short protection via an external P-FET as shown in Figure 1. As long as the output short condition is detected (the inductor current exceeds the short current threshold, typically 20 A or the output voltage drops below the output short threshold, typically 30% of the normal voltage), the external P-FET is turned off by disabling the internal current source sinking from the DIRDRV pin to GND.

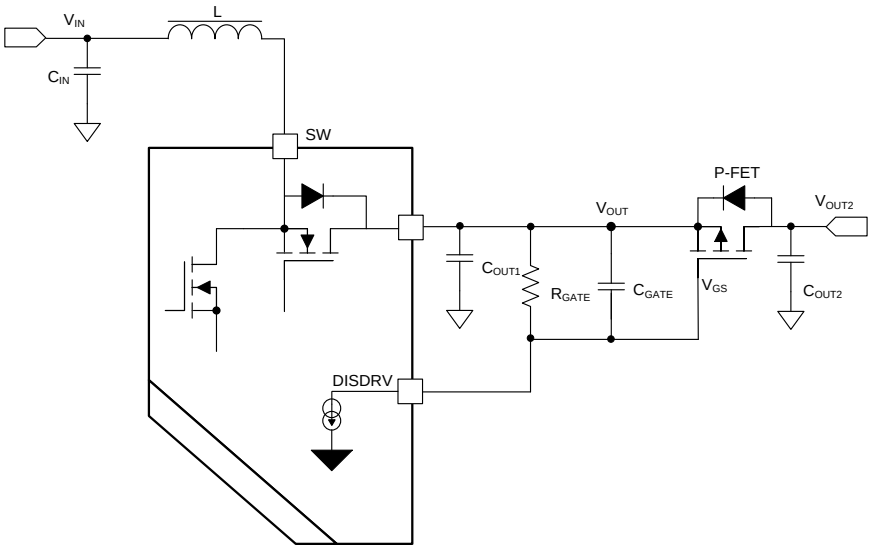

Figure 1. TPS61178x Application Circuit with External P-FET

The device is in sleep mode once it enters into the hiccup mode. At the end of the sleep time, a restart attempt is initiated by ramping up the output voltage. If the output short condition persists, the device cannot start up successfully and enters into the sleep mode again as long as the inductor current triggers the short protection threshold, this process will be repeated during the short steady-state operation. Thus, the device is in a cycle of short burst for the start up (the time is determined by the inductor current ramping up slew rate to reach the short protection threshold) and followed by an off time (typically 90 ms) in sleep mode for the continuous short status. The off time reduces the average overall load current and also lowers the power loss to cool down the system when the output short happens.

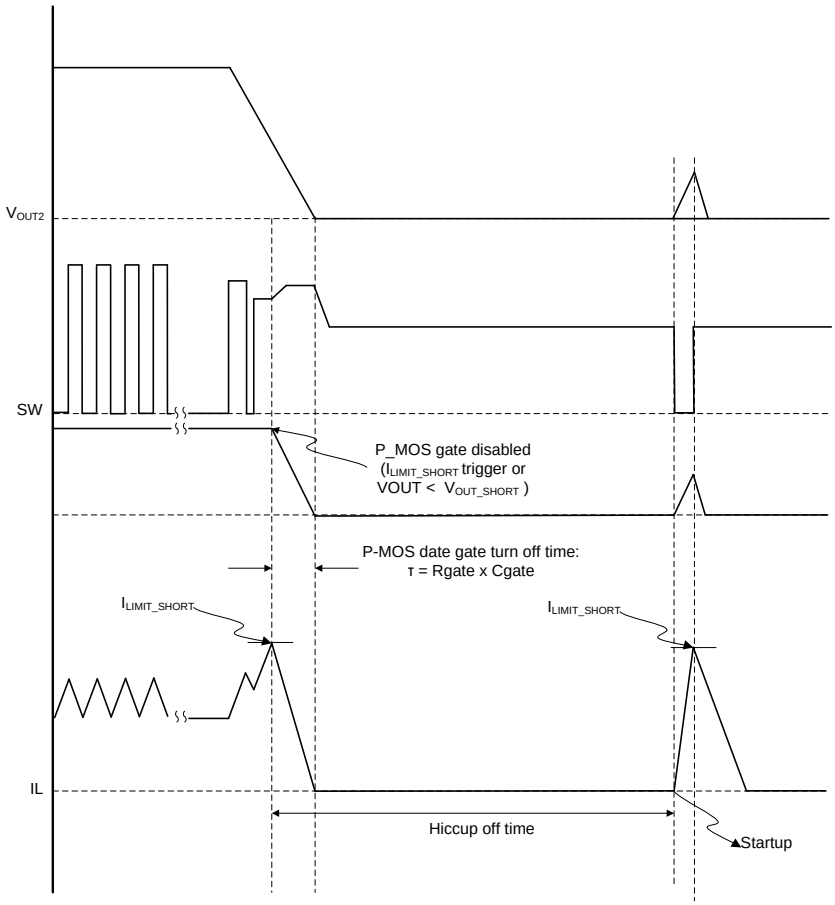

Figure 2. TPS61178x Hiccup Mode Protection Timing Diagram

3 External Components Selection

This section discusses the gate-source resistor and capacitor, and the external P-FET specification.

3.1 Gate-Source Resistor and Capacitor

The TPS61178x achieves the hiccup mode protection by turning off the external P-FET. The external P-FET, gate –source resistor (R_{GATE}) and capacitor (C_{GATE}) are the key components to achieve the robust short protection function. When the short current threshold triggers, the current source from the DISDRV pin to GND is disabled. The gate voltage (C_{GATE}) of the external P-FET is discharged to turn off via R_{GATE} connecting between the source and gate of the external P-FET.

R_{GATE} is determined by the gate driving voltage of the P-FET at normal operation (see Equation 1).

$$R_{GATE} = \frac{V_{GATE}}{I_{GATE}} \quad (1)$$

where

- V_{GATE} is the driving voltage of the external P-FET
- I_{GATE} is the gate sinking current, typically 55 µA of TPS61178x, specified in TPS61178x data sheet (SLVSDA7). For instance, V_{GATE} = 5 V (refer to the external P-FET data sheet), then R_{GATE} = 90.9 kΩ

For the C_{GATE}, it depends on the turn-on timing of the external P-FET (related to the startup inrush current).

$$C_{GATE\_ALL} = \frac{I_{GATE} \times T_{FET\_ON}}{V_{GATE\_TH}} \quad (2)$$

where

- V_{GATE_TH} is the threshold voltage of the external P-FET
- T_{FET_ON} is the turn-on time of the external P-FET during startup. For instance V_{GATE_TH} = –1 V , T_{FET_ON} = 0.5 ms, then get the C_{GATE_ALL} = 27.5 nF.

NOTE: C_{GATE_ALL} is the total capacitor of the external gate capacitor and the FET self-gate capacitance.

$$C_{GATE} = C_{GATE\_ALL} - C_{GATE\_FET} \quad (3)$$

where

- C_{GATE} is the external capacitance connecting between the source and gate of FET

With total C_{GATE_ALL} = 27.5 nF, if the C_{GATE_FET} = 1.6 nF (available from the MOSFET data sheet, SLPS570), a 25-nF external capacitor is required. Choose the closet rating 22-nF capacitor in the real application.

3.2 External P-FET Specification

For the external P-FET, the voltage and current have a straightforward calculation:

$V_{DS} = V_{OUT}$, while $I_{DS\_DC} = I_{OUT}$

NOTE: Voltage stress happens when V_{OUT2} (in Figure 1) is shorted but the V_{OUT} voltage still keeps the normal voltage.

However, the most critical specification of the external FET is the safe operation area (SOA). The heat generated during short protection:

$$Q_{GATE} = \frac{1}{2} \times V_{OUT} \times I_{SHORT} \times T_{SHORT} \quad (4)$$

For instance, V_{OUT} = 16 V, I_{SHORT} = 20 A, T_{SHORT} = 30 us. The Q_{GATE} = 4.8 mJ, the SOA should have enough margin to safeguard the device against damage caused by overstress.

Based on the aforementioned calculation, for instance the 16 V_{OUT} / 3 A I_{OUT} application case, the key specification of the external P-FET is: V_{DS} > 16 V, I_{DS_DC} > 2 A, SOA > 4.8 mJ.

TI's low $R_{DS(on)}$ P-FET - CSD25404Q3 is selected in the TPS61178x EVM, of which the V_{DS_MAX} is –20 V, I_{DS_MAX} is 18 A, and the SOA is around 14 mJ (reference the 100-µs curve in Figure 3).

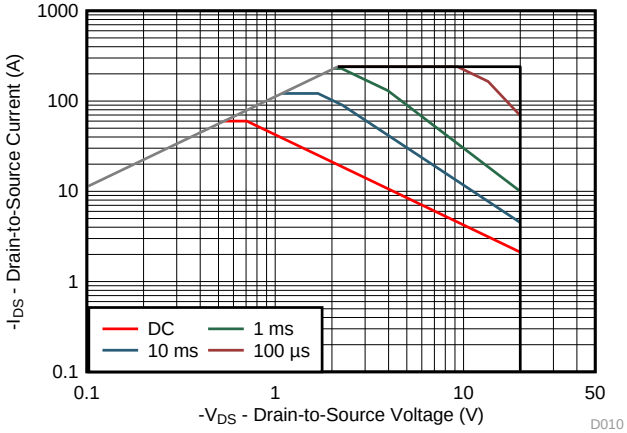

Figure 3. CSD25404Q3 SOA

4 Additional Capacitor Between Gate and GND

For the TPS61178x, when the short protection triggers, the internal current source sinking from the DISDRV pin to GND is disabled to turn off the external P-FET. However, as the V_{OUT} will ring as long the external P-FET turns off, the additional capacitor from gate (of the external P-FET) to GND could lower the ring amplitude of the voltage at the VOUT pin and avoid the oscillation when entering into the short protection.

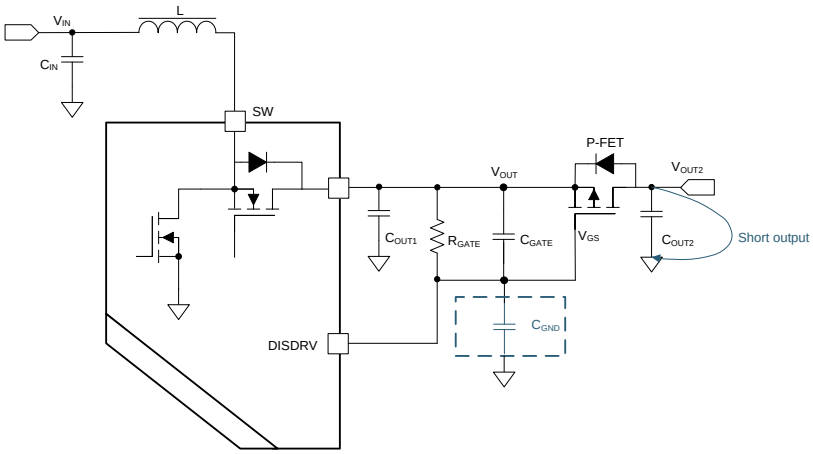

Figure 4. Additional Capacitor from Gate to GND to Improve the Short Protection

4.1 Gate-GND Capacitor Selection

During the short protection, the VOUT maximum voltage should not exceed the VOUT boost normal operating voltage to avoid the overstress issue.

The capacitor from the gate to GND could lower the VOUT voltage during short protection.

V_{OUT_CLAMP} is defined as the maximum voltage of the VOUT pin during short protection transition. V_{GATE_ON} is the gate voltage to turn on the external P-FET to support the inductor short current flowing through the external P-FET (the positive voltage from source to gate the FET).

$$(V_{OUT\_CLAMP} - V_{GATE\_ON}) \times C_{GATE} = V_{GATE\_ON} \times C_{GND} \quad (5)$$

For instance, V_{OUT_CLAMP} = 20 V, C_{GATE} = 22 nF, V_{GATE_ON} = 2 V (the source voltage reference to the gate voltage).

To attain C_{GND} = 2.5 nF, select the 2.2 nF capacitor in the real application.

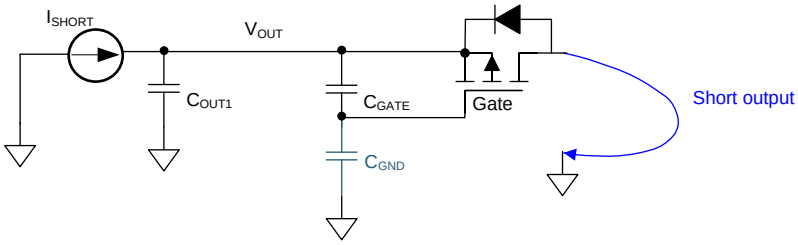

Figure 5. Additional Capacitor Connection

4.1.1 Bench Measurement With and Without a Capacitor Between Gate and GND

With the additional 2.2-nF capacitor added between the gate of the external P-FET to GND.

The VOUT ring voltage is much lower and it will protect the external P-FET against the voltage overstress risk and the short protection entry is smoother compared to the behavior without the capacitor, proven by the real bench measurement in Figure 6 and Figure 7.

Test Condition: V_{IN} = 7.2 V, V_{OUT} = 16 V, L = 3.3 µH, C_{OUT1} = 10 µF, C_{OUT2} = 3 × 22 µF , C_{GND} = 2.2 nF short output. The maximum current limit of the power supply is set to 15 A.

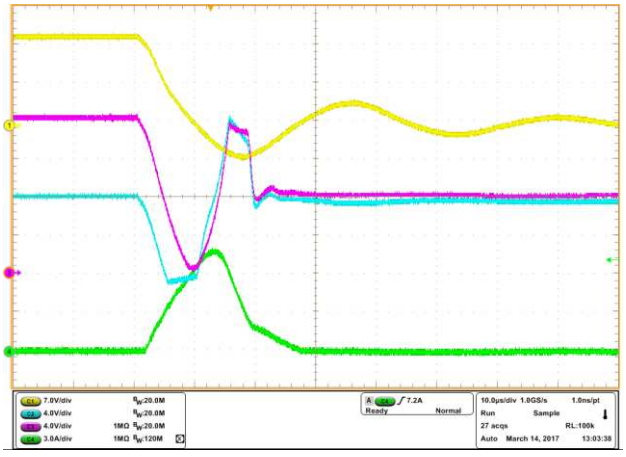

Figure 6. Short Entry With Additional Capacitor

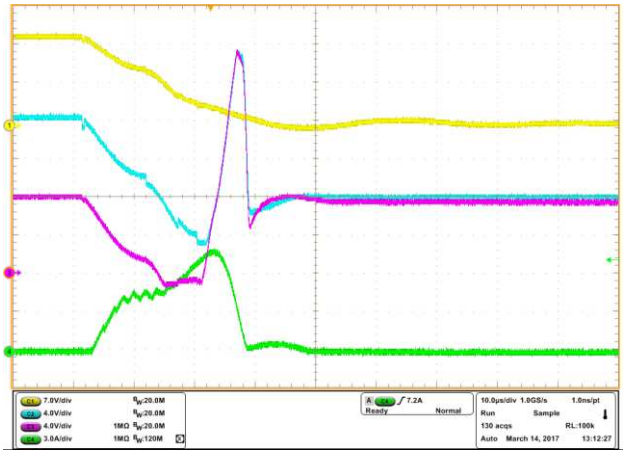

Figure 7. Short Entry Without Additional Capacitor

5 Summary

The TPS61178x uses hiccup mode protection to safeguard the device against an output short condition by reducing the power dissipation and lowering case temperature.

This application note delivers a guidance of selecting the gate resistor and capacitors to optimize the short protection behavior. The bench measurement based on the TPS61178EVM-792 is enclosed and proves the improved performance with the application guidance proposed in this application note.

6 References

- TPS61178x data sheet (SLVSDA7)
- CSD25404Q3 data sheet (SLPS570)

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